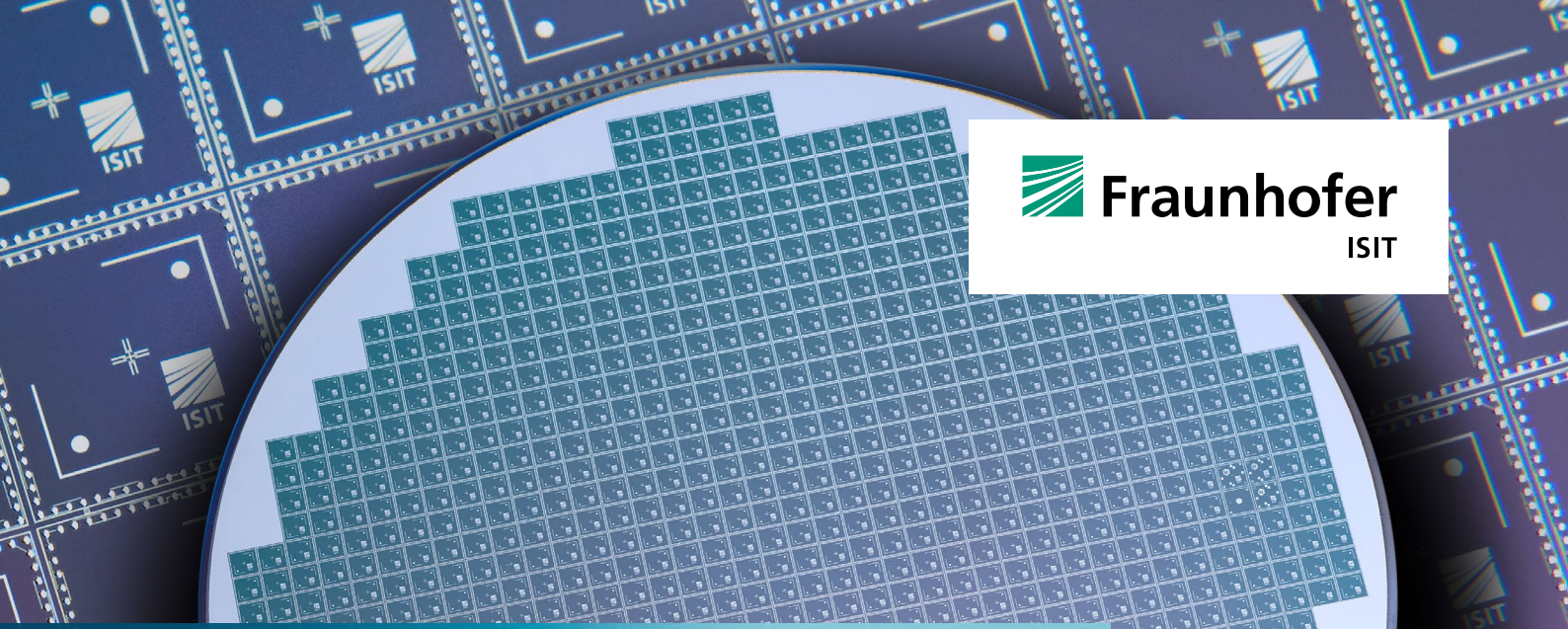


Fraunhofer ISIT

Test Wafers and Subtrates

Test chips and corresponding substrates for process development, material screening and machine demonstration

Silicon Test-Wafer

Motivation

Test wafers are typically used for material screening, process development, and machine demonstration. In contrast to product wafers, which are expensive and difficult to access, test wafers can be fabricated at lower cost with additional features beneficial for the respective application.

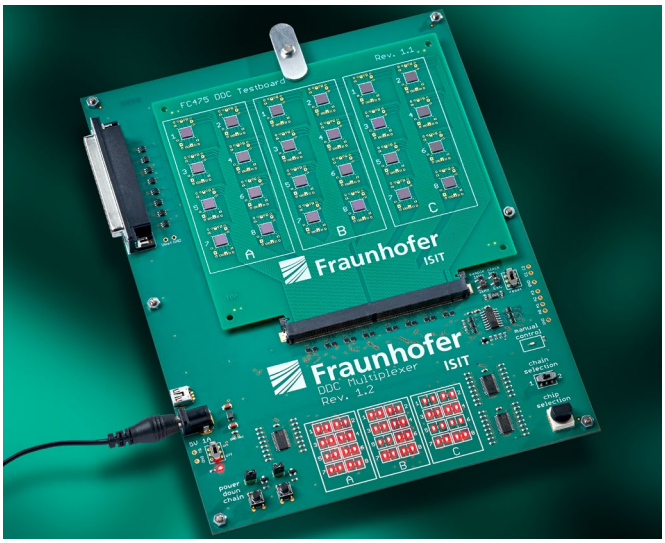
Silicon Wafers

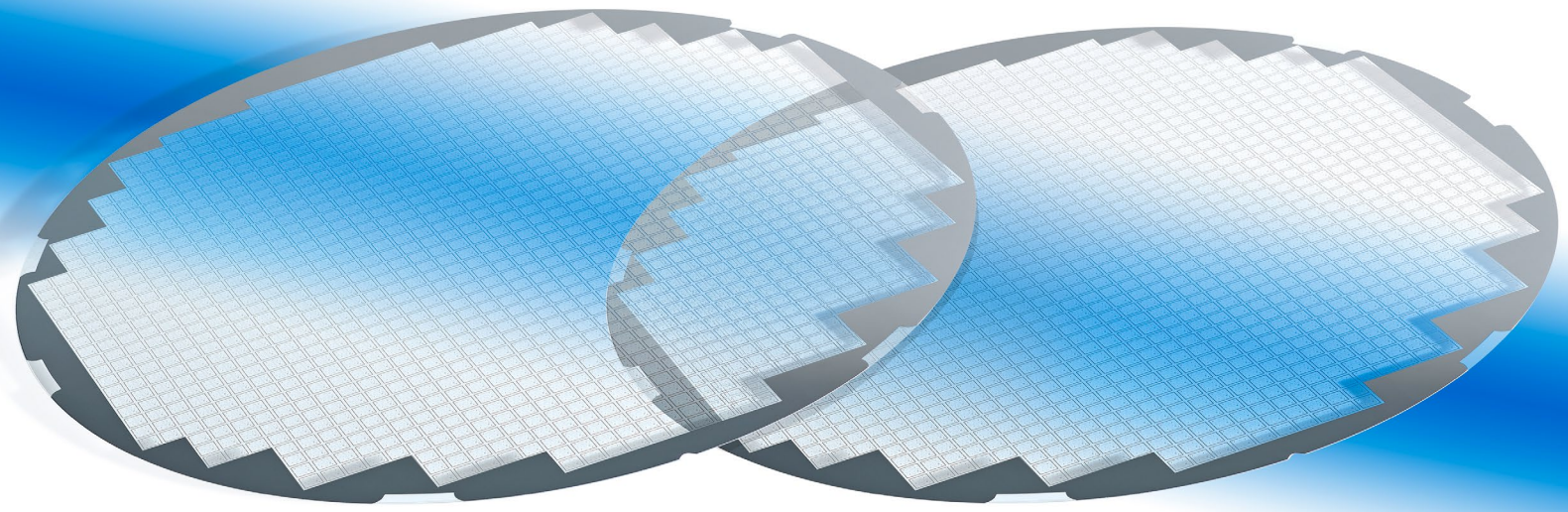
For material screening applications often silicon chips with a daisy chain are used, which enables easy contact and short measurements. Besides daisy chain resistance measurement and short detection, it is possible to determine the contact resistance of the interconnect by Kelvin probe measurements.
Existing layouts for material screening exhibit electrical contacts connected in pairs. A simple two point measurement can be used to check if all contacts are connected. Some designs feature two nested daisy chains. In this configuration a voltage between neighboring contacts can be applied to trigger whisker growth and detect shorts.
Customized wafers with bond frames fabricated by etching or galvanic deposition are well suited for process developments in wafer level packaging applications. Based on ISITs MEMS technology many materials can be used, e.g. aluminum, germanium, gold, copper, or tin. Even chemical nickel gold (ENIG) can be deposited selectively on wafers with aluminum pads.

Glass Wafer

Glass wafers with precise alignment marks and Vernier structures are often used to determine placement accuracy by visual inspection. Typical use cases are calibration marks for camera systems and placement accuracy verification of die placing equipment to demonstrate machine capability during fairs and custom handover.
In addition to custom specific designs, Fraunhofer ISIT offers two standard layouts, each consisting of a chip and a substrate wafer.

Multiplexing electronic for automated measurement





Glass Wafer

Test Substrates

Fraunhofer ISITs wafer portfolio is complemented by corresponding FR4 substrates. Each substrate contains 24 chip positions divided in three groups. Chips can be placed either on the front or back side of the substrate depending on the desired pad configuration. The "FC 475 DDC" test board for example, features contacts for flip-chip connections on the front side and wire bonding on the back side.
Each chip position is surrounded by measurement pads, enabling easy continuity checks. In case of faults, the defective chip area can be located.
Detailed measurements of the electrical connections can be performed in manual standalone mode or in combination with a computerized measurement card with the measurement board developed by Fraunhofer ISIT. A graphic user interface is used to visualize the measurement results.

Our Service

Fraunhofer ISIT offers customized wafer designs as well as standard designs for typical applications including corresponding FR4 substrates and measurement boards. Test wafers manufactured by Fraunhofer ISIT are 200mm in diameter. They are produced on industrial production equipment in our in-house clean rooms. Usually, they are delivered as undiced wafers or diced on tape. Fraunhofer ISIT does not sell single chips.

Fraunhofer ISIT
is participant of the
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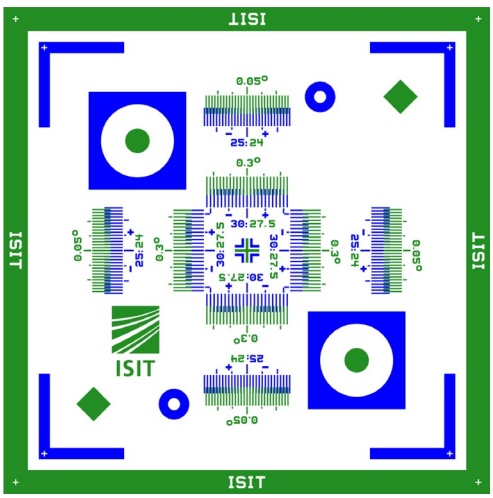
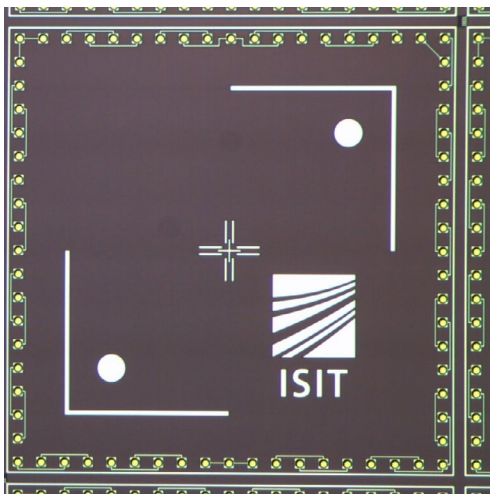
Vernier structure



Daisy chain test structure



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