Fraunhofer ISIT

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Cleanroom Technology Portfolio

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Lithography

- i-line stepper with CD 0.8 & 0.35 µm
  (Canon FPA-3000iW & FPA-3030i5, incl. bottom-side & infrared alignment)
- Mask aligner with CD 1.2 µm
  (SÜSS MA200 Compact, incl. bottom-side alignment)
- Resists thicknesses from 1.2 µm up to 80 µm
- Spray and spin coater (SÜSS ACS200 PLUS, SVG90 S)
- Lift-off processes established for etch free structuring

Deposition

CVD:
- LPCVD: SiN, HTO, TEOS, aSi, polySi (n-doped (PH3) / n.i.d.)
  (ASM 400, ASM A400 DUO)
- PECVD: SiO, SiN, SiON, aSi (n.i.d., n- or p-doped), TEOS
  (Centura DXZ-PECVD)

PVD:
- MSD:
  - Ti, Cu, Cr, WTi, Au, TiN (Evatec LLS EVO2)
  - Ti/TiN/TiO, Pt, AlCu, AlN, AlScN, Mo (Evatec Clusterline 200)
- e-beam evaporation: Ti, Ta, Al, Ni, Ag, Pt, Au, Ir, Ge (Evatec BAK760)

ALD
- Thermal, RPE, O3: SiN, SiO, TiN, TiO, AlO, HfO (Picosun R-200)
- Thermal: AlO, TiO, TiN (Beneq TFS 200)

Epitaxy:
- Silicon (p- or n-doped), thick polysilicon (EpiPoly) (ASM Epsilon 2000)

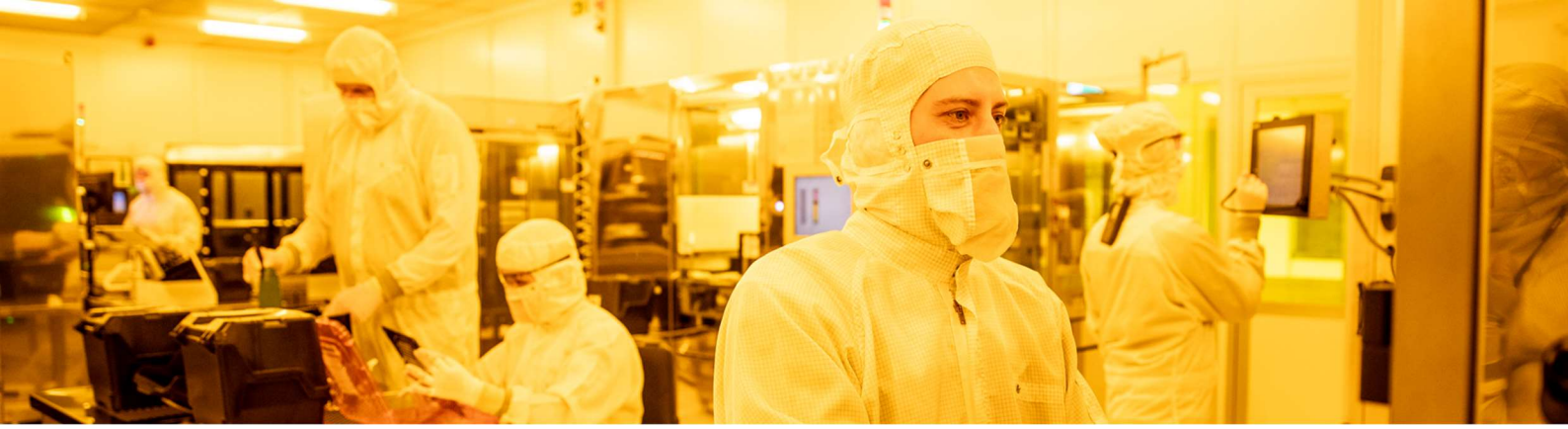
Plating:
- Electro: Cu, Ni, Au, Sn (Semsysco Triton)

Polymer coater:
- Parylene (PPS Parylene Coater)

Metrology

Material science:
- Cleanroom: Reflectometry, ResMap, optical inspection, wafer geometry gauge, white light interferometry, mechanical profilometer, optical profilometer, CDSEM, particle scan
- Lab: AFM, XRD, XRR, Optical Inspection, SEM, X-Ray, XRF, laser microscopy, 2D / 3D Xray tomography

Electric:
- Various (semi-)automatic wafer probers
- Surface insulation resistance: (HV)SIR test: 80 channels up to 100/1000V, max. 100µA
- Blocking test up to 200 channels 120V
- Electrical load change tests (2000A)
- Sample current max 6.5kV / 2000A
- Combined and automated tests (electrical-thermal-mechanical)
- Environmental tests (-70-180°C, 10-98%rH) and thermal stress in different atmospheres up to 1300°C
- Double pulse and UIS test benches



Etching, cleaning and diffusion

Dry
- Dielectric Etch: Si, SiN, SiO, SiON (Applied Materials P5000)
- Metal etch: Al, AlCu, AlN, AlScN, Ti, TiN, Ta, Mo, GaN (Applied Materials Centura Metal Etch)
- Hard material etch: Ta, Pt, SiO, AlScN (STS APS)
- Silicon DRIE (SPTS Pegasus, Lam TCP 9400)

Wet
- Wet Bench: SiO, SiN, glass, Al, AlN, AlScN, AlCu, Mo, Cr, Cu, GaN, Si (KOH / TMAH), Ti, TiN
- Spin Etch: Au, WTi, Ag, Ti, TiN, Cu
- Clean: DSP, HVS, RCA, SC1, SC2, Piranha, dil. HF
- Resist Removal and lift off

Diffusion
- Anneal: 200-1150°C, 30Pa to ATM, O_2,N_2, N_2O, NH_4, 3%H in Ar (Koyo VF-1000LP)
- RTP: 400-1100°C, O_2, N_2, N_2O, NH_4, 3%H in Ar (Mattson 2800)
- Laser anneal: Rofin mWL 200/300t wafer annealer, currently in CMOS FEOL, relocation in 2025 to lab for Post-CMOS

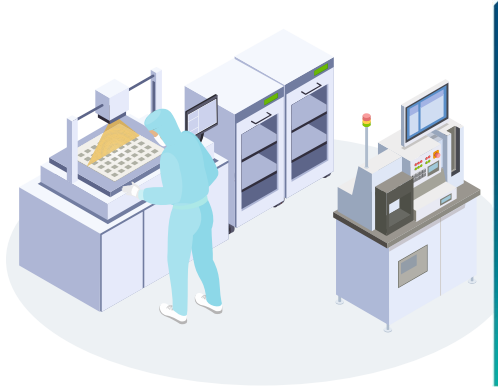
** Implant available via external partner*

Grinding, dicing and polishing

Grinding
- Currently Si & glass (Disco DFG 8540)
- Soon also SiC / AlN

Dicing
- Semi- and fully-automatic blade dicing (Disco DAD3350, DFD6340 & 6240)
- IR alignment, US supported dicing, circle cut

CMP
- CMOS FEOL track (Ebara FREX200)
- Si, SiO, GaN track (metal contaminated) (Ebara FREX200)
- Si, SiO, SiC, GaN track (metal contaminated) (Peter Wolters PM200)



Bonding and WLP

Bonding
- Anodic & fusion: SiO, Au, glass frit (SÜSS SB8e)
- Temporary: resist based, currently being relocated from FEOL to Post-CMOS
- Eutectic: AuSi (SÜSS SB 8e)
- Multi-chip die bonder (Datacon apm 2200, Dr. Tresky T3002-M)

WLP
- Bumping and balling (no HVM), NiAu contacts, ball sizes down to 200µm, pitch down to 400µm, also usable for TAIKO wafer down to 30µm thickness
- Glass / Si cap wafers

Fraunhofer ISIT

Development and production at one location

Institute brief

Fraunhofer ISIT develops and manufactures customer-specific components for power electronics and microsystems technology. It covers the entire value chain from process and device simulation, process development and manufacturing to WLP and characterization. Local and external industrial partners offer the potential for commercialization. Important areas of application are energy and automotive technology, the consumer goods industry, medical technology, communication and automation technology.

Fraunhofer ISIT operates two cleanrooms: An industrial 8″ MOS and PowerMOS front-end (2500 m²) and a separate 8″ MEMS, III-V and BEOL packaging clean room (1000 m²). The capabilities of the latter are illustrated in this portfolio. Additionally, laboratories with an area of 1500 m² are maintained for electrical and mechanical characterization of devices, packaging and interconnect technology as well as for reliability investigations.

Within the FMD, Fraunhofer ISIT is the main location for 8″ post-CMOS technologies, non-CMOS-compatible MEMS and GaN-on-X processing. The latter is specialized in the development of GaN sensor chiplets and advanced membrane transistors as well as the processing of emerging ceramic substrates. Due to its wide ensemble of available post-CMOS materials, Fraunhofer ISIT is well known for the processing of functional materials, e.g., getter, magnetic, piezo- or ferroelectric, for the integration on CMOS chips or active interposers.

Contact and further information

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Info sheet

Virtual clean room tour

Fraunhofer ISIT is member of

Forschungsfabrik Mikroelektronik Deutschland

ECPE

LE.SH Netzwerk Leistungselektronik Schleswig Holstein

Insight of virtual 3D tour app from ballroom and adjacent areas of ISIT's Post-CMOS cleanroom containing:
lithography and metrology
deposition, etch & diffusion
wet chemistry, electroplating and bonding
glass processing
dicing and grinding
fabin