

GaN Technologies

From Planar to Vertical: Custom Solutions for Advanced GaN-based Devices

Fraunhofer Institute for Silicon Technology ISIT

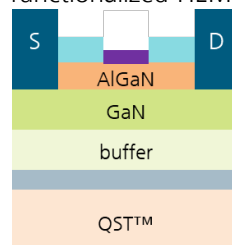
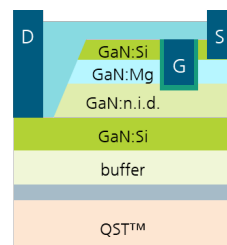
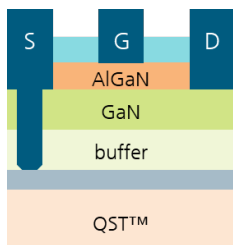
Fraunhofer ISIT has a proven background in application specific Si-based PowerMOS transistors, IGBTs and diodes with blocking capabilities up to 1200V. In 2017 we introduced the first GaN processes and equipment and started to develop our own GaN processes and device designs.

For the manufacturing of these we are utilizing our 1000 m² Post-CMOS fab in Itzehoe, Germany, that offers a unique combination of process capabilities and materials to unveil the potential of your GaN designs. Starting point are most commonly commercial 8" GaN-on-Si and GaN-on-QST substrates with customizable epitaxies based on your device requirements.

In cooperation with APECS-partners, we can offer additional services, ranging from WLP to custom inverter design and application development.

Upcoming MPW-runs and (co-)development opportunities

- Power HEMTs (d-mode, 650V)
- quasi-vertical GaN (trenchMOS, 200V)
- GaN sensors based on open-gated and functionalized HEMTs

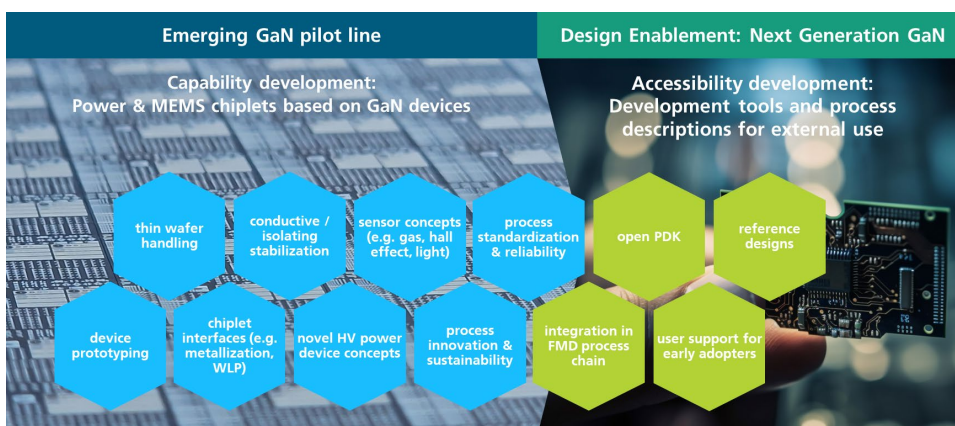
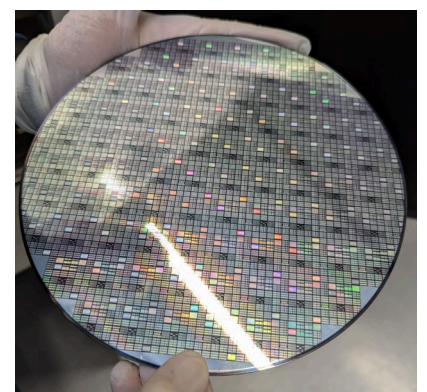
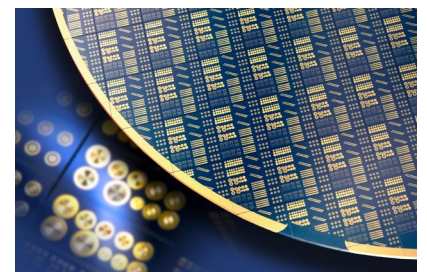


Your input:

- Let us know what devices you would like to realize and or what process sequences you would like to evaluate
- Contribute with your device design and or your wafer material
- Tell us what you require to develop your devices in our fab

Your benefit:

- Significantly reduced costs during MPW setup phase at Fraunhofer ISIT
- Explore processes or device concepts before adapting it in your fab
- Get hands on experience with GaN developers at Fraunhofer and its partners

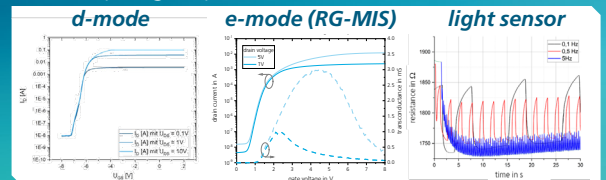
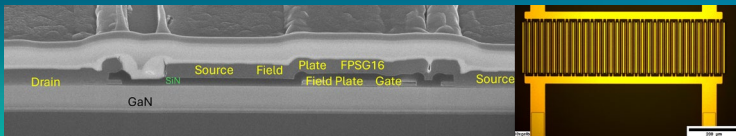


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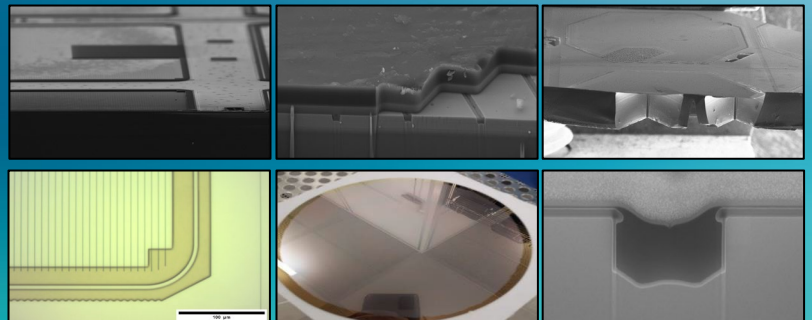
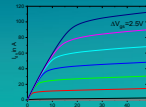
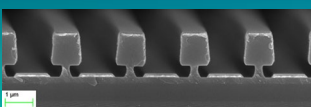
HEMT technologies

- Substrates: 8" GaN-on-Si or GaN-on-QST typ. 200V/650V
- d-mode, e-mode (pGaN from 2026e)
- Device isolation: MESA etch or N implant
- Gate implementation: Schottky, MIS, recess
- Ohm contact: TiAlNiAu or TiAl(Cu)
- Typ. device sizes: single finger up to $\sim 3 \times 3 \text{ mm}^2$
- Sensor concepts: gas, photo, hall effect



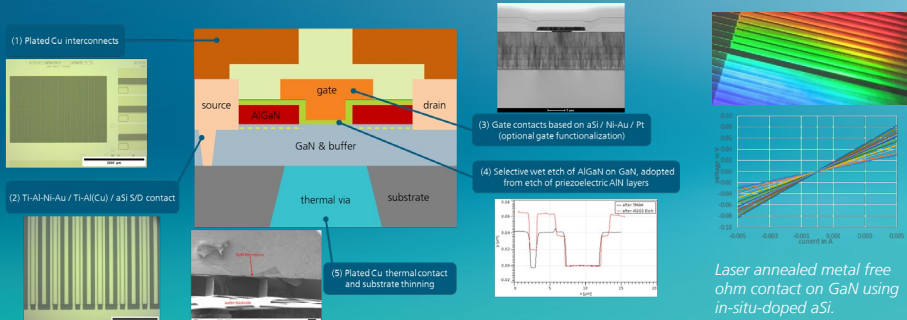
(quasi-)vertical GaN technologies

- Diodes and transistors in development
- Substrates: 8" GaN-on-QST, $\sim 12 \mu\text{m}$ GaN epi
- Gate implementation: trench MOS, e-mode
- Device termination: MESA and field-plates
- Typ. device sizes: $\sim 2 \times 2$ up to $\sim 4 \times 4 \text{ mm}^2$
- Expected Specs for 2025: 48 V, $>40 \text{ A}$ ($>600 \text{ V} / 100 \text{ A}$ in parallel development)



Process technologies

- Post-CMOS process environment
- 0.35 & 0.8 μm process nodes
- Extensive metallization capabilities
- Custom lift-off processes
- Laser anneal for metal free contacts
- Custom QST substrate processes
- Extensive CMP and Cu plating capabilities



TCAD simulation service and compact model development

- DTCO using TCAD process and device simulations
- Creation and optimization of behavioral models for system design
- Implementation of degradation mechanisms in behavioral models

Available tools based on Silvaco:

- 2D/3D process and device simulation
- Electrothermal and mixed-mode simulations
- Parasitic extraction and interconnect optimization
- Spice model generation and circuit simulation

