**PRODUCT DATA SHEET**

**Silicon Wire Bond Test Wafer WB200 8”**

**LAYOUT:**

![Diagram of LAYOUT](image)

**TECHNICAL DATA:**

- Wire Bond Silicon Die
- dummy component with connected aluminium wire bond pads
  - contact pitch: 20µm, 25µm, 30µm, 35µm, 40µm, 45µm, 50µm, and 80µm
  - square pad size: 17µm, 22µm, 27µm, 31µm, 36µm, 40µm, 45µm, and 69µm
- fiducial marks for automated placement
- design size 2.00 mm x 2.00 mm with 120 µm dicing street
- optional passivation available on request
- custom specific wafer thickness
TECHNICAL INFORMATION:

designed chip size  
2.00 mm x 2.00 mm

die pitch  
2.12 mm x 2.12 mm

typical die size after dicing  
2.07 mm x 2.07 mm

other geometries, e.g. 4x4 dies available on request

wafer thickness  
250µm, other thicknesses available on request

pad layout  
276 pads 20µm pitch, 220 pads 25µm pitch, 180 pads 30µm pitch, 156 pads 35µm pitch, 132 pads 40µm pitch, 108 pads 45µm pitch, 84 pads 50µm pitch, 44 pads 80µm pitch, all pads connected

pad geometry  
square geometry with pitch dependent side length: 17µm, 22µm, 27µm, 31µm, 36µm, 40µm, 45µm, and 69µm

pad metal  
1.4 µm AlCu0.5

passivation  
optional on request: 1000 nm PSG (alternatives available)

delivery  
8" wafer, ~6400 dies, diced on tape

normal uses  
High throughput die placing from wafer feeder, automatic wire bonding, encapsulation processes.

typical technologies  
• wire bonding
• stud-bump bonding

available substrates  
Substrates may be designed on request

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gallery variations  
Arbitrary customer-specific layouts including a company’s logotype can be realised on 8” glass and silicon wafers.

* Specifications subject to change without notice.