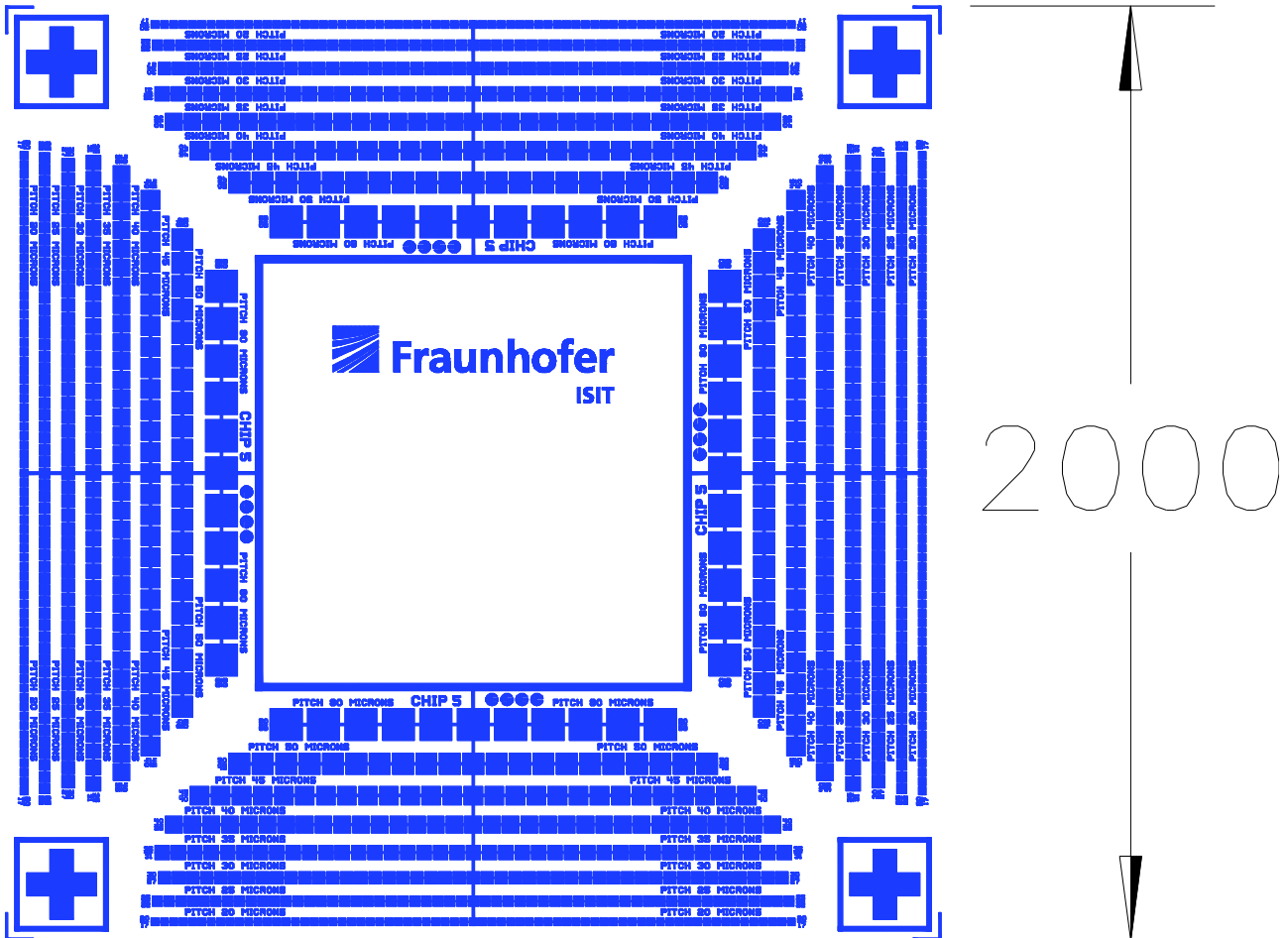

	PRODUCT DATA SHEET	page: 1 of 2
	Silicon Wire Bond Test Wafer WB200 8"	last update 20.02.2017

**LAYOUT:**



**TECHNICAL DATA:**

- Wire Bond Silicon Die
- dummy component with connected aluminium wire bond pads
  - contact pitch: 20µm, 25µm, 30µm, 35µm, 40µm, 45µm, 50µm, and 80µm
  - square pad size: 17µm, 22µm, 27µm, 31µm, 36µm, 40µm, 45µm, and 69µm
- fiducial marks for automated placement
- design size 2.00 mm x 2.00 mm with 120 µm dicing street
- optional passivation available on request
- custom specific wafer thickness

	PRODUCT DATA SHEET	page: 2 of 2
	Silicon Wire Bond Test Wafer WB200 8"	last update 20.02.2017

**TECHNICAL INFORMATION:**

<b>designed chip size</b>	2.00 mm x 2.00 mm
<b>die pitch</b>	2.12 mm x 2.12 mm
<b>typical die size after dicing</b>	2.07 mm x 2.07 mm other geometries, e.g. 4x4 dies available on request
<b>wafer thickness</b>	250µm, other thicknesses available on request
<b>pad layout</b>	276 pads 20µm pitch, 220 pads 25µm pitch, 180 pads 30µm pitch, 156 pads 35µm pitch, 132 pads 40µm pitch, 108 pads 45µm pitch, 84 pads 50µm pitch, 44 pads 80µm pitch, all pads connected
<b>pad geometry</b>	square geometry with pitch dependent side length: 17µm, 22µm, 27µm, 31µm, 36µm, 40µm, 45µm, and 69µm
<b>pad metal</b>	1.4 µm AlCu0.5*
<b>passivation</b>	optional on request: 1000 nm PSG (alternatives available)
<b>delivery</b>	8" wafer, ~6400 dies, diced on tape
<b>normal uses</b>	High throughput die placing from wafer feeder, automatic wire bonding, encapsulation processes.
<b>typical technologies</b>	<ul style="list-style-type: none"> <li>• wire bonding</li> <li>• stud-bump bonding</li> </ul>
<b>available substrates</b>	Substrates may be designed on request
<b>contact</b>	<p>Fraunhofer Institut Siliziumtechnologie Fraunhoferstraße 1; D-25524 Itzehoe Internet: <a href="http://www.isit.fraunhofer.de">http://www.isit.fraunhofer.de</a></p> <p>Dr.-Ing. Dipl. Phys. Dirk Kähler Phone +49 (0) 48 21 / 17 – 46 04 Fax +49 (0) 48 21 / 17 – 42 50 Email: <a href="mailto:dirk.kaehler@isit.fraunhofer.de">dirk.kaehler@isit.fraunhofer.de</a></p> <p>Dr.-Ing. Wolfgang Reinert Phone +49 (0) 48 21 / 17 – 42 16 Fax +49 (0) 48 21 / 17 – 42 50 Email: <a href="mailto:wolfgang.reinert@isit.fraunhofer.de">wolfgang.reinert@isit.fraunhofer.de</a></p>
<b>geometry variations</b>	Arbitrary customer-specific layouts including a company's logotype can be realised on 8" glass and silicon wafers.

\* Specifications subject to change without notice.