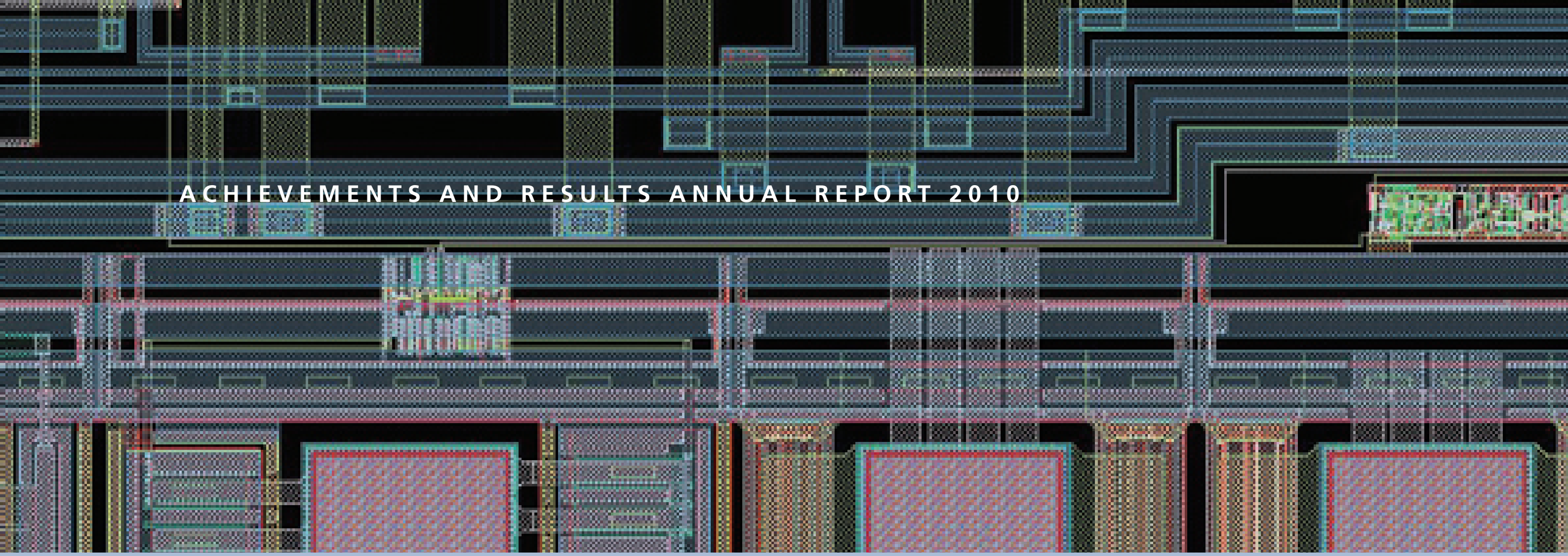
Fraunhofer
ISIT

FRAUNHOFER-INSTITUT FÜR SILIZIUMTECHNOLOGIE ISIT

Achievements and Results
Annual Report
2010

Achievements and Results Annual Report 2010



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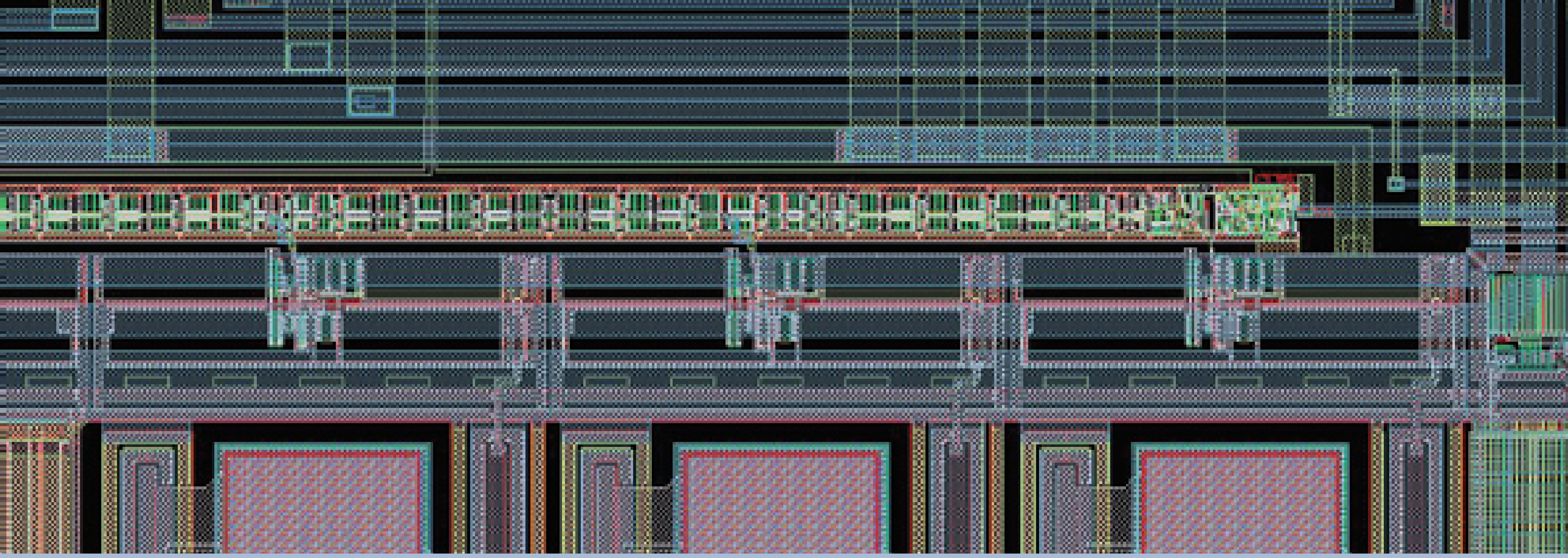

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Festive event on the occasion of start up the new ISIT coating center and settlement of Dispatch Energy Innovations. From left to right: Torge Thönnessen, ISIT, Dr. Günter Schneider, CEO Enolcon, Dr. Gerold Neumann, CTO Dispatch Energy, Prof. Wolfgang Benecke, ISIT, Dr. Andreas Köppen, Mayor of Itzehoe, Dr. Georg Rosenfeld, FhG, Dr. Hans-Martin Henning, ISE, Dietmar Gruidl, CEO Dispatch Energy, Jost de Jager, Minister of Economic Affairs in Schleswig-Holstein

Dear business partners, friends of the ISIT and colleagues,

Fraunhofer ISIT significantly exceeded its set targets, both with regard to the technical advances achieved and the income generated, and the foundations for long-term development of the institute are firmly in place. It is particularly gratifying that industrial revenue increased once again. I would like to take this opportunity to thank all involved for the confidence they have shown in the institute and their constructive support. Thanks are due to our industrial customers, our partners in Fraunhofer-Gesellschaft, the universities, the ministries and funding institutions at state and federal level, project sponsors and the EU, the Executive Board and central administration of the Fraunhofer-Gesellschaft, the institute coordination officer and the members of the Advisory Board. I would also like to acknowledge in particular the exceptional efforts of all our staff, without whom this record of success would not have been possible.

This annual report will provide you with a brief insight into the work of the institute and, we hope, create stimulus for further and future joint R&D projects.

To secure the long-term competitiveness of Fraunhofer ISIT, the 200 mm wafer technology platform was consolidated and expanded in the micro/nanosystems engineering sector. The institute now has one of the most advanced R&D establishments for this technology anywhere in the world. In this connection, the new ISIT Cleanroom II building project continued to make steady progress according to schedule. Approval processes and planning work progressed smoothly and quickly thanks to the vigorous and successful efforts of the parties

Liebe Geschäftpartner, Freunde des ISIT und Kollegen,

das Fraunhofer ISIT konnte seine gesteckten Ziele deutlich übertreffen, sowohl hinsichtlich der erzielten technischen Fortschritte als auch hinsichtlich der Ertragslage und der Weichenstellungen für die langfristige Entwicklung des Hauses. Besonders erfreulich ist, dass die Wirtschaftserträge erneut gesteigert werden konnten. Für das entgegengebrachte Vertrauen und das konstruktive Zusammenwirken möchte ich an dieser Stelle allen Beteiligten danken. Dank gilt unseren industriellen Auftraggebern, den Partnern in der Fraunhofer-Gesellschaft, den Universitäten und Hochschulen, den Ministerien und Förderinstitutionen in Land und Bund, den Projektträgern und der EU und dem Vorstand der Fraunhofer-Gesellschaft mit der Zentralverwaltung, dem Institutsbetreuer und den Kuratoren. Ganz besonders anerkennen möchte ich das außergewöhnliche Engagement aller unserer Mitarbeiterinnen und Mitarbeiter ohne das die erfolgreiche Bilanz nicht zu erreichen gewesen wäre.

Der vorliegende Jahresbericht gibt Ihnen einen kleinen Einblick in die Arbeiten des Hauses und, so hoffen wir, Anregungen für weitere und zukünftige gemeinsame F&E Vorhaben.

Für die langfristige Sicherstellung der Wettbewerbsfähigkeit des ISIT wurde die 200-mm-Wafer-Technologieplattform im Bereich der Mikro- und Nanosystemtechnik weiter konsolidiert und ausgebaut. Das ISIT verfügt damit über eine der international modernsten F&E Einrichtungen auf dem Gebiet. In diesem Zusammenhang konnte der Neubau ‚ISIT Reinraum II' konsequent und im Zeitplan weiter vorangetrieben werden. Für die zügige Durchführung der Bewilligungsverfahren und die Durchführung responsible at state and federal government level and at Fraunhofer-Gesellschaft.

Work on the further development of power electronic systems and components yielded new solutions and concepts. At the Power Electronics Competence Center Schleswig-Holstein (KLSH) innovative converter modules were developed and provided to users for testing and evaluation. New generations of PowerMOS and IGBT components were developed and tested very successfully here at the institute in close cooperation with Vishay. Further modernization and expansion of the Silicon process line

der Planungsarbeiten haben sich die Verantwortlichen im Land, dem Bund und in der Fraunhofer-Gesellschaft sehr konsequent und erfolgreich eingesetzt.

Die Arbeiten zur Weiterentwicklung leistungselektronischer Systeme und Komponenten haben zu neuen Lösungen und Konzepten geführt. Im Rahmen des Kompetenzzentrums Leistungselektronik Schleswig-Holstein KLSH wurden neuartige Umrichtermodule entwickelt und Anwendern für die Erprobung und Evaluation bereitgestellt. Neue Generationen von PowerMOS- und IGBT-Leistungsbauelementen konnten sehr erfolgreich in

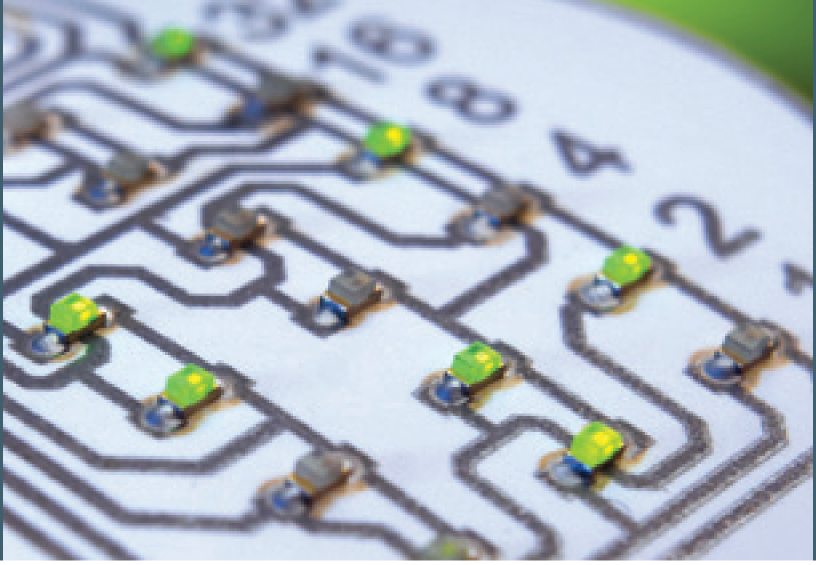
ISIT-Organigramm

on site was a key factor in this success. It is also very gratifying to report that application know-how was strengthened with the creation of a department for this purpose. Work at the ISIT on electrical energy storage systems incorporating lithium-polymer accumulators was significantly expanded, making it possible to take the next step towards taking this technology into production. Of decisive importance in this regard is the procurement of a pilot production unit for foil manufacture, thanks to support received under the federal government's economic stimulus program. Another very pleasing related development was the location of Dispatch Energy Innovations GmbH on site. This company serves markets for decentralized energy storage and supply systems and will cooperate closely with the relevant departments of Fraunhofer ISIT – a constellation that will enable the institute to respond rapidly growing demand for innovative electrical energy storage devices by offering interesting customized solutions.

In microsystems technology, work on piezoelectric films continued very successfully and further strengthened the basis for new classes of piezo MEMS components. Cooperative ventures and projects were established to build on what has been accomplished with inertial sensors and micromirrors in recent years, opening up new applications, such as indoor navigation and image projection (pico beamer). The results achieved are at the leading edge of global developments. Incoming orders at MEMS Foundry Itzehoe GmbH (MFI), and the company's cooperation with Fraunhofer ISIT, have both developed very well. Demand for small and medium-sized production batches of MEMS is growing steadily and confirms MFI's business model, in which the close connection with R&D work at Fraunhofer ISIT

engster Kooperation mit Vishay am Standort entwickelt und erprobt werden. Wichtige Voraussetzung dafür war die weitere und stetige Modernisierung und der Ausbau der Si-Prozesslinie am Standort. Sehr erfreulich ist, dass die Stärkung des Anwendungs-Know-how durch den Aufbau einer entsprechenden Abteilung erfolgen konnte. Die Arbeiten des ISIT zu elektrischen Energiespeichern auf der Basis von Lithium-Polymer-Akkumulatoren wurden deutlich erweitert, dass der nächste Schritt in Richtung der Produktionsreife möglich wurde. Die Beschaffung einer Pilotfertigungsanlage für die Folienherstellung im Rahmen des Konjunkturprogramms der Bundesregierung war dafür entscheidend. Sehr erfreulich ist die in diesem Zusammenhang die Neuansiedlung der Dispatch Energy Innovations GmbH am Standort. Das Unternehmen bedient Märkte für dezentrale Energiespeicher und -versorgungssysteme und wird eng mit den entsprechenden Abteilungen des ISIT zusammenarbeiten. Das rasant wachsende Interesse an innovativen elektrischen Energiespeichern ermöglicht es dem ISIT in dieser Konstellation interessante und kundenspezifische Lösungen anzubieten.

In der Mikrosystemtechnik konnten die Arbeiten zur piezoelektrischen Schichten sehr erfolgreich fortgeführt werden, womit die Basis für neue Klassen von Bauelementen ‚Piezo-MEMS' weiter gefestigt wurde. Aufbauend auf die in den zurückliegenden Jahren durchgeführten Arbeiten zu Inertialsensoren und Mikrospiegeln wurden Kooperationen und Projekte platziert, die neue Anwendungen, wie z. B. Indoor-Navigation oder Bildprojektion (Pico-Beamer) erschließen. Die erzielten Ergebnisse stehen an vorderster Linie auch im globalen/weltweiten Vergleich. Erfreulich entwickelt sich Auftragslage der MEMS Foundry Itzehoe GmbH (MFI) und die Zusammenarbeit mit dem ISIT. Der Bedarf an der Fertigung von MEMS in kleineren und mittleren Stückzahlen wächst ausgeprägt



Detail of a binary clock on paper

gives the company a uniquely competitive standing on the market.

Fraunhofer ISIT has been conducting work on biotechnical microsystems for quite some time now, and consistent development efforts have broadened the basis for these components to enter the market, as reflected in the establishment of POCDIA GmbH (Point-of-Care Diagnostic) in Itzehoe. New applications have been opened up with the participation in projects focusing on cell-free bioproduction.

The activities described have been supported by the Module Integration and IC Design and Simulation departments, which also successfully embarked on their own development projects.

Cooperation with the University of Kiel (Christian-Albrechts-Universität, CAU), and development of the working group at the Faculty of Engineering there, are making gratifying and firm progress. Our involvement in the SFB 855 Magnetoelectric Composites research center is generating interesting impetus for new development projects. We responded with great interest and supported the possibility of participating in the application for a cluster of excellence (Materials for Life) at the CAU.

Fraunhofer ISIT will continue to strengthen and expand those performance attributes that have earned it such high standing in micro/nanosystem technology.
We anticipate that significant advantages for Fraunhofer ISIT can be derived from the institute's unique reputation when competing globally for development projects.
The institute's expertise at system level will also be of major importance in the years ahead. Priority is being given to setting up the requisite working groups and recruiting

und bestätigt das Unternehmensmodell. Die Verbindung mit F&E Leistungen des ISIT verschafft der MFI Alleinstellungsmerkmale.

Biotechnische Mikrosysteme werden bereits seit langem am ISIT entwickelt und untersucht. Auch für diese Bauelemente konnte der Markteintritt durch konsequente Weiterentwicklungen auf eine breitere Basis gestellt werden, was auch mit der Gründung der POCDIA GmbH (Point-of-Care-Diagnostic) in Itzehoe sichtbar wird. Die Erschließung neuer Anwendungen ist mit der Beteiligung an Projekten zur zellfreien Bioproduktion gelungen.

Unterstützt wurden die zuvor genannten Arbeiten durch die Abteilungen für Modulintegration und IC-Design und Simulation, die daneben ebenso erfolgreich in eigene Entwicklungsprojekte eintreten konnten.

Sehr erfreulich entwickelt und festigt sich die Zusammenarbeit mit der Christian-Albrechts-Universität in Kiel und der Aufbau der Arbeitsgruppe an der Technischen Fakultät. Die Teilnahme am SFB 855-Magnetoelektrische Verbundwerkstoffe generiert interessante Impulse für neue Entwicklungsvorhaben. Die Möglichkeit zur Mitwirkung an der Beantragung eines Exzellenz-Clusters an der CAU (Materials for Life) haben wir mit großem Interesse aufgenommen und unterstützt.

Das ISIT wird seine Alleinstellungsmerkmale die in besonderem Maße im Bereich der Mikro- und Nanotechnologie liegen, weiter stärken und ausbauen. Wir erwarten, dass sich hierdurch im globalen Wettbewerb bei der Akquisition von Entwicklungsprojekten signifikant Vorteile für das ISIT darstellen lassen. Auch werden zukünftig die Kompetenzen auf der Systemebene im Hause starke Bedeutung gewinnen. Der Aufbau von entsprechenden Arbeitsgrup-

ISIT's Mangaging Director Prof. Wolfgang Benecke and Holger Pohl, Innovation Consulting at WTSH

personnel to strengthen the institute's expertise in applications development. Attention will focus on applications in the field of power electronics relating to the deployment of renewable energy generation systems, as well as on the use of MEMS in automotive engineering, medical technology and consumer electronics, the further improvement of biosensor systems and the establishment of new fields of work, such as the advancement of printable electronic components on flexible substrates.

Allow me to conclude this review by drawing your attention to the indefatigable and foresighted work of Professor Anton Heuberger for Fraunhofer ISIT. To our great shock and sadness Professor Heuberger died suddenly in February 2011. Without his efforts and commitment the institute, which he directed until 2007, would not exist as it does today at this location. We shall cherish the memory of Professor Heuberger and think of him with gratitude.

Once again I would like to thank all customers and research sponsors for the trust they have placed in Fraunhofer ISIT. The institute possesses an outstanding infrastructure for developing new and innovative systems. We invite you to benefit from the specialized knowledge we have built up over the decades and to make use of the excellent technical facilities we have to offer. We welcome any chance to discuss problems or tasks for which you seek our advice.

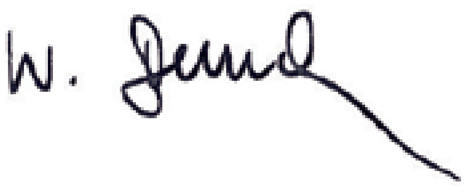
We look forward to working with you again.

pen und die Gewinnung von Personal zur Stärkung des Anwendungs-Know-how wird mit hoher Priorität verfolgt. Anwendungen im Bereich der Leistungselektronik in Verbindung mit der Nutzung regenerativer Energieerzeugungsysteme, der Einsatz von MEMS in der Automobiltechnik, der Medizintechnik und der Konsumelektronik, die weitere Verbesserung biosensorischer Systeme und der Aufbau neuer Arbeitsfelder, beispielsweise für druckbare elektronische Funktionseinheiten auf flexiblen Substraten werden dabei im Vordergrund stehen.

Zum Abschluss dieses Jahresrückblicks möchte ich Ihre Aufmerksamkeit auf das unermüdliche, stetige und vorausschauende Wirken von Herrn Prof. Anton Heuberger für das Fraunhofer ISIT lenken. Herr Prof. Heuberger ist für uns alle überraschend und zu unserer großen Trauer im Februar 2011 verstorben. Ohne sein Engagement würde es das Institut, dessen Leitung er bis zum Jahre 2007 inne hatte, an diesem Standort und in der Ihnen bekannten Ausrichtung nicht geben. Wir werden Herrn Heuberger ein ehrendes, dankbares Andenken bewahren.

Für das entgegengebrachte Vertrauen möchte ich noch einmal allen Kunden und Förderern des ISIT danken. Das Institut ist für die Entwicklung neuer und innovativer Systeme bestens aufgestellt. Nutzen Sie das über Jahrzehnte geschaffene Wissen und die hervorragenden technischen Möglichkeiten. Wir sind jederzeit für Sie ansprechbar, um Problem- und Aufgabenstellungen zu beraten.

Wir freuen uns auf die Zusammenarbeit mit Ihnen.



Fraunhofer ISIT in Itzehoe: lecture halls

FRAUNHOFER-INSTITUT FÜR SILIZIUMTECHNOLOGIE (ISIT)

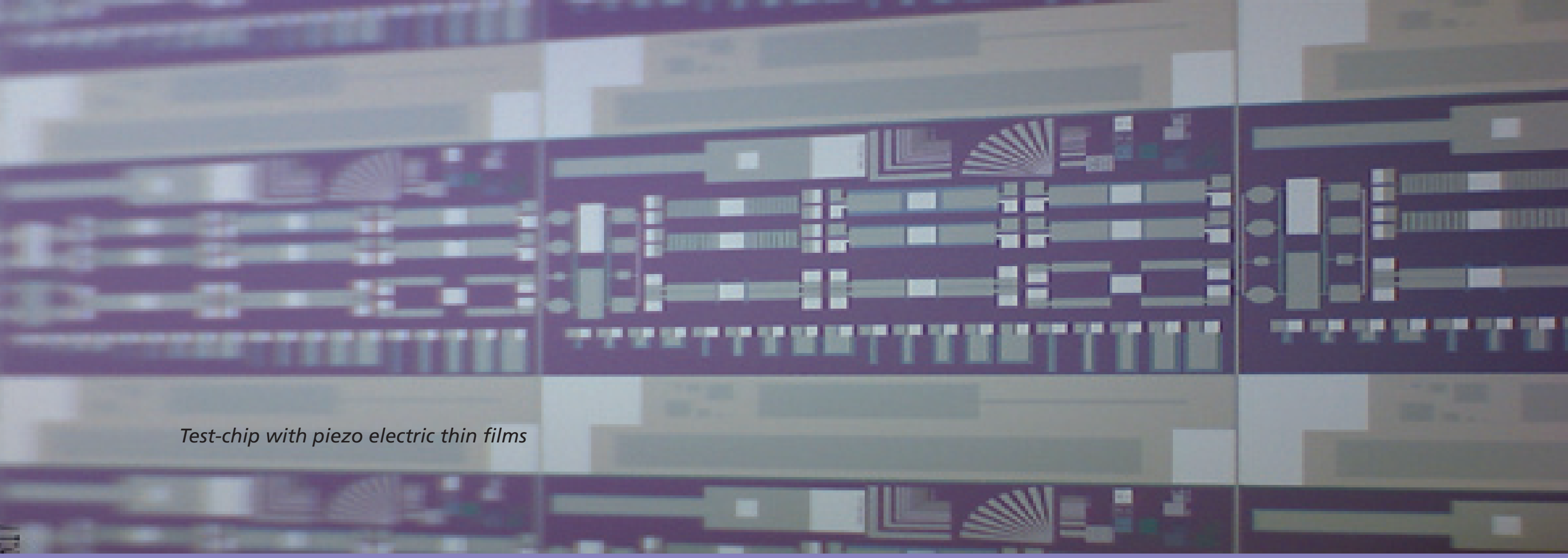
Research and Production at one Location

The Fraunhofer-Institut für Siliziumtechnologie (ISIT) develops and produces microelectronic and microsystem components. The advanced process line based on a 200 mm silicon wafer technology and the expertise built up over decades ensure a world-leading position for ISIT and its customers. Microcomponents for a wide range of applications are developed by the institute. The main areas of application are automotive and transport engineering, consumer goods industry, medical technology, communication systems and automation.

ISIT carries out the design and system simulation of microcomponents for its customers and provides prototypes and pilot production, provision of samples and preparation of series production. The institute also offers application-specific integrated circuits (ASICs) for the operation of sensors and actuators and deals with all the important tasks involved in system integration, assembly and interconnection technology (packaging) and the reliability and quality of components, modules and systems. Activities are completed by intensive development work on electrical energy storage devices based on Lithium polymer batteries.

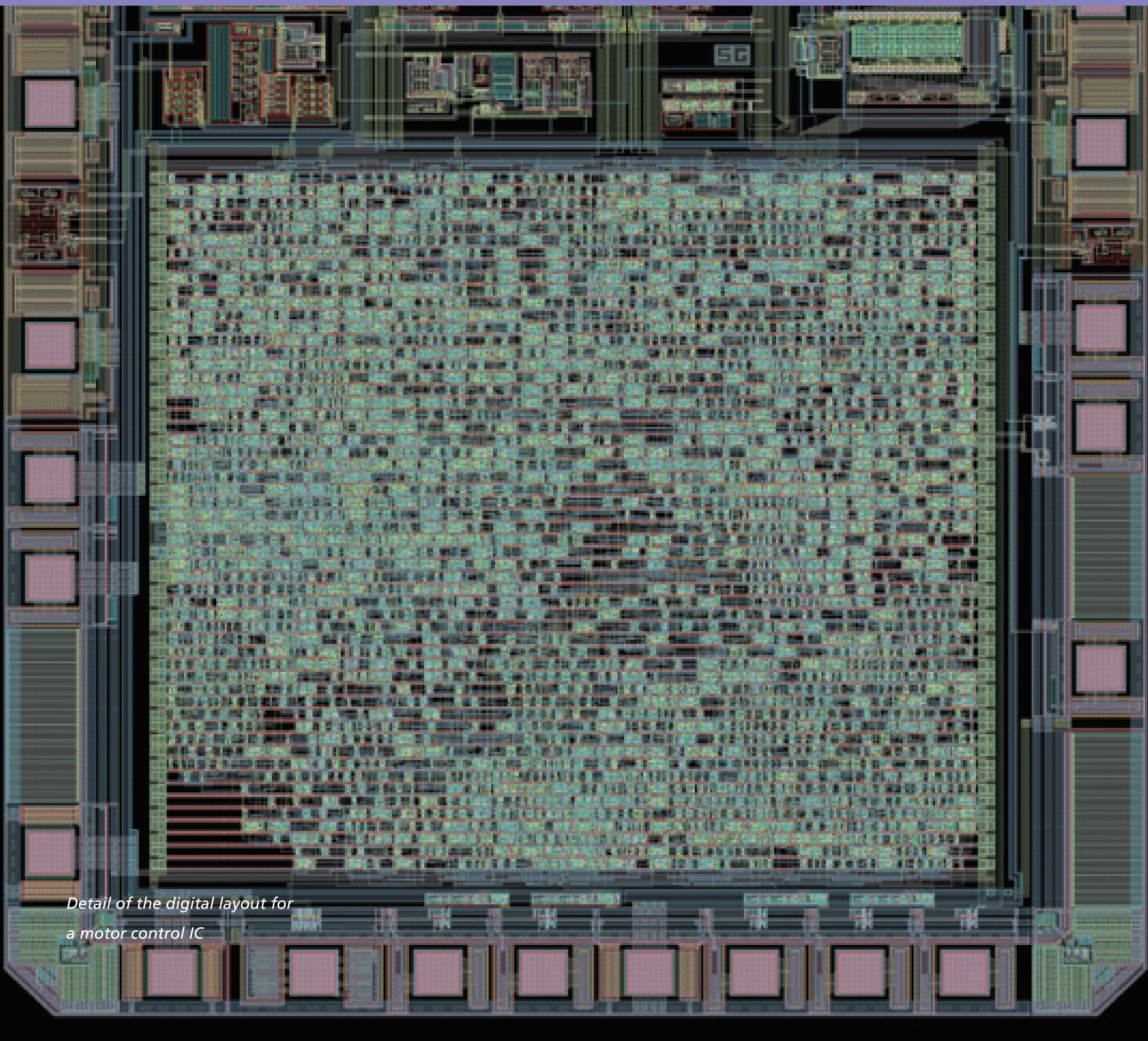
MAIN FIELDS OF ACTIVITY

The new ISIT coating center for electrode foils

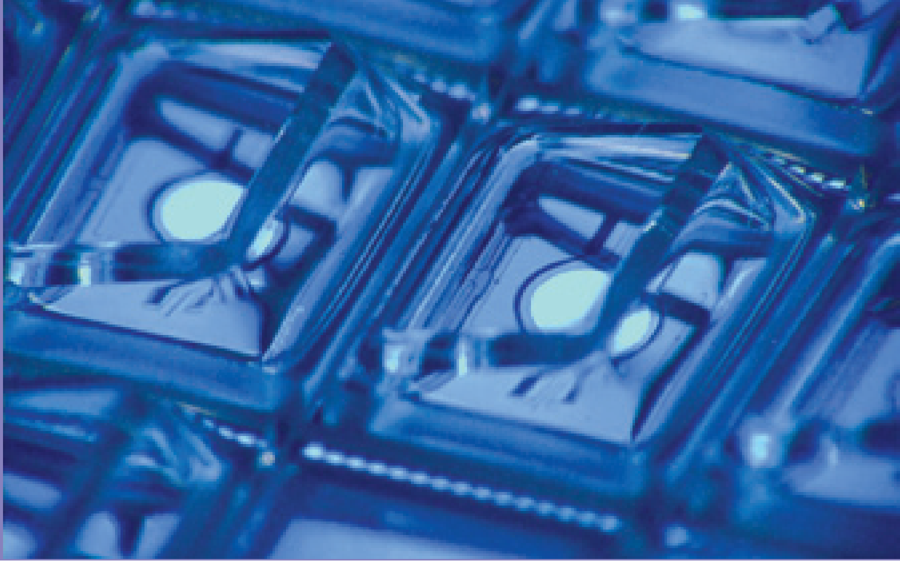


Test-chip with piezo electric thin films

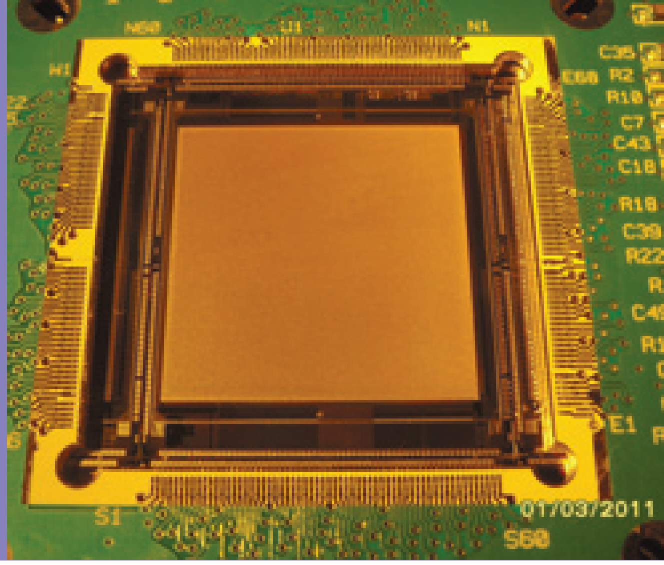
MICROSYSTEMS TECHNOLOGY (MEMS) AND IC DESIGN



Detail of the digital layout for a motor control IC



Vacuum packaged two-axis-scanning micromirrors with inclined optical glass windows



Programmable aperture plate system with 262.000 deflection cells for projection maskless multi e-beam lithography (32 nm-node and beyond)

Research in microsystems technology is a core activity of Fraunhofer ISIT in different departments. For more than 25 years ISIT scientists are working on the development of micro electro mechanical systems (MEMS). This covers the complete spectrum starting from simulation and design, technology and component development up to development of endtest strategies and reliability tests. One of the core competences of the ISIT service offer is the development of integration technologies, like cost effective assembly of several chips in a common package, MEMS packaging on waferlevel (WLP) with defined cavity pressure or a system-on-chip approach. MEMS devices can be combined with a suitable ASIC to miniaturized systems with high functionality.

The ISIT cooperation model allows further to offer also a fabrication of prototypes and starting a pilot production. If high volume MEMS production is requested the on-site operating industrial partner MEMS Foundry Itzehoe (MFI) is able to meet this demand.

ISIT is focussed on MEMS applications in the core areas: physical sensors and actuators, devices and technologies for high frequency application (RF-MEMS), passive and active optical microsystems as well as piezoelectric MEMS.

In the field of sensor systems strong activities are put on inertial sensors (accelerometer, gyrometer, IMUs) and on flow sensors with integrated electronics (ASICs) respectively. Special technological process modules for sensor development are available, e.g. thick poly silicon as a functional layer or hermetic encapsulation on waferlevel.

High frequency microsystems at ISIT are primarily for application in wireless reconfigurable communication networks, in particular developments for RF-MEMS switches, ohmic switches and waferlevel packaging are running.

In the field of optical MEMS devices ISIT is active in the development of micromirrors for laser projection displays, optical scanning systems and light modulators. Passive optical microsystems are also in the portfolio of ISIT, as there are glass lens arrays or aperture systems for laser beam intensity forming.

At ISIT a variety of single process technologies are available. These have been combined to specific qualified MEMS process modules. They work like a tool kit to realize several applications. Special attention is paid to the PSM-X2 process module, which is based on thick polysilicon layer for the fabrication of accelerometers or gyrometers with automotive qualification AEC Q100.

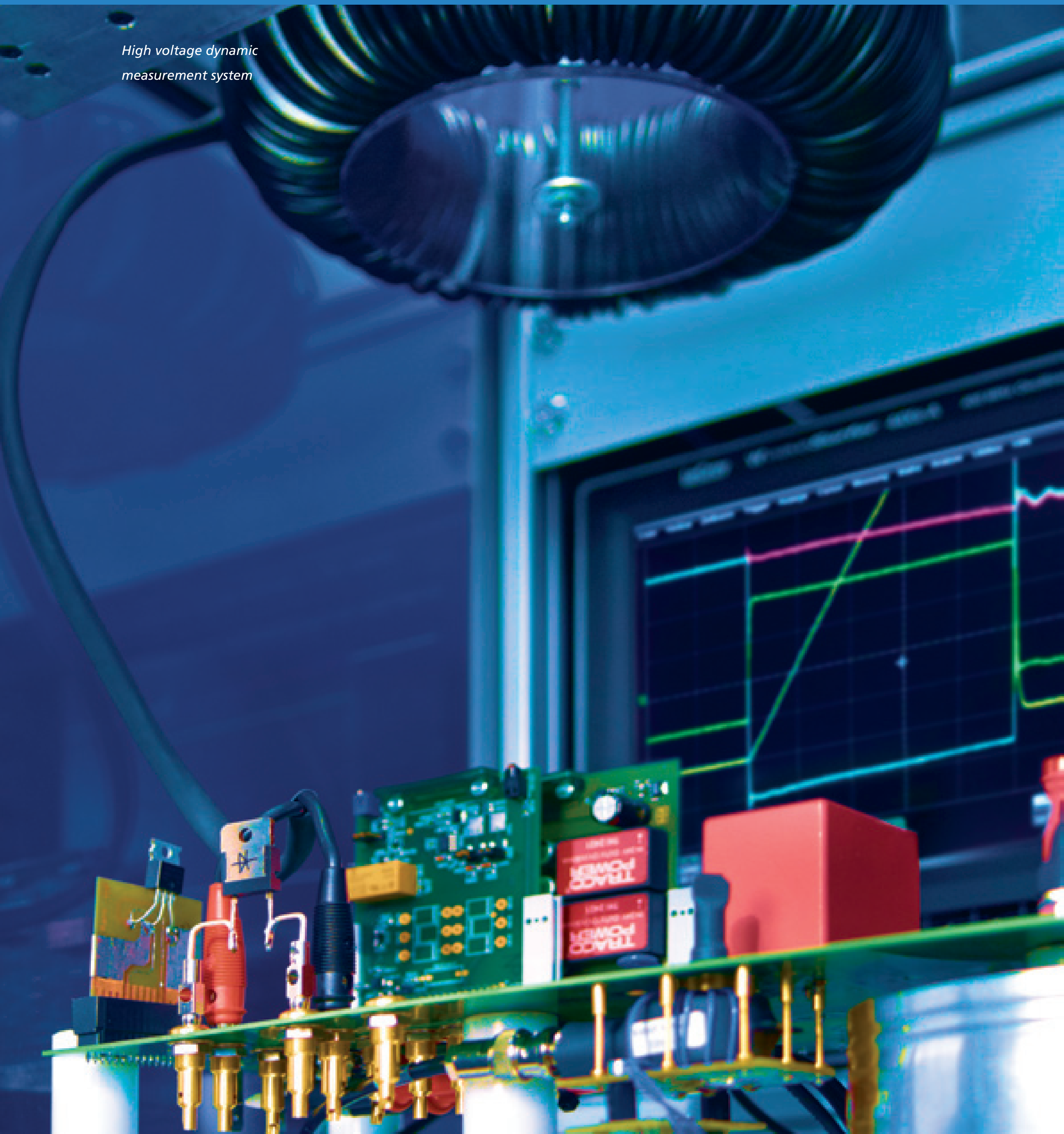
One of the prerequisites for the development of microsystems and microelectronic components is a highly capable integrated circuit design group. The staff at ISIT is specialist in the design of analog/digital circuits, which enable the electronic analysis of signals from silicon sensors. The designers also model micromechanical and micro optic elements and test their functionality in advance using FEM and behavorial modeling simulation tools.

Microsystems Technology
Prof. Bernhard Wagner
+49 (0) 4821 / 17 – 4213
bernhard.wagner@isit.fraunhofer.de

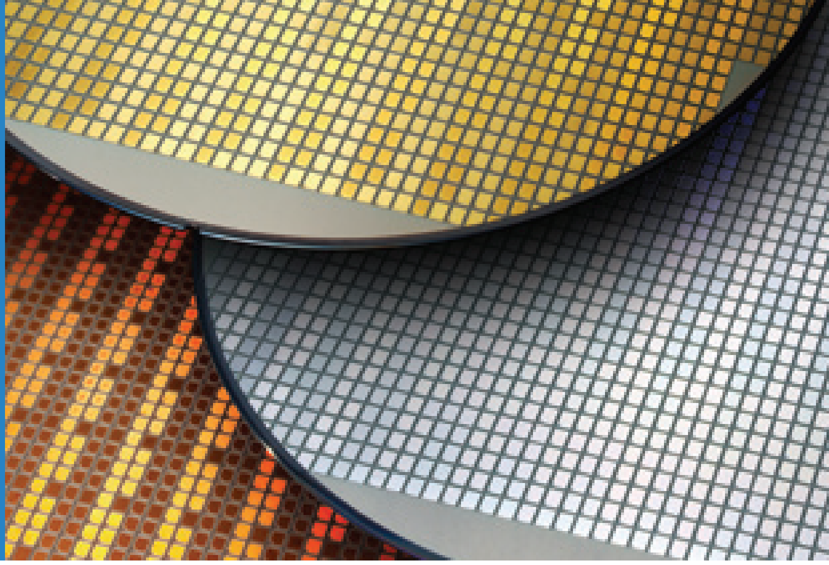
Dr. Klaus Reimer
+49 (0) 4821 / 17 – 4233
klaus.reimer@isit.fraunhofer.de

IC Design
Jörg Eichholz
+49 (0) 4821 / 17 – 4253
joerg.eichholz@isit.fraunhofer.de

MAIN FIELDS OF ACTIVITY



High voltage dynamic measurement system



IGBTs with customer-specific metallization (standard Al, electroless Ni/Au and Cu-metalization) for advanced assembly techniques

IC TECHNOLOGY AND POWER ELECTRONICS

The power electronics and IC technology group develops and manufactures active integrated circuits as well as discrete passive components. Among the active components the emphasis lies on power devices such as smart power chips, IGBTs, PowerMOS circuits and diodes. In this context application specific power devices and new device architectures are special R&D areas. The development of new processes for advanced power device assembly on waferlevel is a further important research topic. It comprises e. g. adapted chip metallization and novel techniques for backside processing of ultra thin Silicon substrates. Additional support is provided by a number of tools for simulation, design and testing. ISIT also benefits from years of experience in the design and manufacturing of CMOS circuits.

Passive components developed and fabricated at ISIT are primarily chip capacitors, precision resistors and inductors. Development of materials and the integration of new materials and alloys into existing manufacturing processes play an important role in the development process. ISIT develops individual processes, process modules and complete process flows for diverse applications. The institute also offers processing of customer-specific silicon components in small to medium-sized quantities on the basis of a qualified semiconductor process technology. In the field of power electronics ISIT coordinates a competence center which was founded in close cooperation with universities and companies of the federal country Schleswig-Holstein. A special R&D group with focus on power electronic systems works on application specific topics covering the interface to system end users.

To support the development of new semiconductor production techniques, production equipment of particular interest is selected for testing and optimization by the ISIT staff. This practice provides the institute with specialized expertise related to e. g. etching, deposition, lithography, and planarization methods. Planarization using chemical-mechanical polishing (CMP) in particular is a key technology for manufacturing advanced integrated circuits and microsystems. The intensive work done by ISIT in this area is supported by a corresponding infrastructure. A special emphasis lies in the application of CMP for the manufacturing of MEMS devices and microsystems.

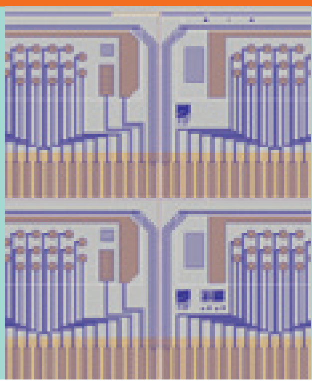
The institute's CMP application lab is equipped with CMP polishing machines and post-CMP cleaning equipment as well as the corresponding measurement tools for wafer diameters between 100 and 300 mm. The CMP group at ISIT works in close relationship to Peter Wolters AG since many years, as well as with other semiconductor equipment manufacturers, producers of polishing slurries and pads, CMP users and chip and wafer manufacturers.

The group's work encompasses the following areas:

- Testing of CMP systems and CMP cleaning equipment
- Development of CMP processes for
  - Dielectrics (SiO_2, TEOS, BPSG, low-k, etc.)
  - Metals (W, Cu, Ni, etc.)
  - Silicon (wafers, poly-Si)
- Testing of slurries and pads for CMP
- Post-CMP cleaning
- CMP-related metrology
- Implementation of customer-specific polishing processes for ICs and micro systems

IC Technology and Power Electronics
Detlef Friedrich
+49 (0) 4821 / 17 -4301
detlef.friedrich@isit.fraunhofer.de

CMP
Dr. Gerfried Zwicker
+49 (0) 4821 / 17 -4309
gerfried.zwicker@isit.fraunhofer.de



Silicon based electrical array biochips

Automated analysis system for bio detection

BIOTECHNICAL MICROSYSTEMS

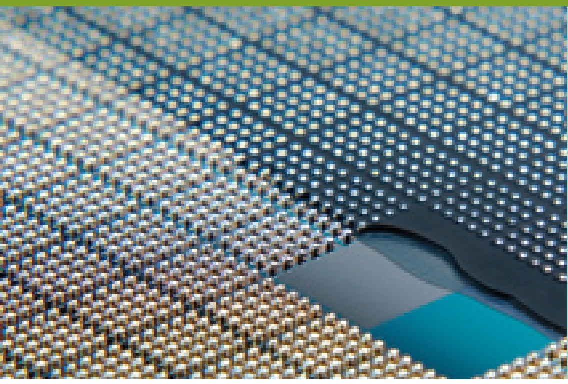
ISIT is one of the worldwide leaders at the field of electrical biochips. These chips allow the realization of very efficient biosensors and are the basis for fast and cost effective analytical systems.

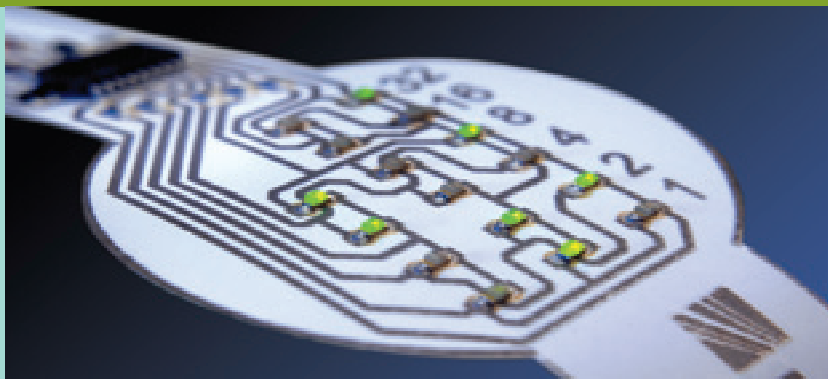
The electrical biochip technology offers intrinsic advantages over optical biochips because of particle tolerance and mechanical robustness by the direct transduction of biochemical reactions into electrical current. The use of gold electrode arrays combined with integrated reference and auxiliary electrodes along with sensitive, selective measurement techniques like "Redox-Cycling" enables powerful sensor systems. These arrays are useful for the detection of a variety of analytes within one probe simultaneously. User-friendly operability is realized by integrating the biochips into cartridges. In combination with micro-fluidic components and integrated electronics, these electrical microarrays represent the basis of rapid and cost-effective analysis systems. They can be used to identify and quantify DNA, RNA and proteins. Further biosensors enable continuous monitoring, e.g. of metabolites as glucose or lactate. The measurement of these substances is realized by enzymatic conversion and electrochemical detection.

The development of additional micro systems for specialized applications involves the production of different kinds of modified electrodes. Supplementary to gold and platinum, diamond electrodes show intrinsic advantages in direct electrochemical detection of substances, e.g. in pulsed amperometry. They are suitable for the detection in chromatography applications (e.g. HPLC) and can be integrated in miniaturized systems like a MEMS chromatography chip.

Miniaturized Iridium oxide electrode chips are used for potentiometric measurements in small volume flow through cells and bio reactors.

Biotechnical Microsystems
Dr. Eric Nebling
+49 (0) 4821 / 17 -4312
eric.nebling@isit.fraunhofer.de





Wafer molding offers new possibilities for low cost packaging

Printed functional structures on paper: binary clock

PACKAGING TECHNOLOGY FOR MICROELECTRONICS AND MICROSYSTEMS

The “Advanced Packaging” group is specialized in detecting and promoting new trends and technologies in electronics packaging. The industrial challenges of tomorrow are addressed in direct collaboration with suppliers of materials, components, modules and equipment. As an example, the automatic pick-and-place assembly of thin dies on flexible substrates was already developed several years ago. For the encapsulation of MEMS components, the glass frit bonding was developed and later on replaced by the more efficient metallic bonding. ISIT equally participates in development activities on organic electronics and RFID technology.

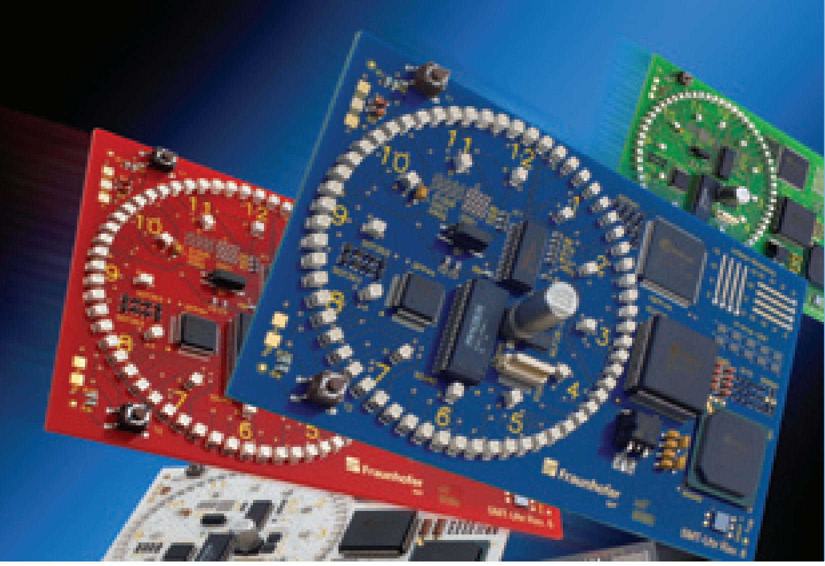
The Fraunhofer ISIT disposes of all basic technologies for the automatic or manual handling of microchips and microsensors, as well as electrical interconnect methods like wire bonding and flip chip technologies.

Through the close relationship between MEMS technology and packaging in ISIT’s premises, the institute has become a leading R&D service provider in the domain of waferlevel-packaging. A cross-disciplinary technology portfolio is now available that allows to reduce cost and volume of a system. Even more, the packaging itself can become a functional part of the microsystem in many cases, e.g. by integrating optical elements or directly interconnecting MEMS and ASIC dies. Outstanding success was achieved in the vacuum encapsulation of micromechanical sensors by eutectic wafer bonding, which paved the way towards the industrialization of a gyro sensor product family for automotive applications.

ISIT continuously expands their assortment of test chips and -substrates that facilitate the ramp up and calibration of production lines for securing quality on a high level.

Packaging Technology for Microelectronics and Microsystems
Karin Pape
+49 (0) 4821 / 17 -4229
karin.pape@isit.fraunhofer.de

Dr. Wolfgang Reinert
+49 (0) 4821 / 17 -4617
wolfgang.reinert@isit.fraunhofer.de



ISIT SMT testboard

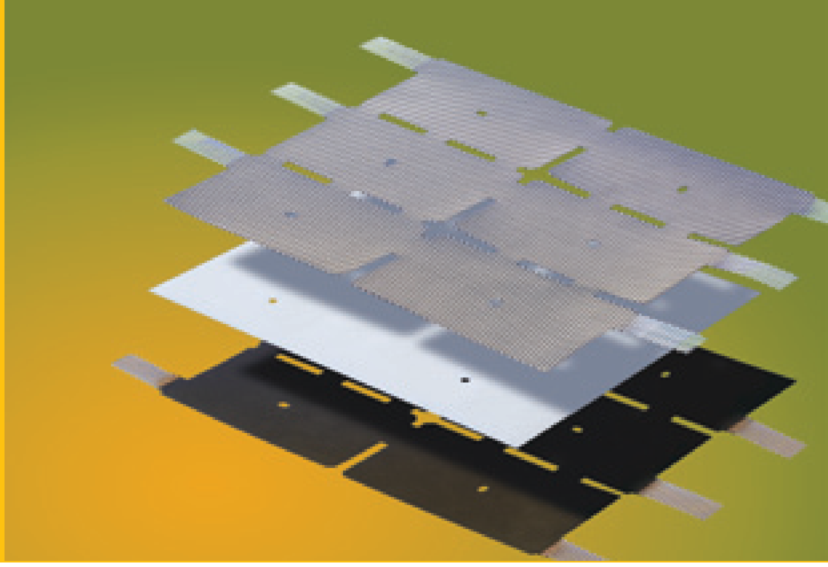
QUALITY AND RELIABILITY OF ELECTRONIC ASSEMBLIES

Quality evaluation – in particular for the soldering work done in pre-production, pilot and main series lots – represents a continuous challenge for ISIT, as for example whenever new technologies such as lead-free soldering are introduced, or when increased error rates are discovered, or if a customer desires to achieve competitive advantages through continual product improvement. To reveal potential weak points, ISIT employs both destructive and non-destructive analysis methods, such as X-ray transmission radiography and scanning acoustic microscopy. Working from a requirements matrix, ISIT scientists also evaluate long-term behavior of lead-free and lead-containing assemblies alike. They then formulate prognoses on the basis of model calculations, environmental and time-lapse load tests, and failure analysis.

In anticipation of a conversion to lead-free electronics manufacturing, Fraunhofer ISIT is undertaking design, material selection and process modification projects for industrial partners. To effect a further optimization of manufacturing processes, the institute applies process models and produces samples on industry-compatible equipment. The group also addresses issues related to thermal management and reliability for customer-specific power modules.

In addition to these technological activities, the group regularly holds training sessions, including multi-day classes, at the institute or at company site.

Quality and Reliability of
Electronic Assemblies
Karin Pape
+49 (0) 4821 / 17 -4229
karin.pape@isit.fraunhofer.de



Electrodes and separator for Lithium Ion batteries

INTEGRATED POWER SYSTEMS

Secondary Lithium batteries as a powerful storage medium for electrical energy are rapidly capturing new fields of application outside of the market of portable electronic equipment.

These new fields include automobiles, medical devices, stationary electric storage units, aerospace, etc. Therefore, this type of rechargeable batteries has to meet a variety of new requirements. This covers not only electrical performance but also design and safety features. The Lithium polymer technology developed at ISIT is characterized by an extensive adaptability to specific application profiles like extended temperature range, high power rating, long shelf and/or cycle life, extended safety requirements, etc. Also included is the development of application-specific housings.

In the Lithium polymer technology all components of the cell from electrodes to housing are made from tapes. At ISIT the complete process chain starting with the slurry preparation over the tape casting process and the assembly and packaging of complete cells in customized designs is available including also the electrical and thermo-mechanical characterization. This allows access to all relevant parameters necessary for an optimization process. The electrode and the electrolyte composition up to the cell design can be modified.

In addition to the development of prototypes, limited-lot manufacturing of optimized cells on a pilot production line at ISIT with storage capacities of up to several ampere-hours is possible. Specific consideration in process development is addressed to the transferability of development results in a subsequent industrial production.

ISIT offers a wide portfolio of services in the field of secondary Lithium batteries:

- Manufacturing and characterization of battery raw materials by half cell as well as full cell testing
- Selection of appropriate combinations of materials and design of cells to fulfil customer requirements
- Application driven housing development
- Test panel
- Prototyping and limited-lot manufacturing of cells

Additional services are:

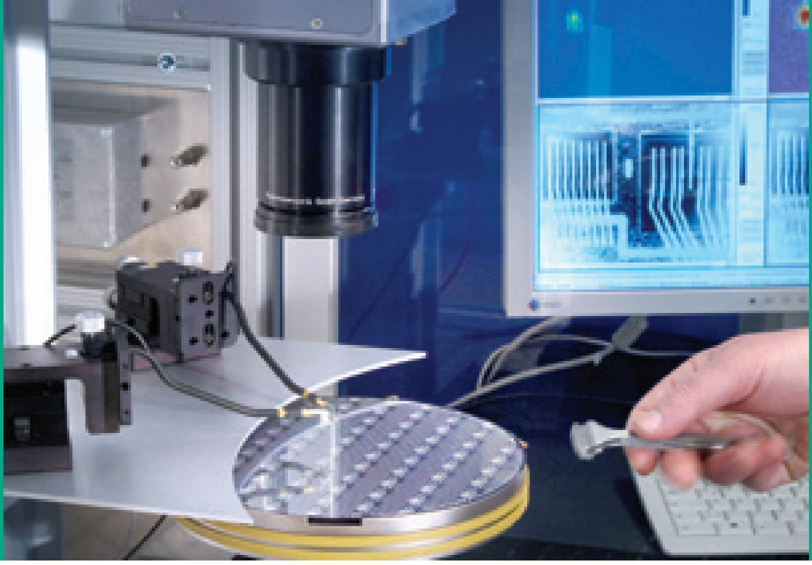
- Preparation of studies
- Failure analysis
- Testing (electrical, mechanical, reliability etc.)
- Technical consultation

Integrated Power Systems
Dr. Peter Gulde
+49 (0) 4821 / 17 -4307
peter.gulde@isit.fraunhofer.de

Dr. Andreas Würsig
+49 (0) 4821 / 17 -4336
andreas.wuersig@isit.fraunhofer.de

OFFERS FOR RESEARCH AND SERVICE

Electrode foil manufacturing at ISIT



Micro lock-in thermography measurement system for defection localization

FACILITIES AND EQUIPMENT

ISIT operates in collaboration with Vishay Siliconix Itzehoe GmbH a semiconductor production line for 200 mm (8") Si wafers (cleanroom area 2.500 m²). The process line is used for the development of new components and processes as well as for the production of components (PowerMOS, MEMS). Further cleanrooms (650 m²) are available for specific processes, as needed for example in microsystem engineering, and for chemical-mechanical polishing (CMP). In addition to the basic processes of microsystem engineering, highly developed processes are maintained, e.g. for high-precision deep etching (DRIE), deposition of non-IC-compatible materials such as piezoelectrics, thick-layer lithography and electroplating, glass molding and grey-scale lithography. The institute has particular expertise in wafer bonding and waferlevel packaging (WLP), achieving unique levels of quality for various MEMS components (gyroscopes, scanner mirrors, RF-MEMS, etc.). Further laboratory areas (1.500 m²) are equipped for characterization, qualification and assembly and interconnection technology. The scope of activities is widened by laboratories for the development of Lithium polymer batteries, in which a pilot production plant is operated for sample production and evaluation tasks. To expand the institute's capacity, a further cleanroom and laboratory building is planned, which is scheduled for completion in mid-2012.
The ISIT's facilities are certified to ISO 9001-2008.

RANGE OF SERVICES

Fraunhofer ISIT has many years of experience in industrial collaboration. Primarily the concept of technology platforms is pursued, i.e. the definition of process procedures in which the customer-specific solutions take place through the design and packaging. This allows to offer services which, beyond the technical specifications, are attractive in terms of risk, development time, development expense and production cost. Series production can ultimately be carried out in close cooperation with the locally based MEMS Foundry Itzehoe GmbH (MFI).

CUSTOMERS

ISIT cooperates with companies of different sectors and sizes. In the following some companies are presented as a reference:

ABB AG, *Ladenburg*

ABB, *Västerås, Sweden*

Ablestik, *Cambridge, England*

Accretech Europe GmbH, *München*

Advaplan, *Espoo, Finland*

AEMtec, *Berlin*

Airbus Operations GmbH, *Buxtehude*

aixACCT Systems GmbH, *Aachen*

Analytik Jena AG, *Jena*

AJ eBiochip GmbH, *Itzehoe / Jena*

Alcatel Vacuum Technology, *Annecy, France*

Andus electronic GmbH, *Berlin*

Applied Materials, ICT, *München*

ASE, *Seoul, Korea*

Atmel Germany GmbH, *Heilbronn*

Atotech Deutschland GmbH, *Berlin*

BASF SE, *Ludwigshafen*

Basler Vision Technologies, *Ahrensburg*

Biont, *Bratislava, Slovakia*

Bruker *Daltonik GmbH, Bremen*

B. Braun Melsungen AG, *Melsungen*

Cleanobil, *Itzehoe*

Condias GmbH, *Itzehoe*

Conti Temic, *Karben*

Conti Temic microelectronic GmbH, *Nürnberg*

DancoTech A/S, *Ballerup, Denmark*

Danfoss Drives, *Graasten, Denmark*

Danfoss Silicon Power GmbH, *Schleswig*

Datacon Technology AG, *Radfeld/Tirol, Austria*

Delong Instruments a.s., *Brno, Czech Republic*

Design und Siebdruck Freudenberg GmbH, *Dresden*

Diehl Avionik Systeme GmbH, *Überlingen*

Dispatch Energy Innovations GmbH, *Itzehoe*

Dow Chemical Company, *Lausanne, Switzerland*

Dräger Systemtechnik, *Lübeck*

E.G.O. Elektro-Gerätebau GmbH, *Oberderdingen*

EADS Deutschland GmbH, *Corporate Research Germany, München and Ulm*

EN Electronic Network, *Bad Hersfeld*

Engineering Center for Power Electronics GmbH, *Nürnberg*

EPCOS, *Nijmegen, Netherlands*

ESCD GmbH, *Brunsbüttel*

ESW-Extel Systems GmbH, *Wedel*

EVGroup, *Schärding, Austria*

Evonik Degussa GmbH, *Hanau*

FeCon GmbH, *Flensburg*

Flextronics, *Althofen*

Freudenberg & Co. KG, *Weinheim*

Fujitsu Siemens Computers GmbH, *Augsburg*

GPS GmbH, *Stuttgart*

Hannusch Industrie-elektronik, *Laichingen*

Harman/Becker Automotive Systems GmbH, *Karlsbad*

Dr. Johannes Heidenhain GmbH, *Traunreut*

Hella KG, *Lippstadt*

Heraeus Holding GmbH, *Hanau*

Honeywell GmbH, *Schönaich*

ID-Systec GmbH, *Neumünster*

Ifm electronic GmbH, *Essen*

IMS Nanofabrication AG, *Wien, Austria*

Jenoptik Innovavent GmbH, *Göttingen*

Jungheinrich AG, *Norderstedt*

Kavlico GmbH, *Minden*

Kristronics GmbH, *Harrislee-Flensburg*

Kuhnke GmbH, *Malente*

Lam Research, *Fremont, USA*

Lenze Drive Systems GmbH, *Hameln*

Liebherr Elektronik GmbH, *Lindau*

Litef GmbH, *Freiburg*

Mair Elektronik GmbH, *Neufahrn*

Marquardt GmbH, *Rietheim-Weilheim*

Meder eletronic AG, *Engen-Welschingen*

MELZER maschinenbau GmbH, *Schwelm*

Prof. Wolfgang Benecke, ISIT's Managing Director, Jost de Jager, Minister of Economic Affairs, and Dietmar Gruidl, CEO of Dispatch Energy at the ISIT festive event „New milestones for battery development in Itzehoe"

MEMS Foundry Itzehoe GmbH, *Itzehoe*

Microelectronics Packaging, *Dresden*

Micronas GmbH, *Freiburg*

Micropelt GmbH, *Freiburg*

MKS, *München*

NU-Tech GmbH, *Neumünster*

NXP Semiconductors Germany GmbH, *Hamburg*

Océ-Technologies B.V., *Venlo, Netherlands*

Oerlikon AG, *Liechtenstein*

Omicron Laserage GmbH, *Rodgau*

Osram Opto Semiconductors GmbH, *Regensburg*

Oticon A/S, *Hellerup, Denmark*

Oy Advaplan Inc., *Espoo, Finland*

PAC Tech, Packaging Technologies, *Santa Clara, USA*

Panasonic, *Neumünster*

Panasonic Electric Works Co. Ltd., *Osaka, Japan*

PAV Card GmbH, *Lütjensee*

Peter Wolters GmbH, *Rendsburg*

PharmedArtis GmbH, *Aachen*

PlanOptik AG, *Elsoff*

Plath Eft GmbH, *Norderstedt*

Preh GmbH, *Neustadt a.d.S.*

Prettl Elektronik Lübeck GmbH, *Lübeck*

Protec Process Systems GmbH, *Siegen*

Raytheon Anschütz GmbH, *Kiel*

Raytrix GmbH, *Kiel*

Rehm Anlagenbau GmbH, *Blaubeuren-Seissen*

Rena Sondermaschinen GmbH, *Gütenbach*

Robert Bosch GmbH, *Reutlingen*

Robert Bosch GmbH, *Salzgitter*

Robert Bosch GmbH, *Stuttgart*

Rutronik Elektrische Bauelemente GmbH, *Ispringen/Pforzheim*

SAES Getters S.p.A., *Lainate/Milan, Italy*

Sartorius Hamburg GmbH Research & Development, *Hamburg*

Sauer, Danfoss, *Nordborg, Denmark*

SEF GmbH, *Scharnebek*

Sensonor Technologies AS, *Horten, Norway*

SensorDynamics (SD) AG, *Lebring, Austria*

Siemens AG, *Erlangen*

SMA Regelsysteme GmbH, *Niestetal*

Smart Material GmbH, *Dresden*

Smyczek, *Verl*

Solar Direct GmbH, *Itzehoe*

Sonion A/S, *Roskilde, Denmark*

Sony Deutschland GmbH, *Stuttgart*

ST Microelectronics, *Crolles, France*

ST Microelectronics Srl, *Milano, Italy*

Still GmbH, *Hamburg*

SÜSS Microtec AG, *Garching*

Technolas GmbH, *München*

Thales, *Paris, France*

Theon, *Athens, Greece*

Treichel Elektronik GmbH, *Springe*

Trinamic, *Hamburg*

Umicore AG & Co., *Hanau*

Vectron International GmbH & Co. KG, *Neckarbischofsheim*

Vishay BCcomponents Beyschlag GmbH, *Heide*

Vishay, *Dimona and Holon, Israel*

Vishay Siliconix Itzehoe GmbH, *Itzehoe*

Vishay Siliconix, *Santa Clara, USA*

Vistec, *Jena*

Volkswagen AG, *Wolfsburg*

Wabco GmbH, *Hannover*

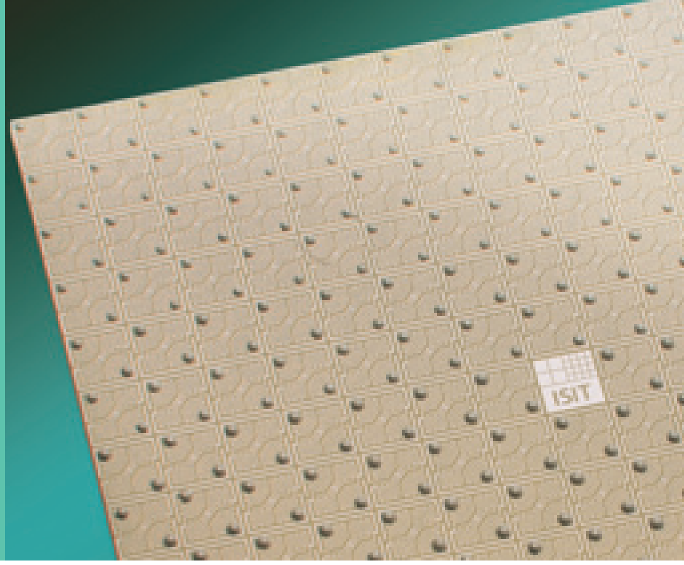
Würth Elektronik GmbH, *Schopfheim*

X-FAB Semiconductor Foundries *AG, Erfurt*

INNOVATION CATALOGUE

ISIT offers its customers various products and services already developed for market introduction. The following table presents a summary of the essential products and services. Beyond that the utilization of patents and licences is included in the service.

Product / Service	Market	Contact Person
Testing of semiconductor manufacturing equipment	*Semiconductor equipment manufacturers*	**Dr. Gerfried Zwicker** + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
Chemical-mechanical polishing (CMP), planarization	*Semiconductor device manufacturers*	**Dr. Gerfried Zwicker** + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
Wafer polishing, single and double side	*Si substrates for device manufacturers*	**Dr. Gerfried Zwicker** + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
IC processes and power devices CMOS, PowerMOS, IGBTs	*Semiconductor industry IC-users*	**Detlef Friedrich** + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Single processes and process module development	*Semiconductor industry semiconductor equipment manufacturers*	**Detlef Friedrich** + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Customer specific processing	*Semiconductor industry semiconductor equipment manufacturers*	**Detlef Friedrich** + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Microsystem products	*Electronic industry*	**Prof. Ralf Dudde** + 49 (0) 4821/17-4212 ralf.dudde@isit.fraunhofer.de
Inertial sensors	*Motorvehicle technology, navigation systems, measurements*	**Dr. Klaus Reimer** + 49 (0) 4821/17-4213 klaus.reimer@isit.fraunhofer.de
Piezoelectric microsystems	*Sensors and actuators*	**Hans-Joachim Quenzer** + 49 (0) 4821/17-4643 hans-joachim.quenzer@isit.fraunhofer.de
Microoptical scanners and projectors	*Biomedical technology, optical measurement industry, telecommunication*	**Ulrich Hofmann** + 49 (0) 4821/17-4553 ulrich.hofmann@isit.fraunhofer.de
Flow sensors	*Automotive, fuel cells*	**Dr. Peter Lange** +49 (0) 4821/17-4506 peter.lange@isit.fraunhofer.de
Microoptical components	*Optical measurement*	**Hans Joachim Quenzer** + 49 (0) 4821/17-4643 hans-joachim.quenzer@isit.fraunhofer.de
RF-MEMS	*Telecommunication*	**Thomas Lisec** + 49 (0) 4821/17-4512 thomas.lisec@isit.fraunhofer.de
Beam deflection components for maskless nanolithography	*Semiconductor equipment manufactorers*	**Dr. Klaus Reimer** + 49 (0) 4821/17-4233 klaus.reimer@isit.fraunhofer.de
Design and test of analogue and mixed-signal ASICs	*Measurement, automatic control industry*	**Jörg Eichholz** + 49 (0) 4821/17-4253 joerg.eichholz@isit.fraunhofer.de



Test die matrix for silver epoxy dispening

Product / Service	Market	Contact Person
Design kits	*MST foundries*	**Jörg Eichholz** *+ 49 (0) 4821/17-4253* *joerg.eichholz@isit.fraunhofer.de*
MST design and behavioural modelling	*Measurement, automatic control industry*	**Jörg Eichholz** *+ 49 (0) 4821/17-4253* *joerg.eichholz@isit.fraunhofer.de*
Electrodeposition of microstructures	*Surface micromachining*	**Martin Witt** *+ 49 (0) 4821/17-4613* *martin.witt@isit.fraunhofer.de*
Electrical biochip technology (proteins, nucleic acids, haptens)	*Biotechnology, related electronics microfluidics, environmental analysis, Si-chipprocessing, packaging, chip loading*	**Dr. Eric Nebling** *+ 49 (0) 4821/17-4312* *eric.nebling@isit.fraunhofer.de*
Microsystem production service	*MEMS fabless manufacturers*	**Dr. Peter Merz** *+ 49 (0) 4821/17-4221* *peter.merz@isit.fraunhofer.de*
Secondary Lithium batteries	*Mobile electronic equipment, medical applications, automotive, smart cards, labels, tags*	**Dr. Peter Gulde** *+49 (0) 4821/17-4307* *peter.gulde@isit.fraunhofer.de*
Battery test service, electrical parameters, climate impact, reliability, quality	*Mobile electronic equipment medical applications, automotive, smart cards, labels, tags*	**Dr. Peter Gulde** *+49 (0) 4821/17-4307* *peter.gulde@isit.fraunhofer.de*
Quality and reliability of electronic assemblies (http://www.isit.fraunhofer.de)	*Microelectronic and power electronic industry*	**Karin Pape** *+ 49 (0) 4821/17-4229* *karin.pape@isit.fraunhofer.de*
Material and damage analysis	*Microelectronic and power electronic industry*	**Dr. Thomas Knieling** *+ 49 (0) 4821/17-4605* *thomas.knieling@isit.fraunhofer.de*
Thermal measurement and simulation	*Microelectronic and power electronic industry*	**Dr. M. H. Poech** *+ 49 (0) 4821/17-4607* *max.poech@isit.fraunhofer.de*
Leadfree / RoHS transformation in electronic assembly	*Electronic industry*	**Helge Schimanski** *+49 (0) 4821/17-4639* *helge.schimanski@isit.fraunhofer.de*
Packaging for microsystems, sensors, multichip modules (http://www.isit.fraunhofer.de)	*Microelectronic, sensoric and medical industry*	**Karin Pape** *+ 49 (0) 4821/17-4229* *karin.pape@isit.fraunhofer.de*
Wafer level packaging, ultra thin Si packaging and direct chip attach techniques	*Microelectronic, sensoric and medical industry, automotive industry*	**Dr. Wolfgang Reinert** *+ 49 (0) 4821/17-4617* *wolfgang.reinert@isit.fraunhofer.de*
Vacuum wafer bonding technology	*Microelectronic, sensoric and medical industry, automotive industry*	*Dr. Wolfgang Reinert* *+ 49 (0) 4821/17-4617* *wolfgang.reinert@isit.fraunhofer.de*

REPRESENTATIVE FIGURES

EXPENDITURE

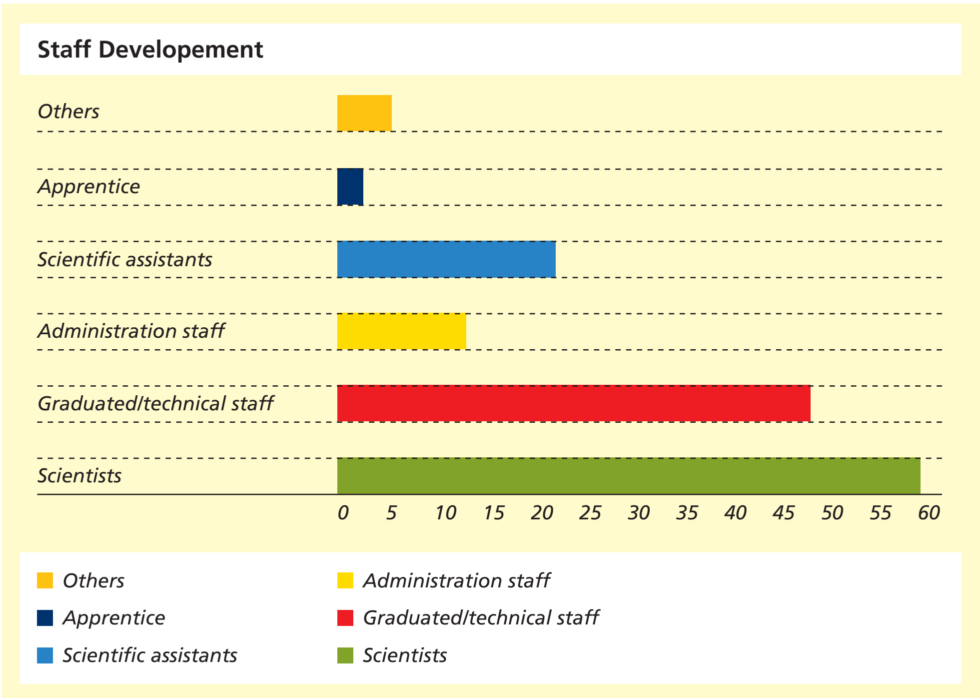
In 2010 the operating expenditure of Fraunhofer ISIT amounted to 20.866,7 T€. Salaries and wages were 8.002,3 T€, material costs and different other running costs were 12.453,4 T€. The institutional budget of capital investment was 411,0 T€.

INCOME

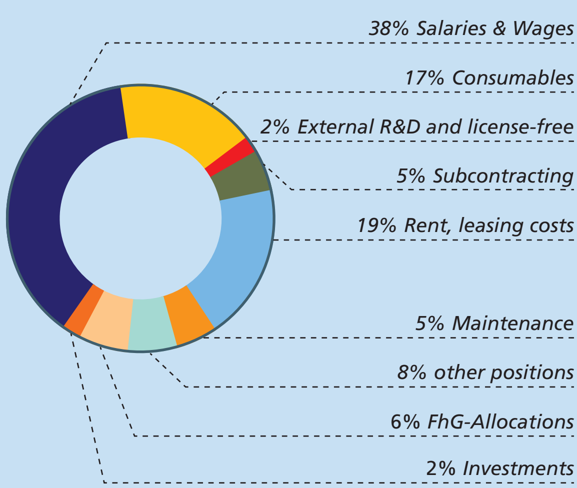
The budget was financed by proceeds of projects of industry/industrial federations/small and medium sized companies amounting to 12.174,0 T€, of government/project sponsors/federal states amounting to 3.189,7 T€ and of European Union/others amounting to 1.140,8 T€. Furthermore there were FhG-projects about 1.102,3 T€ und basic funding with 3.259,9 T€.

STAFF DEVELOPMENT

In 2010, on annual average, the staff consisted of 121 employees. 59 were employed as scientific personnel, 49 as graduated/technical personnel and 13 worked within organisation and administration. The employees were assisted through 22 scientific assistants, 3 apprentices and 5 others.

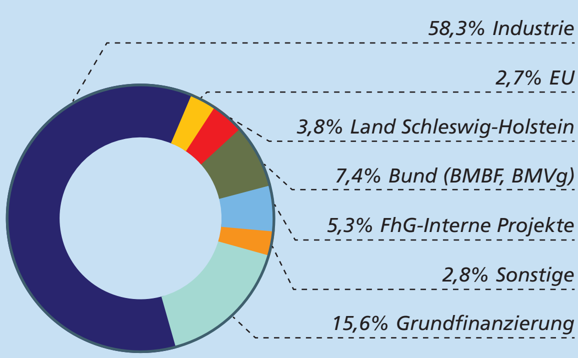


Expenditure



- Salaries & Wages
- Consumables
- External R&D and license-free
- Subcontracting
- Rent, leasing costs
- Maintenance
- other positions
- FhG-Allocations
- Investments

Income



- Industrie
- EU
- Land Schleswig-Holstein
- Bund (BMBF, BMVg)
- FhG-Interne Projekte
- Sonstige
- Grundfinanzierung

THE FRAUNHOFER-GESELLSCHAFT

Research of practical utility lies at the heart of all activities pursued by the Fraunhofer-Gesellschaft. Founded in 1949, the research organization undertakes applied research that drives economic development and serves the wider benefit of society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration.

At present, the Fraunhofer-Gesellschaft maintains more than 80 research units in Germany, including 60 Fraunhofer Institutes. The majority of the more than 17,000 staff are qualified scientists and engineers, who work with an annual research budget of €1.7 billion. Of this sum, more than €1.4 billion is generated through contract research. Two thirds of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. Only one third is contributed by the German federal and Länder governments in the form of base funding, enabling the institutes to work ahead on solutions to problems that will not become acutely relevant to industry and society until five or ten years from now.

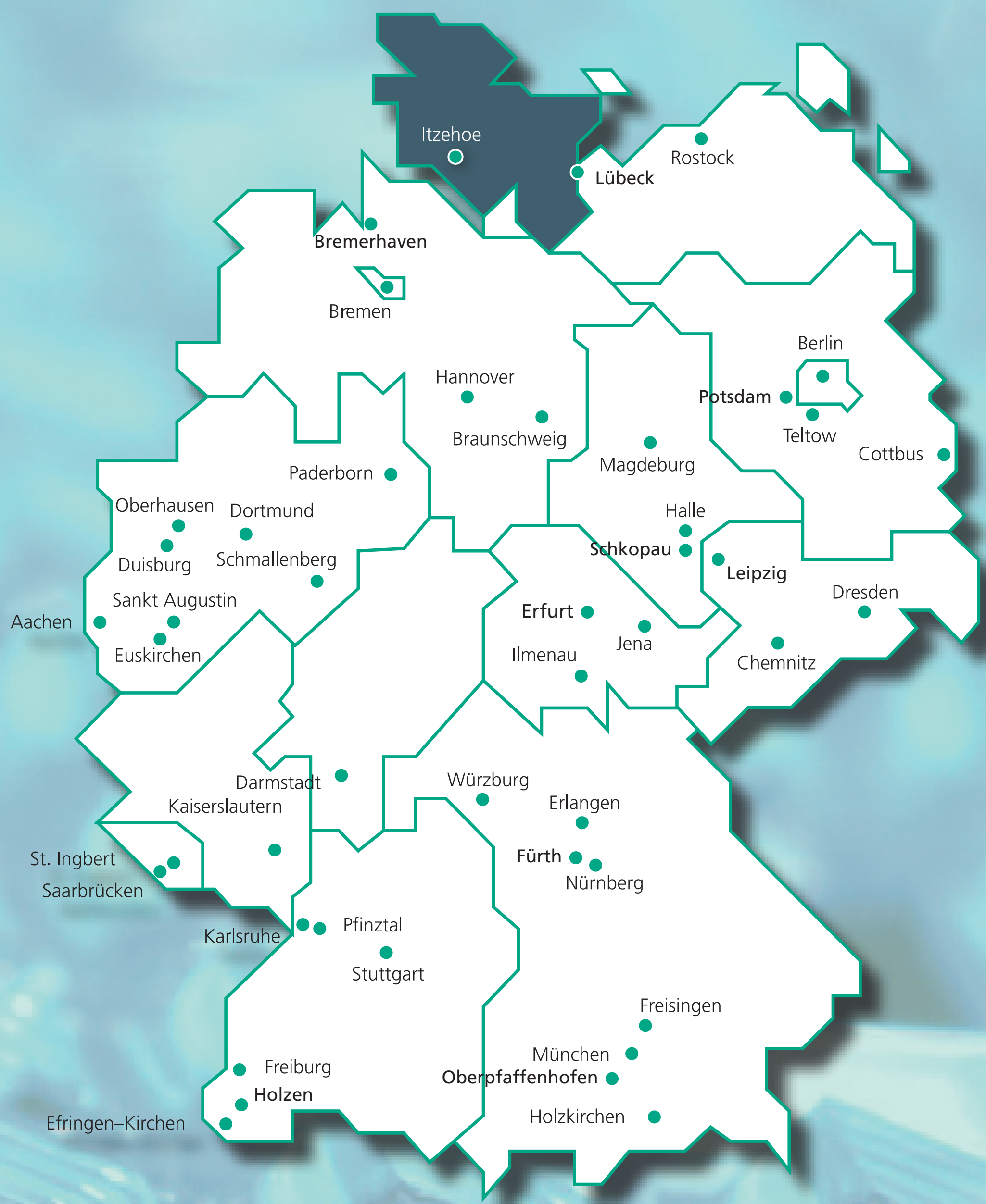
Affiliated international research centers and representative offices provide contact with the regions of greatest importance to present and future scientific progress and economic development.

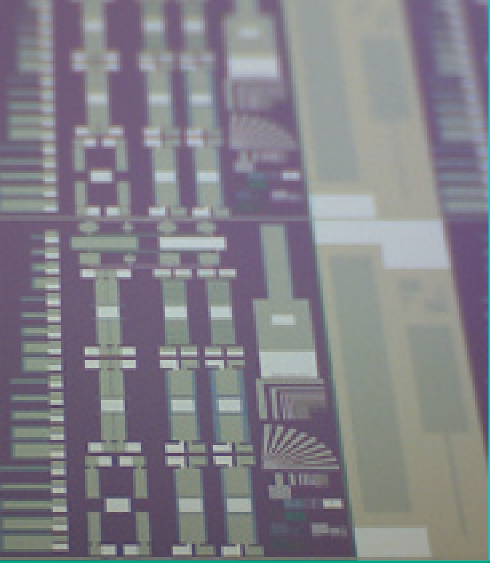
With its clearly defined mission of application-oriented research and its focus on key technologies of relevance to the future, the Fraunhofer-Gesellschaft plays a prominent role in the German and European innovation process. Applied research has a knock-on effect that extends beyond the direct benefits perceived by the customer: Through their research and development work, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. They do so by promoting innovation, strengthening the technological base, improving the acceptance of new technologies, and helping to train the urgently needed future generation of scientists and engineers.

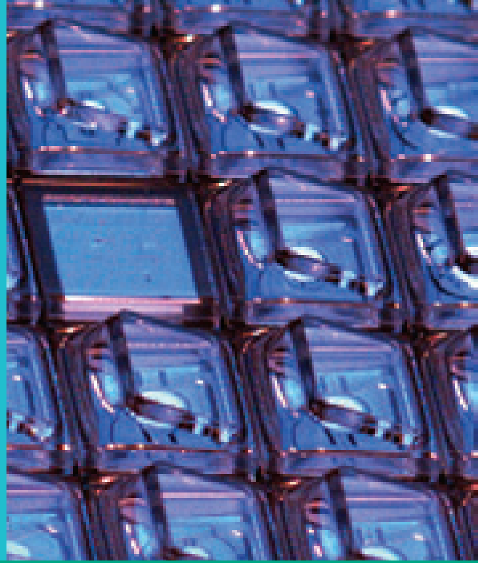
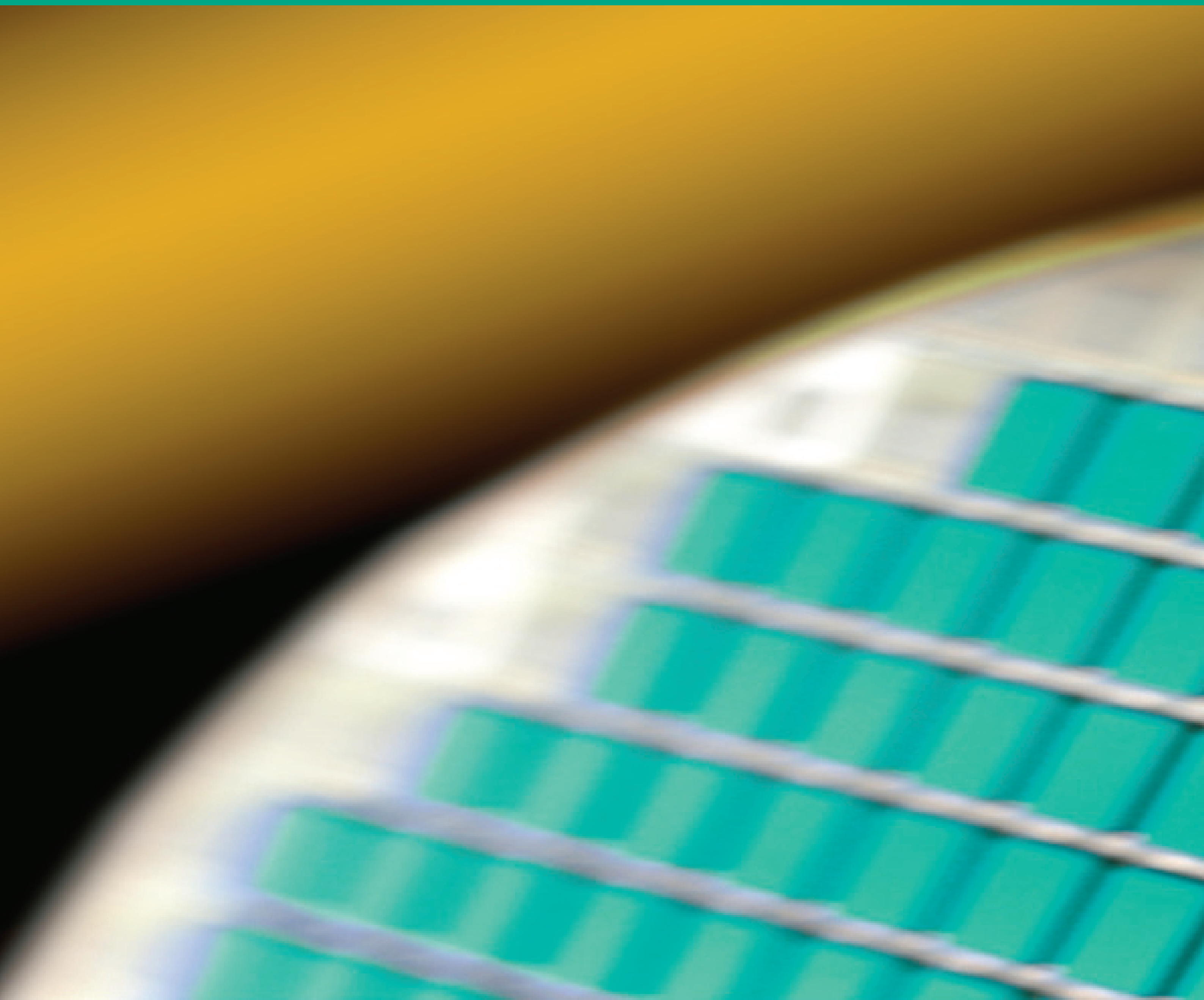
As an employer, the Fraunhofer-Gesellschaft offers its staff the opportunity to develop the professional and personal skills that will allow them to take up positions of responsibility within their institute, at universities, in industry and in society. Students who choose to work on projects at the Fraunhofer Institutes have excellent prospects of starting and developing a career in industry by virtue of the practical training and experience they have acquired.

The Fraunhofer-Gesellschaft is a recognized non-profit organization that takes its name from Joseph von Fraunhofer (1787–1826), the illustrious Munich researcher, inventor and entrepreneur.

LOCATIONS OF THE RESEARCH ESTABLISHMENT



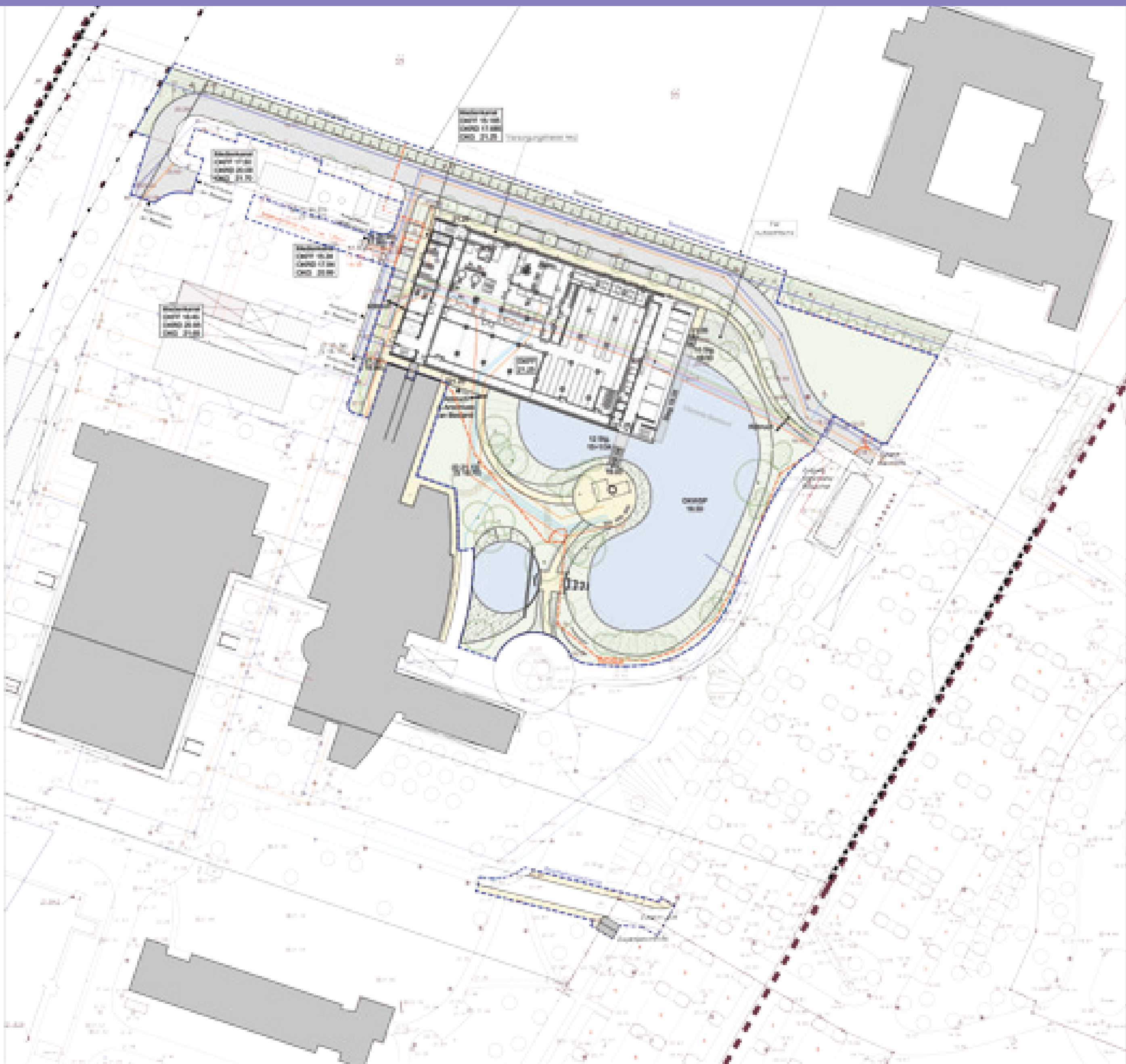


REPRESENTATIVE RESULTS OF WORK

REPRESENTATIVE RESULTS OF WORK

MICROSYSTEMS TECHNOLOGY (MEMS) AND IC DESIGN



EXPANSION OF ISIT TECHNICAL INFRASTRUCTURE

The main technological working areas of ISIT - MEMS technologies and power electronics - are experiencing a strong and continuous growth rate. In line with this increasing demand ISIT is executing research projects every year with more than 350 enterprises.

Growing demand has led to a strong capacity utilisation of all resources in the ISIT laboratories and a high occupation of office areas. This high utilisation rate is starting to constrain the working potential in the clean room areas. Accordingly in the last years all reserve areas in the ISIT clean room building and basement area below the clean room have been upgraded into laboratory areas to set up necessary working environments for many projects.

To secure sufficient working areas for future projects of ISIT, to extend research areas of ISIT and to be able to perform this research according to „state of the art" and to remain an attractive research partner for industry it is now necessary to take in hand a fundamental expansion step for ISIT by set up and instrumentation of new and advanced clean room laboratories.

Site Development

A new laboratory building will be set up and integrated into the existing ensemble of orthogonal building blocks on the ISIT site. A new building will be erected in northern direction partly extending into the existing, artificial pond. The new building will therefore be located in front of the entrance gate and will become a prominent sign of ISIT.

The new building will be connected by a bridge to the existing laboratory building 301 allowing an uninterrupted internal transfer of staff members and materials between all laboratories. Additionally, cooling units that are needed for running of the new laboratories will be installed on the roof of the 301 building next to the new building. The new building will be aligned to the base directions of the existing buildings creating a protected courtyard from the prior created green area. The chosen building site minimises interference with existing infrastructure, especially the gas farm while at the same time an optimized connection to existing laboratories is realised.

As a consequence of the chosen building site the existing road for delivery of gases, materials and chemicals has to be shifted further north to the land boundary of Fraunhofer property. Additionally several supply lines that are laid below the existing road have to be replaced to prepare the building ground. The shifted supply road will be used for material transportation into the new building. Additionally, materials for the new laboratories can be supplied directly from the existing supply and disposal facilities next to the new building. For visitors and employees of the older buildings the main access way from the entrance gate will not be changed.

Building Conception

The new building will enclose three different functional areas: offices, laboratories and storage areas. These functions will be separated creating three consecutive sections within the new building with the laboratory areas in the middle. Approx. 600 m^2 office areas will be errected that are planned for 60 Fraunhofer employees, students and scientific assistants. The functional building blocks will be covered by a uniform frontage with a hierarchically arranged level of transparency. Zones between the functional blocks will be used for room access by open floors. Main part of the new building will be approx. 1000 m^2 clean room areas next to 500 m^2 standard laboratory areas. All necessary supply floors and installations are arranged around this storey.

In the basement (level 0) all technical installations for supply and disposal functions will be set up like electric power supply, DI and process cooling water distribution including neutralization and water disposal, storage of chemical materials and bypack areas for equipment installations. Also secure gas cabinets will be setup for stocking and distribution of speciality gases similar to the existing clean room.

In the clean subFab section (level 1) air from the clean room is distributed to the air return shafts. Additionally gases, wet chemicals and further supply lines are distributed in this section and connected through the clean room floor to the equipment. In this floor below the clean room laboratory also the interlock for clean room access is set up. This interlock is connected by a stairway with the air interlock to enter the clean room.

The clean room section (level 2) is divided into a clean room area specified at class ISO 5 and a standard laboratory section. From the initial clean room layout planning sufficient area is available for installation of planned new equipment and to relocate equipment from the existing ISIT backend area when necessary.

The plenum (level 3) is made up from suspended ceiling elements and will be used for clean room fresh air supply using filter fan units. Make up of air and heating units (level 4) will be installed in the top most section above the plenum similar to the existing clean room building.

Time schedule

In 2010 general conception and detailed planning of the architectural realization as well as of the technical infrastructure and installations was performed. Company HTP Architekten und Ingenieure, Braunschweig is responsible for all architectural aspects while company DERU, Dresden is the technical planner for Fraunhofer. These technical plans have been examined and approved by public authorities in Schleswig-Holstein and by the federal government. Beginning of 2011 a final signing off of the total finance volume is expected. After the final financial approval Fraunhofer building department can initiate the necessary calls for tender on an European scale for the various building and installation blocks. The bidding procedure demands for a fixed period of time including two weeks of waiting time to allow for complaints from companies that are not chosen and do not receive a contract from Fraunhofer. It is expected that in summer 2011 first constructions above and below ground can start. Before start of construction the building site and new supply roads will be arranged on Fraunhofer area. It is expected that end of 2012 first equipment can be installed in the new laboratory building.

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Erweiterung Kältezentrale
Ansicht Ost
Neubau Reinraum II
Ansicht West
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ISIT_FRAUNHOFER-GESELLSCHAFT
NEUBAU REINRAUM 2
Z-Bau 01.10.2010
ARCHITEKTUR
ANSICHT WEST/OST

DUAL-USE OF 200 MM MEMS LINE FOR R&D AND PRODUCTION

At the Fraunhofer ISIT site the combination of volume production and R&D services has been successfully established within the same MEMS clean room line. Such a dual-use concept seems to be a chance to handle the tremendous cost pressure which advanced 200 mm MEMS production processes imply.

MEMS is different

The outer appearance of a MEMS fabrication site (MEMS fab) is in general not significantly different from a common semiconductor fab. Both make use of similar clean room facilities, equipment and process technology. However, for integrated electronics in principle only few basic elementary units like e.g. transistors and resistors are needed. Based on their intrinsic electronic properties mathematical logic concepts can be emulated. Here the synergy of similar technological demands for various product applications pioneered the present semiconductor industry and especially the role of foundries. Yet for MEMS the absence of an equivalent mechanical elementary unit results in the lack of such generic processing. It is well-known that very often a MEMS product needs its own specific process flow or at least dedicated process modules. This fundamental limitation, also known as the 1st MEMS Law: one product – one process – one package, impedes streamlined and high volume industrial production of different MEMS devices. Hence the very fragmented MEMS product and process landscape effectuates minor production volumes and low capacity utilization rates (see figure 1). These special conditions are still major challenges for all MEMS manufacturers. To strengthen and stabilize MEMS production business a strong diversification of customers and technologies is therefore required. A supplementary combined use of clean room facilities and equipment for production on one hand and research and development activities on the other hand can facilitate a cost-effective operation structure.

Motivation for coexistence of MEMS production and R&D

Combination of research and production activities is assessed controversially; most often quality and reliability issues are put into question. But here it is reasonable to distinguish between different levels of research (basic, industry) as well as to account for the concept of collaboration. Nowadays modern research methods have reached industrial-like requirements in respect to cost planning, process performance and technology grade and even make use of similar quality management tools. Especially industry driven MEMS R&D has closed the gap and the necessities of an industrial production have been recognized. These high-level industrial specifications first of all increase effort and cost and may diminish some autonomous spirits of research. Nevertheless several beneficial results are attained:

Figure 1

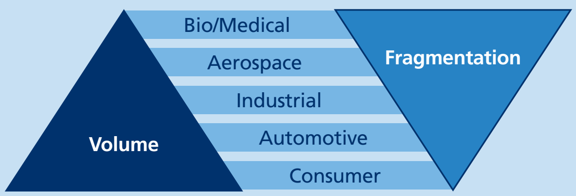


Figure1: Market volume and market differentiation for various MEMS product groups

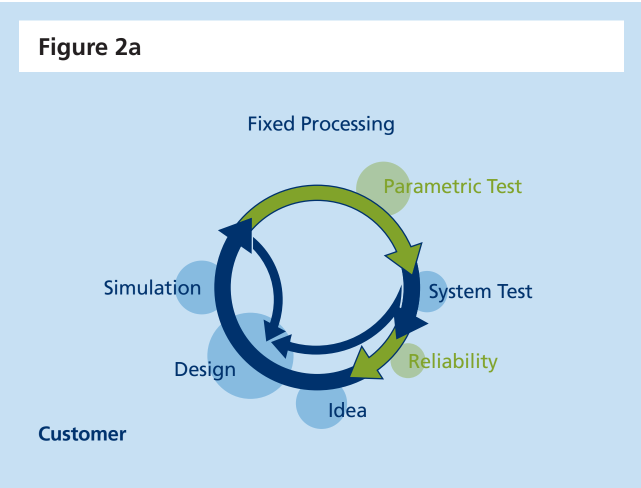


Figure 2a: Microelectronic Development Cycle

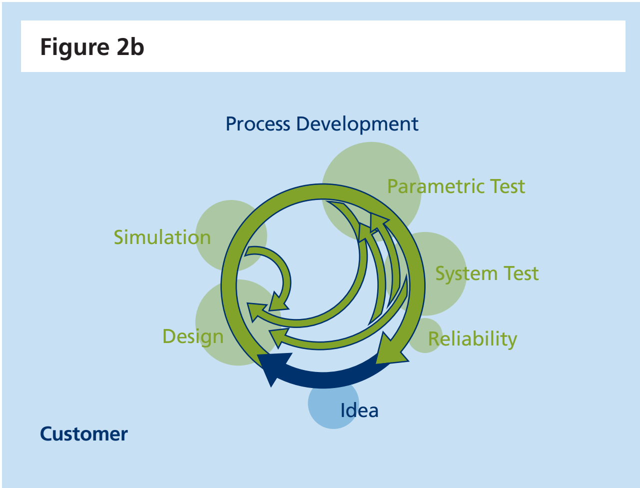


Figure 2b: MEMS Development Cycle

1. For MEMS the accomplishment of the different products stages from the idea to the final mass production (see figure 2) are in most cases not linear but highly iterative. There is a continuous interaction between design and process throughout the complete maturation process. The agglomeration of R&D and production helps to shorten these product cycles by barrier-free and instant information exchange. The R&D team is aware of the production demands and designs the product for manufacturability right from the scratch.
2. For a state-of-the art 200 mm MEMS fabrication line a capital invest of 50 - 100 million US$ is needed and annual operational cost >10 million US$ are estimated. A pure R&D business model is not able to cover neither operating nor primary capital costs. On the other hand MEMS manufacturer often start with low volumes after a long development time span. It is apparent that a symbiotic dual-use of manufacturing facilities is beneficial for both parties.
3. During MEMS development a lot of process know-how and IP is generated not only within the architecture and design but also in conjunction with the process flow. A close and associated R&D-Production consortium prevents the risk of knowledge drain.
4. Implementing research within a production environment means having access to highly stable and mature processes at any time. Engineering loops are drastically shortened. Research manpower is focused on relevant process development.

The need for 200 mm wafer

Although there may be an antagonism regarding the MEMS product volume and a requested substrate size of 200 mm, a conversion will become mandatory within the next years. Lowering factory costs is the major driving factor. Here a cost reduction of 30 - 40 % per device can be achieved by switching from six to eight inch.

Another argument is the conditional compatibility to standard CMOS Foundries, either for post-CMOS MEMS or for wafer scale packaging of CMOS and MEMS wafer. Finally equipment-related synergies from standard semiconductor business can be exploited. Here eight inch machinery is in general more advanced, features superior performance and guarantees availability of repair and spare parts. In addition a broad spectrum of used equipment is available. For MEMS manufacturer as well as for research organizations the conversion to eight inch is a challenging but fundamental contribution to secure future competitiveness and to maintain the innovative ability.

Dual-Use Concept at Fraunhofer ISIT Itzehoe

The Fraunhofer ISIT is one of the German pioneers in MEMS technology. More than 25 years industry-oriented research and development in the field of MEMS sensors and actuators, microoptics, microfluidics and RF-MEMS has established ISITs superior reputation for microsystem technology. ISIT provides more than 3.200 m² of clean room spacing for the common development and production of IC electronics and MEMS devices. Next to technology sharing ISIT offers access to its potent and valuable IP portfolio.

The MEMS Foundry Itzehoe is a newly formed spin-off from the Fraunhofer ISIT and is located within the same wafer fabrication facility. MFI is focusing on 200 mm MEMS foundry services and acts as a customer oriented contract manufacturer. For this MFI has a close contracted coope-ration with the Fraunhofer ISIT. Fraunhofer ISIT is offering industrial MEMS research and development services up to a prototyping stage. The subsequent industrialization and production service from medium to high volume within the same clean room environment is then assumed by MFI. So MFI together with Fraunhofer ISIT can offer a complete one-stop shop for MEMS products which includes all stages of a product cycle from the basic idea up to sustainable high volume production.

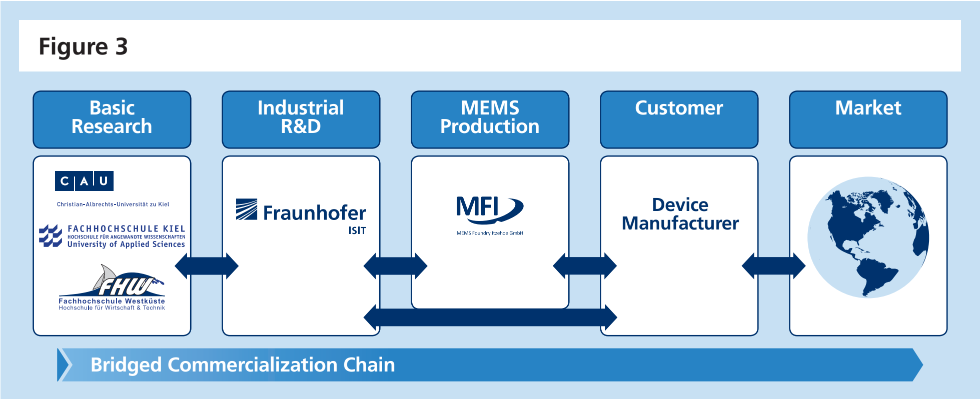


Figure 3: Cooperation concept in development and production

Figure 1: Oerlikon cluster line, view from the clean room

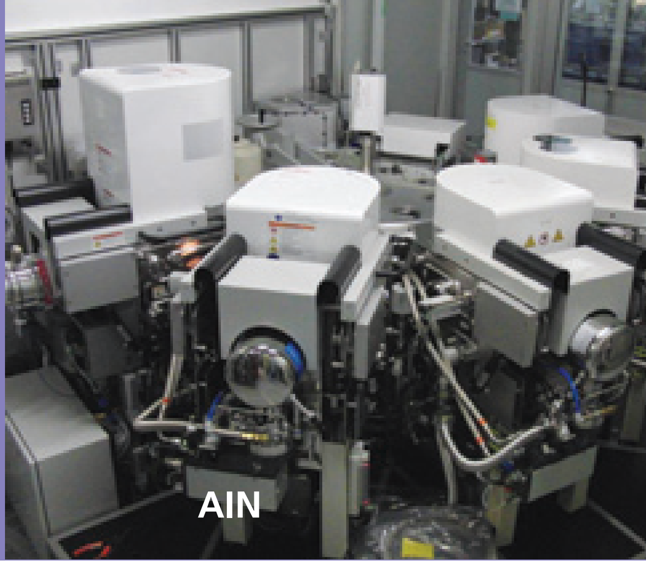


Figure 2: Rear side of the cluster line. Around the central handling robot, the various process chambers can be seen. The lower left chamber is used for sputtering AlN

PIEZOELECTRIC ALN FILM ON CANTILEVERS FOR SENSING AND ACTUATION

In the EC project PROTEM („Probe-based Terabit Memory", FP6 Project 2005-IST-5-34719), a new fabrication technology for conducting AFM cantilevers with Aluminum Nitride (AlN) integrated actuators has been developed together with IBM Rüschlikon [IBM: U. Drechsler, A. Sebastian, M. Despont: IBM Research GmbH, Zurich Research Laboratory, Rüschlikon, Switzerland]. This type of AFM cantilevers is of great interest for dynamic AFM applications such as tapping or dithering mode as well as for using piezoelectric structures as an integrated sensor.

Piezoelectric materials are able to convert an electrical voltage into a mechanical movement, which makes them an interesting material for micromechanical sensors and actuators. One of the most readily available candidates for silicon process integration used to be AlN, yet the recent progress in the deposition of Lead-Zirconate-Titanate (PZT) offers many promising perspectives. Compared to PZT, AlN generates much smaller cantilever deflections at the same voltage level due to a significantly lower piezoelectric d_{31} coefficient. However, AlN has several important benefits over PZT regarding the integration in MEMS fabrication processes. Beside the fact that AlN is fully CMOS-compatible, the AlN layers can easily be patterned by dry etching. Moreover, AlN does not require any poling after its deposition since it is not a ferroelectric material and it is less critical to long term stability issues. Due to a much lower dielectric constant of AlN, cantilever structures show a better sensitivity compared to those made of PZT. Hence, with exception of applications where large actuations forces or deflections are required, AlN is favoured over PZT for cantilever sensor and actuator structures.

Figure 3

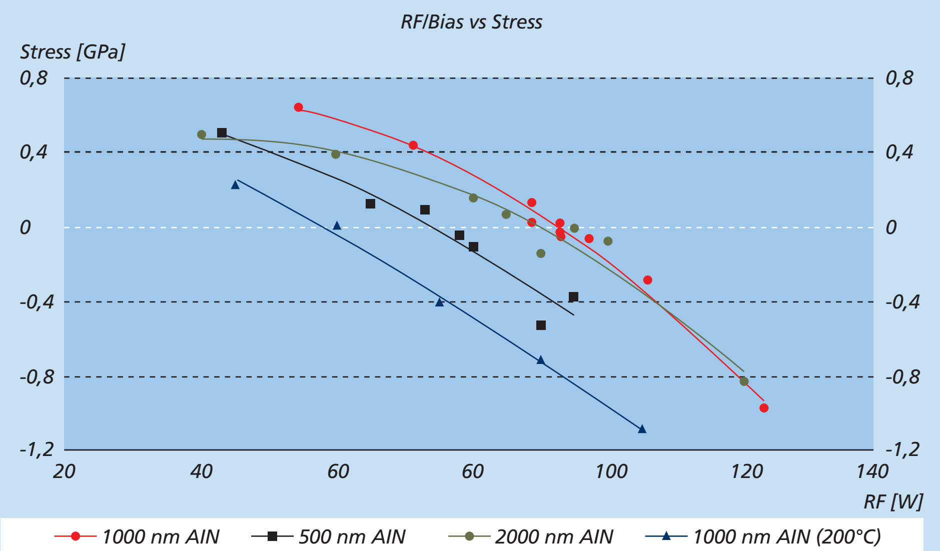


Figure 3: Dependence of the mechanical stress in the sputtered AlN films from the applied RF power. To achieve zero stress, the power level must be adapted to the projected film thickness. Using a process temperature of 200 °C instead of 400 °C used in the standard process leads to a drastical shift in the mechanical stress behavior of the deposited AlN films (lower vs. upper curve)

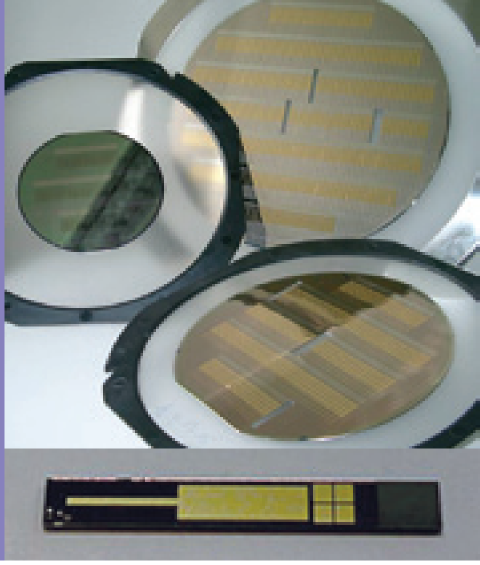


Figure 6: Wafer with test pattern for the characterization of the piezoelectric performance of sputtered AlN films. The inset picture shows a diced test chip used for determining the $e_{31,f}$ values of the piezoelectric film

Figure 4

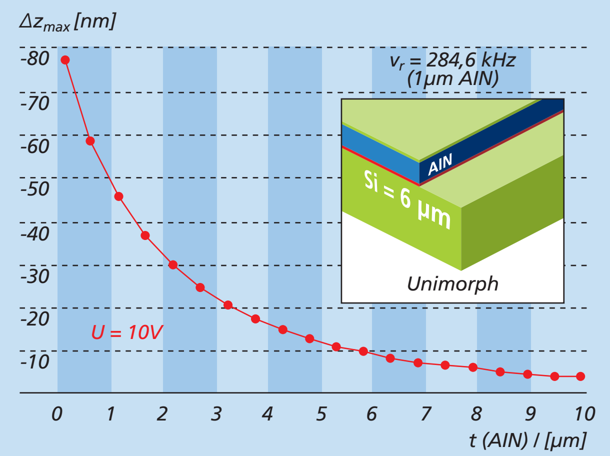


Figure 4: FEM simulation of cantilever deflection for a given applied voltage of 10 V as a function of AlN layer thickness. Using thinner AlN films would increase the achievable beam deflections

Figure 5

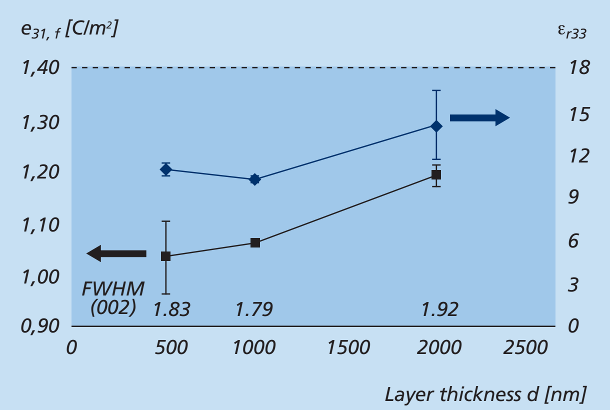


Figure 5: Measured $e_{31,f}$ values for AlN layers of different thicknesses. Thin AlN layers showed a decrease in their piezoelectric performances

For the deposition of AlN layers, a dedicated sputter tool (Oerlikon cluster line, see figure 1 and figure 2) is available at Fraunhofer ISIT, which allows the preparation of high quality and very uniform AlN layers. Typically, the AlN films are sputtered at wafer temperatures around 400 °C to ensure a high degree of texturation of the deposited films. Since the mechanical stress causes a bending of the cantilever structure, the control of stress and strain in the sputtered AlN films is essential. A detailed study shows that the stress in AlN depends primarily on the applied RF power during sputtering, but also in minor degree on the thickness of the prepared AlN layer (see figure 3).

To provide an adequate actuation at low voltage (<15V), a thin AlN layer would be desirable. The finite element simulations (FEM) clearly show that even on 6 µm thick silicon, AlN layers down to 100 nm would continous increase the deflection (see figure 4). However, preparing cantilever test elements (see figure 6) for determining the lateral piezoelectric module ($e_{31,f}$) (see figure 5) of sputtered AlN films of various thicknesses showed lower $e_{31,f}$ values for 500 nm and 1000 nm, compared to 2000 nm thick AlN layers (see figure 5). The use of a platinum bottom electrode limits the reduction in the $e_{31,f}$ values to about 20 % compared to molybdenum bottom electrodes. The observed degradation of AlN films below 500 nm is probably induced by dominating interface effects.

For fabricating cantilever structures with integrated actuator and conducting tip, a common fabrication process has been developed jointly by Fraunhofer ISIT and IBM. In the wafer runs, the piezoelectric and electrode layers are integrated directly on pre-processed 100 mm wafer from IBM. Prior to the fabrication of the piezoelectric drive, the conduction tip was prepared on 100 mm SOI wafers by IBM

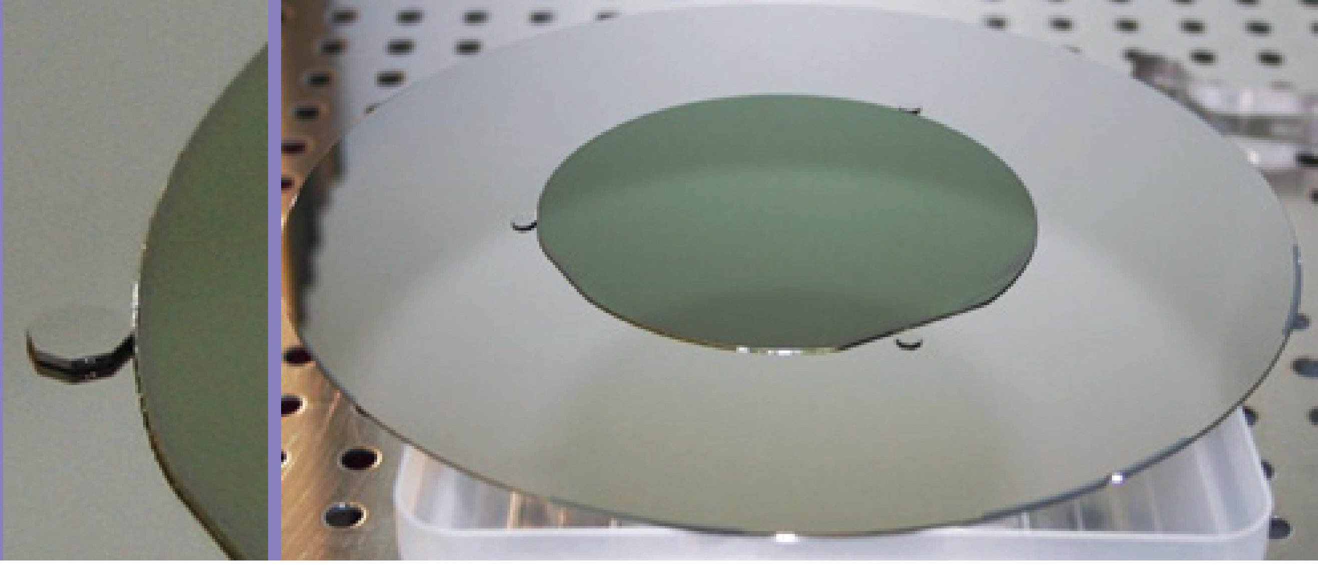


Figure 7: The 200 mm carrier wafer features small additional glass pins to guarantee a fixation of the 100 mm device wafer. Since the silicon surface of the carrier wafer remains unprocessed, a very smooth and even contact area between the silicon wafers can be achieved. The glass pins are thermally adapted to silicon and bonded anodically to the silicon wafer. An additional metal layer ensures good electrical coupling and homogeneous temperature rise during thermal ramp-up

Since 100 mm wafers cannot be directly processed in the ISIT 200 mm process line, a carrier wafer concept has been developed where specially prepared 200 mm wafers with features carries 100 mm wafer (see figure 7). During the sputtering process, the temperature control is very critical for the preparation of high quality piezoelectric AlN. Previous experiments with dry-etched cavities for the fixation of the 100mm wafer showed an undefined thermal coupling to the heated 200 mm wafer and higher chuck temperatures become inevitable. To improve the thermal coupling, the carrier wafer features bonded glass pins that ensure an accurate alignment and clamping of the 100 mm wafer. Since in this design the area between the wafers remains very even and smooth, a much better thermal contact between device wafer and carrier wafer can be achieved.

Test wafer prepared on the 200 mm carrier showed a lateral piezoelectric modulus $e_{31,f}$ between 0.89 and 0.94 C/m^2, which is about 10 % smaller than similar values measured on samples directly prepared on 200 mm wafer (see figure 8 and figure 9).

The process flow to fabricate a complete AFM cantilever with PtSi-based conduction tip and integrated actuators using 500 nm thick AlN actuators is summarized in figure 10. To avoid degradation of the piezoelectric stack during the high temperature treatment required for the tip fabrication, the tip is made prior to the metallization and AlN layer deposition.

A silicon oxide layer, used to avoid interdiffusion between the silicon cantilever and the piezoelectric stack, is kept as thin as possible to minimize cantilever bending. The cantilevers are fabricated on silicon-on-insulator wafer with an n-type device layer of 3 µm thickness. The tip is patterned and etched isotropically using SF_6. During this

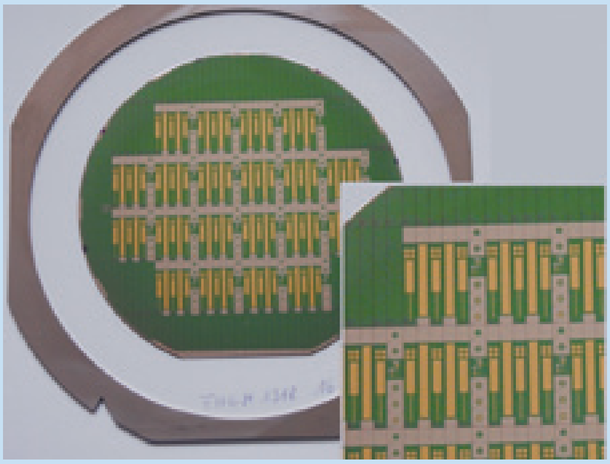


Figure 8: Test wafer with AlN test structures processed on the carrier wafer with glass pins. Underneath the AlN layer, platinum as the bottom electrode was applied

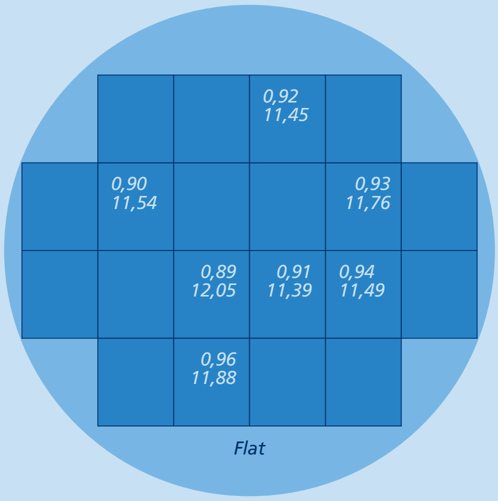
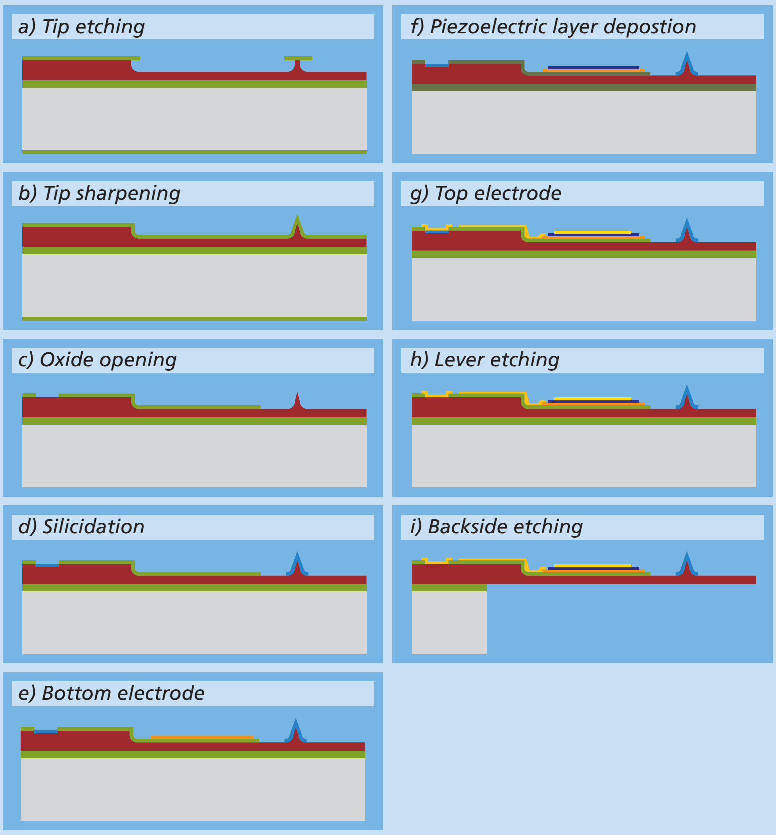


Figure 9: Results of electrical and piezoelectrical characterization of the AlN test wafer from Fig. 8. The $e_{31,f}$ coefficients (upper value) are in the range of 0.89…0.94 C/m^2, while the permeability (lower value) ranged from 11 to 12

step, the anchor for the cantilever is also defined. The bottom electrodes are formed by Ti/Pt patterns fabricated using a lift-off process. The piezoelectric AlN layer is then hot-sputtered on the wafer, followed by sputter deposition of a molybdenum layer that serves as a hard mask for wet etching in hot TMAH solution. After its removal, the top electrode and wiring are formed by sputtering an Au/Cr layer and structuring it through wet etching. The whole fabrication process (see figure 10) is completed by patterning the cantilevers and finally releasing them using deep RIE of the bulk silicon. SEM images of completely fabricated AFM devices are shown in figure 11 and 12.

Measurements on the completed devices show a static deflection in the range of 100 nm, depending on the designs. First AFM tapping mode imaging experiments using the piezoelectric AFM cantilevers demonstrate the viability of the concept.

Figure 10



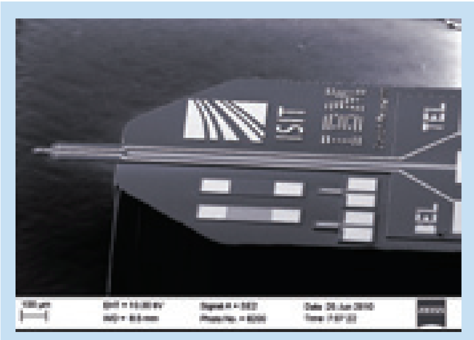


Figure 11: SEM picture of the complete AFM cantilever chip

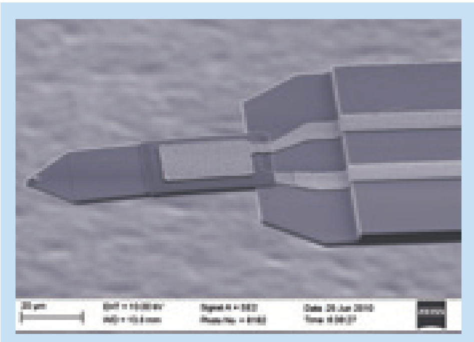


Figure 12: Detail of AFM cantilever with integrated AlN structure and tip

MICRO LENSES BY VISCOUS GLASS MICRO MACHINING

Micro optical elements made of glass are interesting since plastic materials suffer from many limitations with respect to thermal, chemical and long term stability issues. The project "Innovative Technologie zur viskosen Formgebung von Glaslinsen auf Waferebene ViGO" Förderkennzeichen: KF2217501BN9 together with Plan Optik AG, Elsoff is focused on advancing the viscous glass forming (VIG) technique, originally invented by Fraunhofer ISIT. The VIG process starts with dry etched cavities in a silicon wafer which is sealed with an additional glass wafer by anodic bonding. During a separate annealing step, the glass material starts flowing, resulting finally in a lens shape.

The VIG glass process allows the fabrication of micro lenses on complete 8" glass wafers. This technique enables the preparation of lenses with sagittal heights of several hundreds of micrometers, which is unique for wafer level based fabrication of micro lenses. The process allows the preparation of concave and convex lenses. Since the VIG process avoids any mechanical contact of the surface of the glass lenses with a tool, very smooth surface can easily be obtained. The shape of the fabricated glass lenses differs from the ideal spherical lens shape in the range of 200 nm PV (peak to valley) (edge exclusion of 15 %) which corresponds to a lens quality of approx. $\lambda/8$ rms (see figure 1).

Figure 1

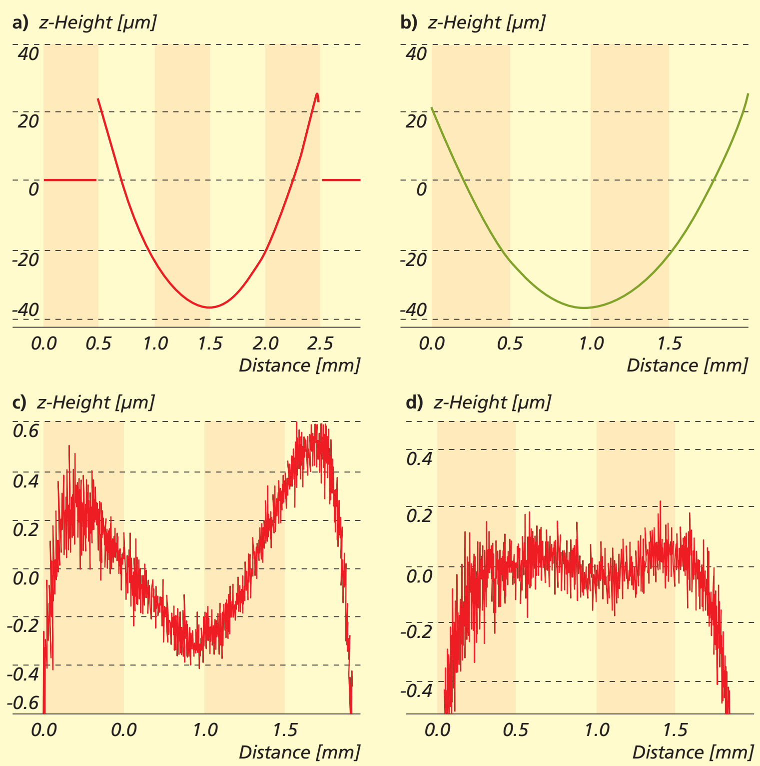


Figure 1: Measured curvature of a lens made of Borofloat® 33 (a); scanned surface of the lens (b); deviation from the spherical contour without any edge exclusion (c); deviation of the lens form with 15% edge exclusion (d)

Figure 2

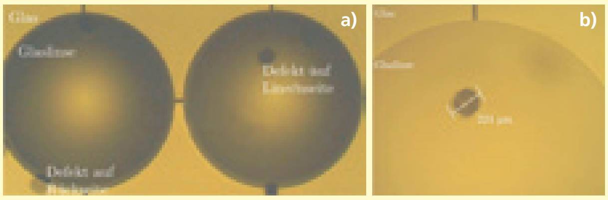


Figure 2: Microscopic view (10X) on same lenses made from Borofloat® 33. On the left side, several defects are clearly visible. The picture on the right side (20X) shows a single defect with a dimension of over 200 µm. The diameter of the lenses is approx. 2 mm.

Figure 3

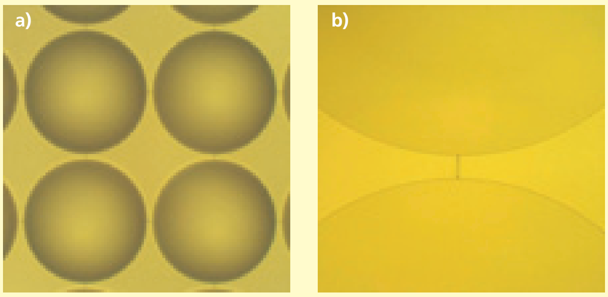


Figure 3: Microscopic view (2.5X) of a part of a lens wafer (left side). In this experiment the lenses are made of „Glass II“. On the right side, a more detailed view is visible (20X). In both pictures all lens surfaces are completely free of glass defects.

Main issues of the project are studies on the process stability and reproducibility, the wafer bow and the reduction of surface defects on the glass lenses. Since the commonly used Borofloat glasses tend to develop sporadic defects during the annealing process (see figure 2), a new glass material (Glass II) was tested for its principle applicability.

Despite the fact that this new glass material needs a higher process temperature, the density and the size of the defects could be drastically reduced by several orders of magnitude so that the overall yield could be increased to almost 100 % of the micro lenses (see figure 3). Since the achieved contour accuracy is comparable to the Borofloat glass, this glass type will become the preferred material for the VIG process (see figure 4).

Figure 4

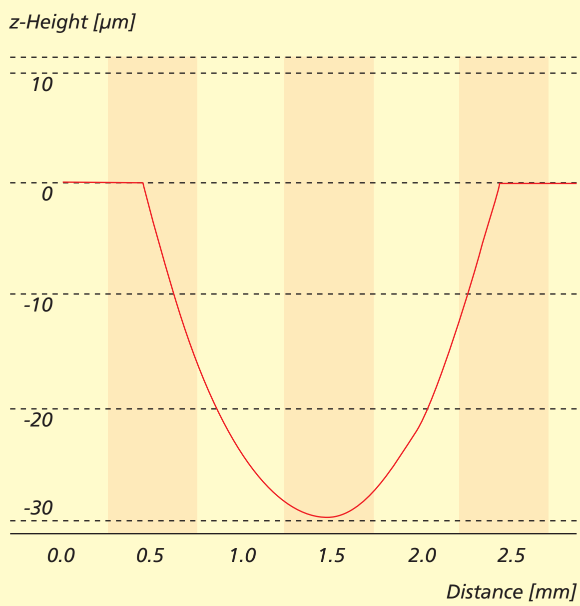


Figure 4: Scan over a lens surface made of Glass II. The central cut through the lens is visualised

RELIABLE LOW TEMPERATURE PACKAGING PROCESS FOR RF-MEMS

In most cases micromechanical devices must be hermetically packaged at the end of the fabrication process. Often a packaging on wafer level, before singulation, is the most efficient solution. For this purpose at ISIT a bonding process based on gold-tin soldering at temperatures below 300 °C has been developed for 8 inch wafers. In such a way even thermally sensitive MEMS structures, consisting of low melting metals like Al or Au, for example RF-MEMS, can be packaged without damaging.

Figure 1 presents a cross-sectional view through a packaged device and a photo of single chips. The cavity between MEMS and cap chip is typically only few tenth of µm in height but can exhibit edge lengths of several mm. The width of the surrounding AuSn sealing frame is usually clearly below 100 µm. Nevertheless a robust and hermetic sealing of the MEMS inside the cavity is achieved. The package widthstand prolonged storage at elevated temperatures as well as extreme humidity (1500 hours in water vapour at 121 °C and 2 bar) or thermal cycling (1000 times -40 °C/ +140 °C) without a degradation of the MEMS performance. The sealing strength is high. Even with 50 µm wide sealing frames a shear strength of about 90 MPa is achieved. That allows thinning of the 1,5 mm thick wafer stack from both sides down to 500 µm using common grinding and polishing.

To ensure the electrical connection of the MEMS structures within the cavity by lateral feedthroughs below the sealing frame the bonding process should tolerate a certain topology. In this particular case up to 1 µm thick feedthroughs can be reliable sealed. This renders this packaging suitable for RF applications. For a compensated CPW with only 0,5 µm thick feedthroughs return and insertion losses of respectively > 15 dB and < 0,3 dB can be achieved in a range from DC to 40 GHz.

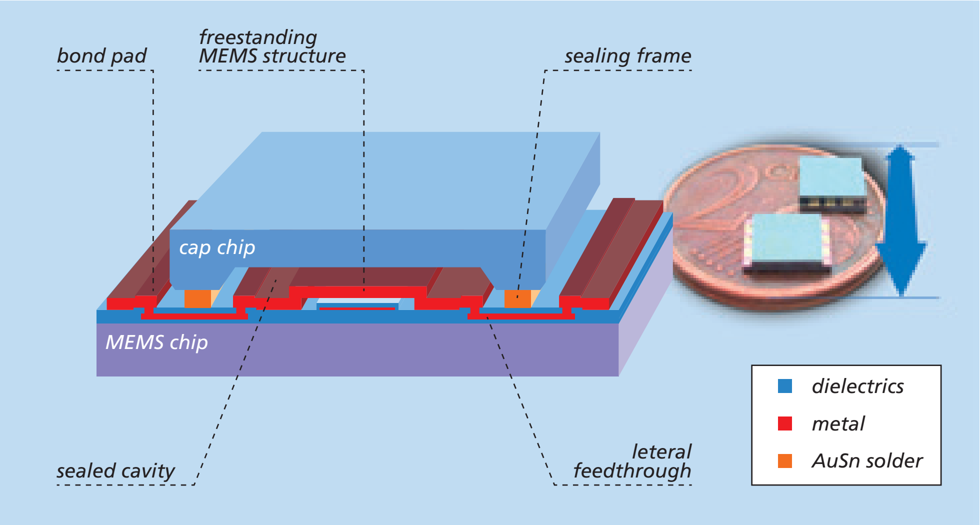


Figure 1: Schematic cross-section through a MEMS device sealed on wafer-level using Au-Sn soldering and a photo of single chips

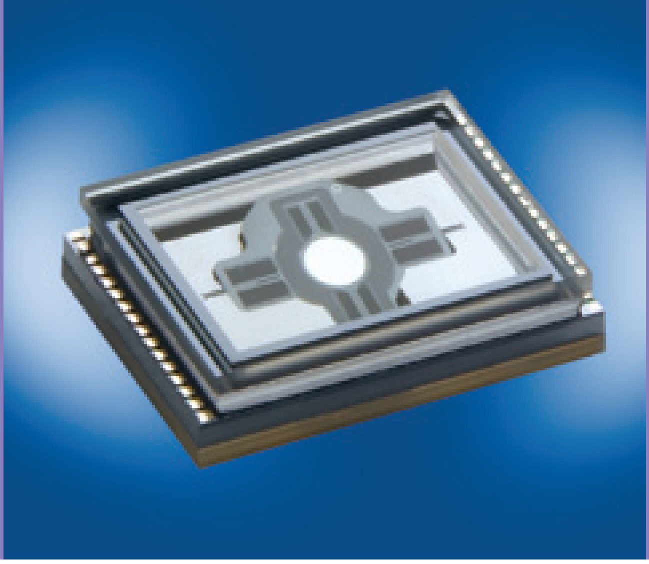


Figure 1: Vacuum packaged 2D MEMS scanning mirror; the chip volume is only 0.07 ccm

SYSTEM ELECTRONICS TO CONTROL A TWO AXIS MICROMIRROR FOR LASER PROJECTION

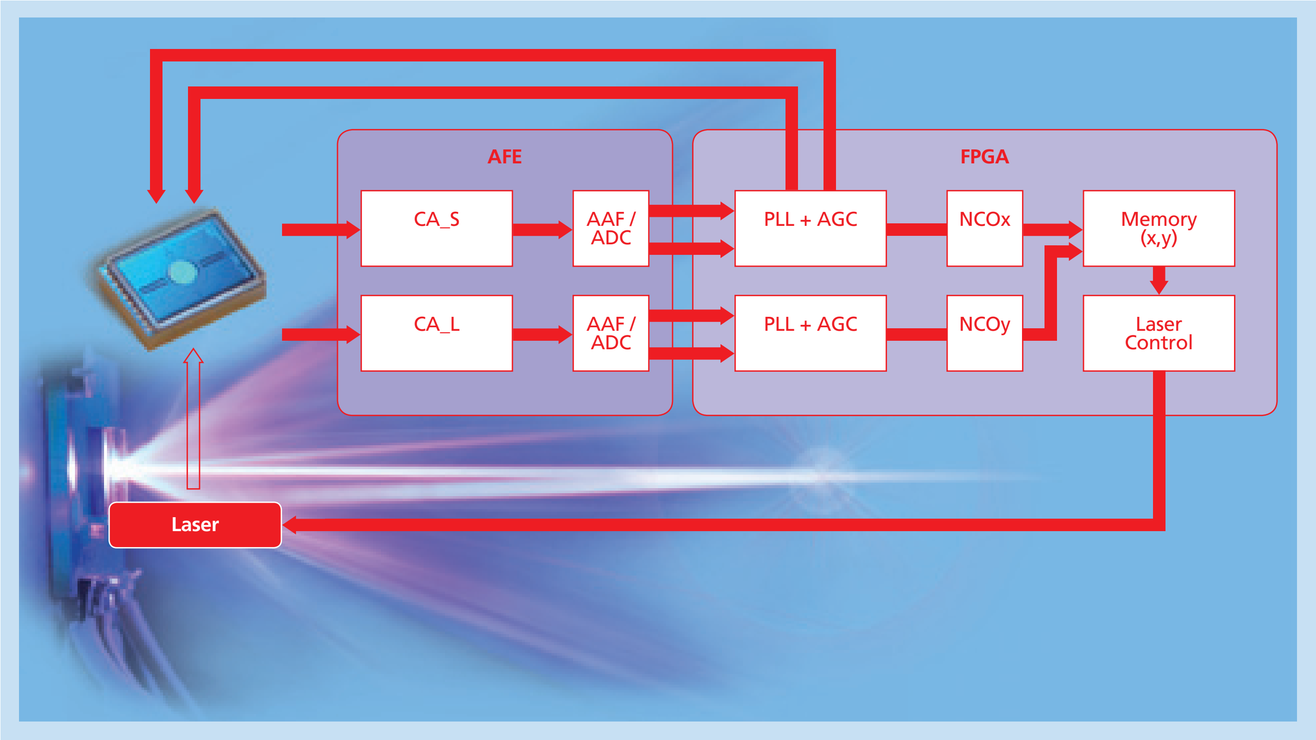
The intensive development of micromechanical two-axis mirrors for laser projection applications has resulted in devices with unique properties like

- very large optical scanning angle up to 70 deg at resonance in both axis
- very low power consumption due to driving in resonance
- very small system of less than 0,07 ccm including excitation and measuring electrodes

To be able to make use of these mechanical qualities a complex system electronics is needed to drive and control the movement of the mirror and to synchronize the output of a laser-beam very synchronic with the mirrors position.

The mirror itself can be represented in a first step as a network of variable capacitors. The readout electronics located in an analog frontend (AFE) part converts the changes of the comb

Figure 2: Block diagram of system electronics including loop and laser control



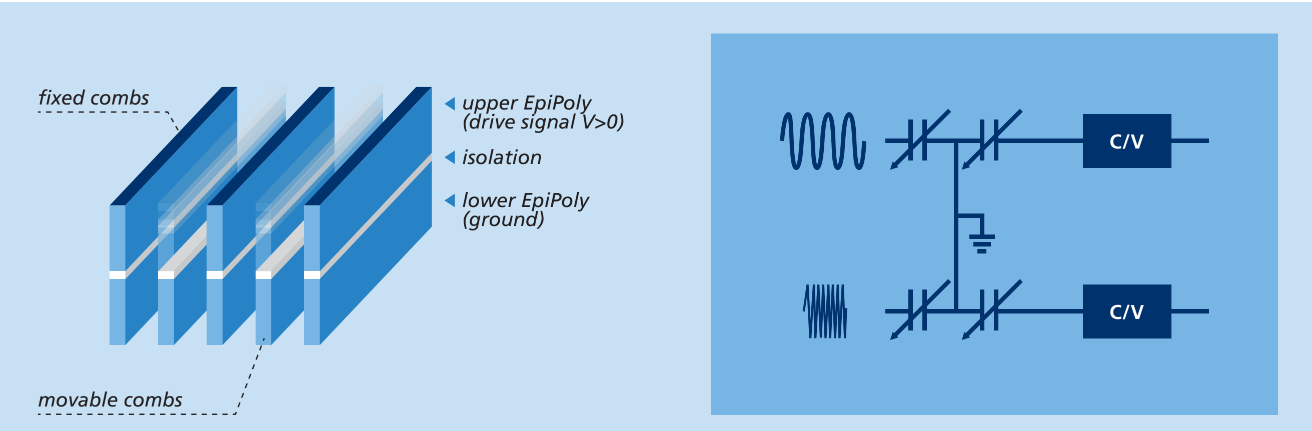


Figure 3: Comb structure for electrostatic driving and capacitive detection (left) and the corresponding electrical diagram including c/v-converters (right)

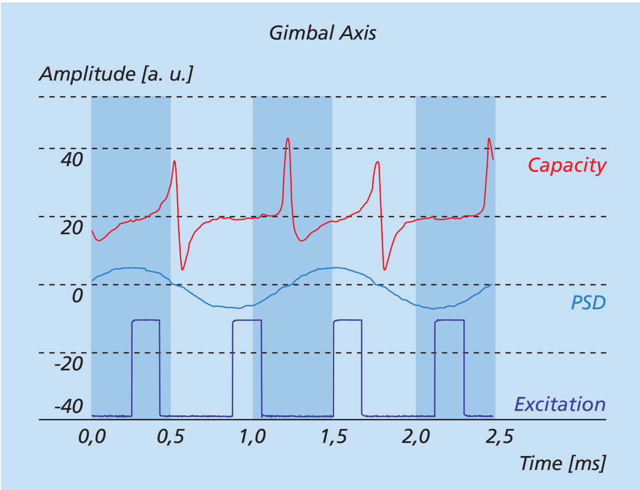


Figure 4: Measured signal waveforms

capacitors into a voltage proportional to the motion of the mirror. This capacitor-to-voltage conversion (C/V) is realized by dedicated charge-amplifiers, where the very "special" output signal form is caused by the process oriented design of the mirror.

The control electronics is based on a straight forward PLL (phase locked loop) approach coupled with a amplitude-gain control to keep the movement of the mirror stable regarding frequency and amplitude.

The main challenges that have to be solved to stabilize the control loops are the very poor signal-to-noise ratio and the mechanical crosstalk between the two axes. A special read-out strategy has been developed that allows a sufficient demodulation of the wanted signal out of the noise floor.

The motion and laser control has been implemented in a first step in a FPGA, written in VHDL. This flexible programmable platform allows a continuous improvement with low debug times. In the next step it is planned to transfer the analog and digital part into a single asic.

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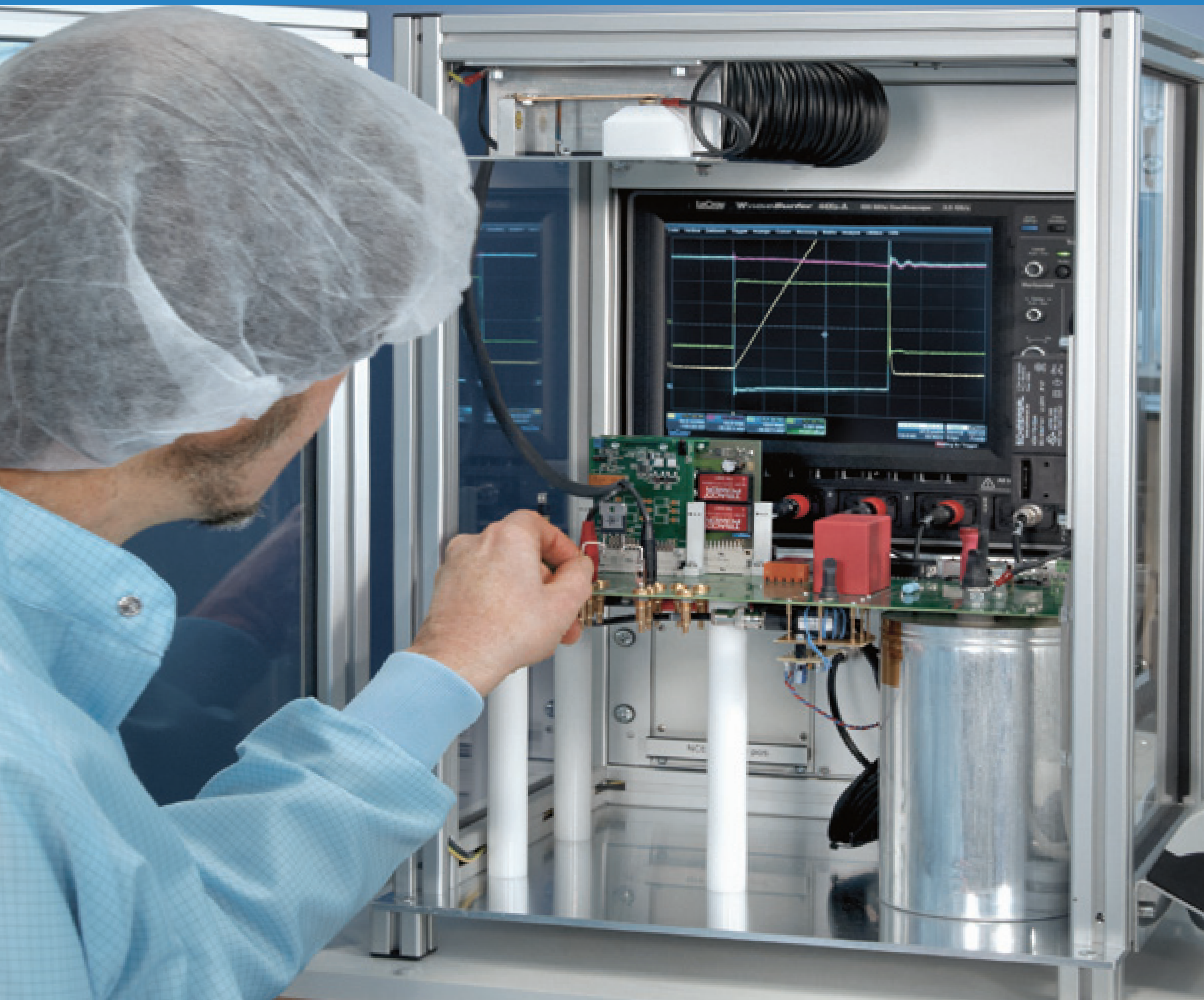
REPRESENTATIVE RESULTS OF WORK

IC TECHNOLOGY AND POWER ELECTRONICS



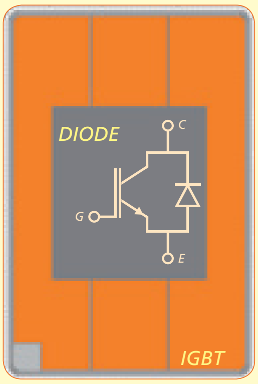


Figure 1: Layout of an RC-IGBT with integrated diode (dark) and IGBT trench cells (orange)

DEVELOPMENT OF RC-IGBTs

Energy efficiency, power density and robustness are the key issues regarding the development of modern technologies for power conversion and electro traction. With respect to these objectives Fraunhofer ISIT is engineering the base technology for a new generation of monolithic integrated silicon based power devices, namely "Reverse Conducting Insulated Gate Bipolar Transistor" (RC-IGBT). Within the research project "Fraunhofer Systemforschung Elektro-Mobilität" (FSEM) these RC-IGBTs are designated to be used as demonstrator in power modules for DC/DC conversion in electric drive applications.

As shown in figure 1a free wheeling diode and IGBT trench cells are integrated on a single chip. The RC-IGBT is designed for 1200 V at 150 A. The size of the chip is 10 x 15 mm² and one third of the component is used as diode area. Because of this monolithic integration of the free wheeling diode into the IGBT, the number of chips within the power modules and also their parasitic inductance are reduced. The latter is increasing the switching speed clearly.

The integration of the diode into the IGBT normally leads to a so called "snapback" characteristic. Simulation results for RC-IGBTs with and without a snapback progression in the current-voltage characteristic (I_C(A) vs. V_{CE}(V), are shown in figure 2a and 2b. A snapback behavior is always observable except in case the snapback is prevented by constructional measures. An insulation between diode and IGBT would effectively suppress the snapback.

The simulation results can be explained by focusing on the function of the p^+ emitter in an IGBT structure (see figure 3). In the forward direction, the p^+ emitter is injecting holes into the n^- region of the IGBT drift zone. This, together with the electrons from the MOS-Transistor trench cells, results in an increased conductivity as in case of a bipolar transistor (see figure 2a).

If the p^+ emitter is missing from the structure, only a vertical MOS-transistor with its high resistivity drift zone is operating, which produces a curve characteristic similar to that in the beginning of curve 2b. For the RC-IGBT with existing

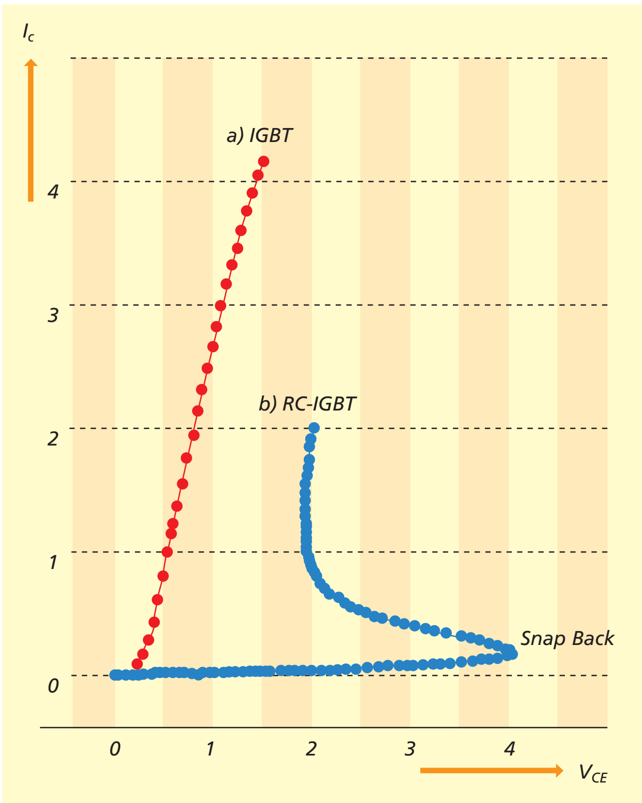
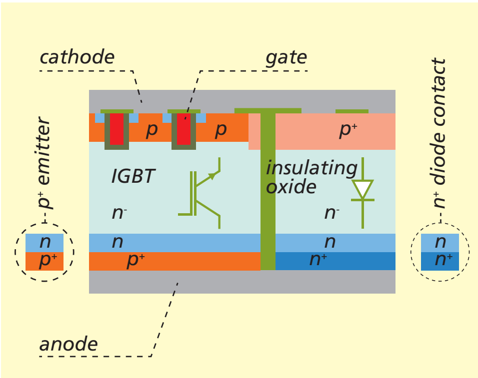
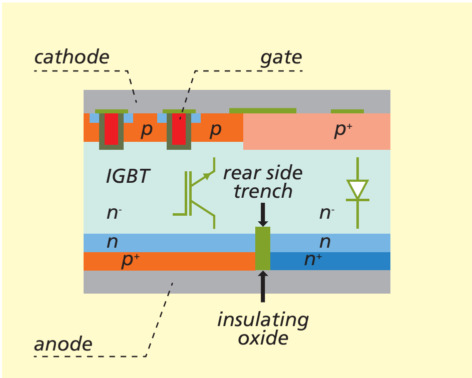


Figure 2: Simulation of the snapback characteristic
a) No snapback progression because either an insulating trench is extending through the silicon substrate or no diode is existing.
b) Strong snapback because of the emitter short





Left, Figure 3: Cross section of through the silicon trench insulation (green) between Diode and IGBT

Right, Figure 4: Cross section displaying a rear side trench, which is dividing the diode and IGBT contact area

p+ emitter the simulation shows at first a MOS and then an IGBT curve progression. For low forward voltage, the n+ contact acts as low resistance short relatively to the p+ emitter of the IGBT. At higher forward voltages the p+ emitter becomes effective and the current snaps back to the IGBT characteristic. The suppression of the emitter effect at low forward voltages is known from the thyristor technology and is called emitter-short.

The first idea to avoid the emitter-short is to insulate the diode completely from the IGBT by use of a deep trench as shown in figure 3. The trench would extend completely through the silicon substrate (e.g. 130 µm), separating both, the IGBT device and the diode perfectly from each other. On the one hand, great deal of effort is required for realizing the trench etching and filling process, on the other hand the silicon substrate might suffer from mechanical instabilities caused by emerging mechanical stress.

An alternative is the etching of a rear side trench into the silicon which separates the IGBT p+ emitter from the n+ diode contact as shown in figure 4. The corresponding simulation results are displayed in figure 5. They exhibit, that 4 µm to 10 µm deep rear side trenches filled with insulating oxide are deep enough for dramatically reducing the snapback effect. Therefore, the through silicon trench was replaced by a rear side trench.

Technology

A Field-Stop (FS) design is used for the Fraunhofer RC-IGBTs. The application of the FS technology is allowing to decrease the thickness of the component significantly. At least a minimum drift zone thickness of about 130 µm is required for 1200 V IGBTs. The thinning of the rear side of the Silicon wafer is lowering the on-resistance (low V_{sat}) and hence increasing the energy efficiency of the component.

After completing the front side processing, the wafer are temporarily bonded upside down to carrier wafer. It is mandatory to mechanically stabilize the IGBT device wafer in this way prior to the thinning process, since otherwise they could not be handled safely any more. The IGBT wafer are grinded to 130 µm thickness and finally polished (CMP) to reduce surface roughness.

In the following the rear side p⁺ emitter, the n field-stop and the n⁺ diode contact layers are defined by ion-implantation. The implantations are electrically activated by laser-annealing employing a pulsed YAG laser at 515 nm wave length while the wafer is still temporarily bonded. During laser-annealing, the intensity of the illuminating laser is controlled in such a way, that the wafer rear side is melting, whereas the front side of the 130 µm thick device wafer remains below the release temperature of the temporary bond.

The wafer are de-bonded from the carrier wafer as soon as the rear side processes and the final metallization are completed. By now the IGBTs are ready for first testing on wafer level.

First electrical results

In order to monitor the success of the RC-IGBT fabrication, first measurements on IGBTs without diode functionality have been performed. The IGBT break down is observed at 1200 V as displayed in figure 6. The threshold voltage, determined at 250 µA, amounts to 5 V. As shown in figure 7, a collector-emitter voltage of 1,2 V was determined for I_C = 5 A, measured on wafer level. Thus, the device technology for the 1200 V, 150 A, 10x15 mm² large RC-IGBT behaves as expected. The values measured are meeting the IGBT specifications.

The processes related to the rear side trench insulation with activated RC-IGBTs are in progress and will be reported next.

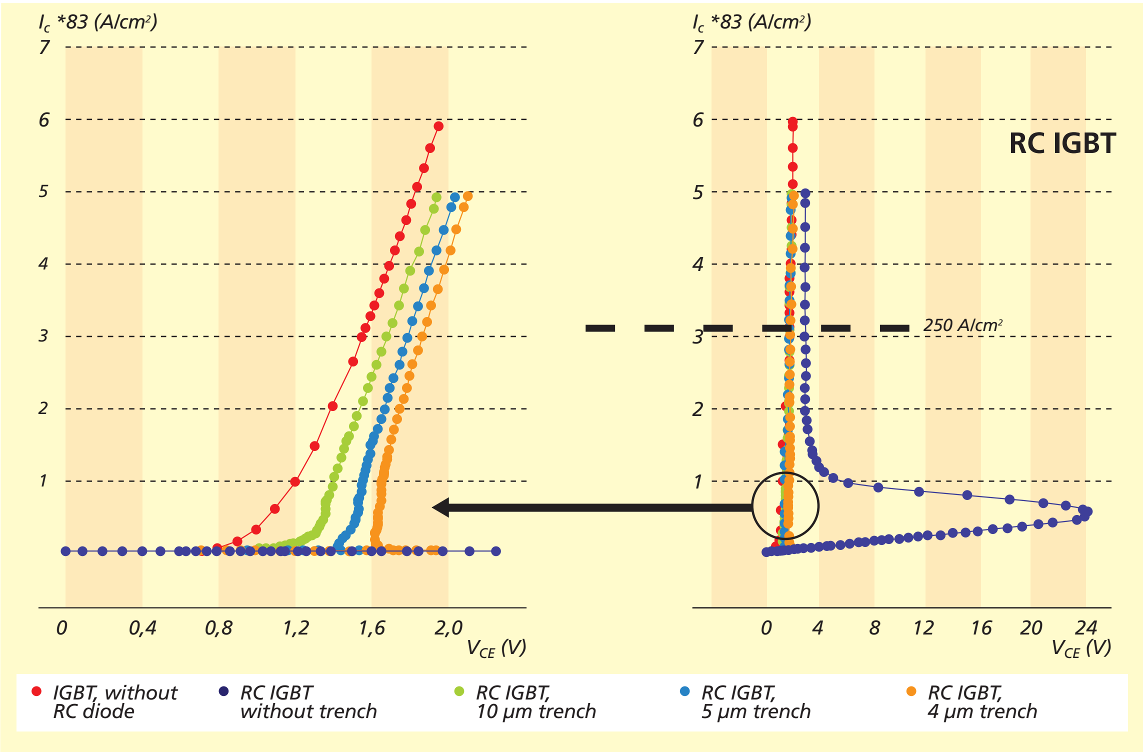


Figure 5: Snapback progression of RC-IGBT with increasing depth of the rear side trench of 4 µm to 10 µm. The rear side trench strongly reduces the snapback effect

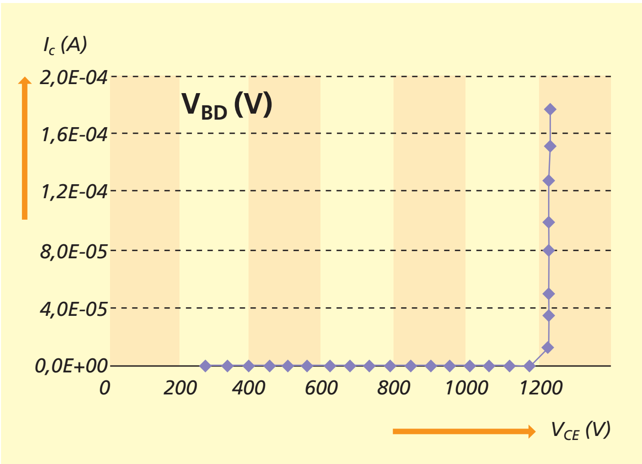


Figure 6: Break down voltage measurement (I_C vs. V_{CE} for 1200 V IGBT)

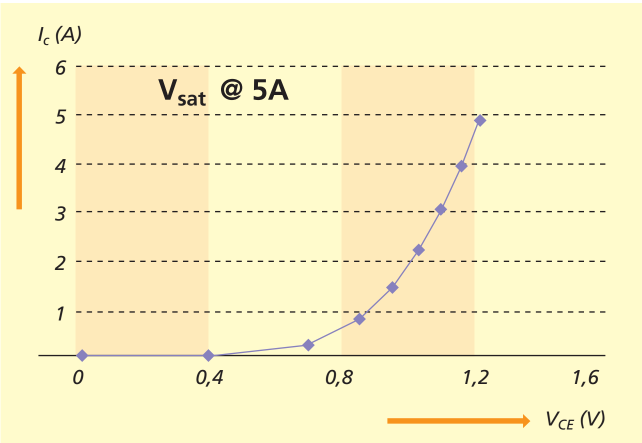


Figure 7: IGBT collector-emitter voltage (V_{ce} (V)) of 1,2 V measured at 5 A on wafer level

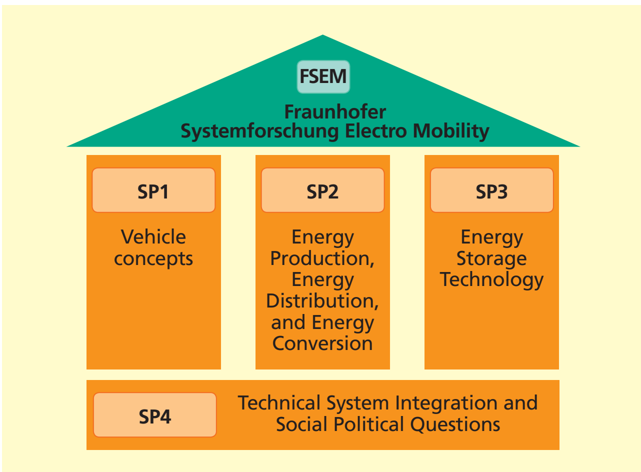
FSEM Project

The development of the RC-IGBT is founded by the federal government project "Fraunhofer Systemforschung Elektro-Mobilität" (FSEM) which is dealing with power electronic and drive technology. As shown in figure 8, the project is focusing on:

- Vehicle concepts (SP1),
- Energy Production, Energy Distribution and Energy Conversion (SP2),
- Energy Storage Technology (SP3), and
- Technical System Integration, Social Political Questions (SP4),

More than 30 Fraunhofer research institutes will bring in their expertise into the project. The Fraunhofer Society and in cooperation with their industrial partners, is convinced that the outcome of the project can be used to aid a sustainable turnabout in direction of electro mobility.

Figure 8: Key aspects of activity within the project of "Fraunhofer Systemforschung Electro Mobility" (FSEM)



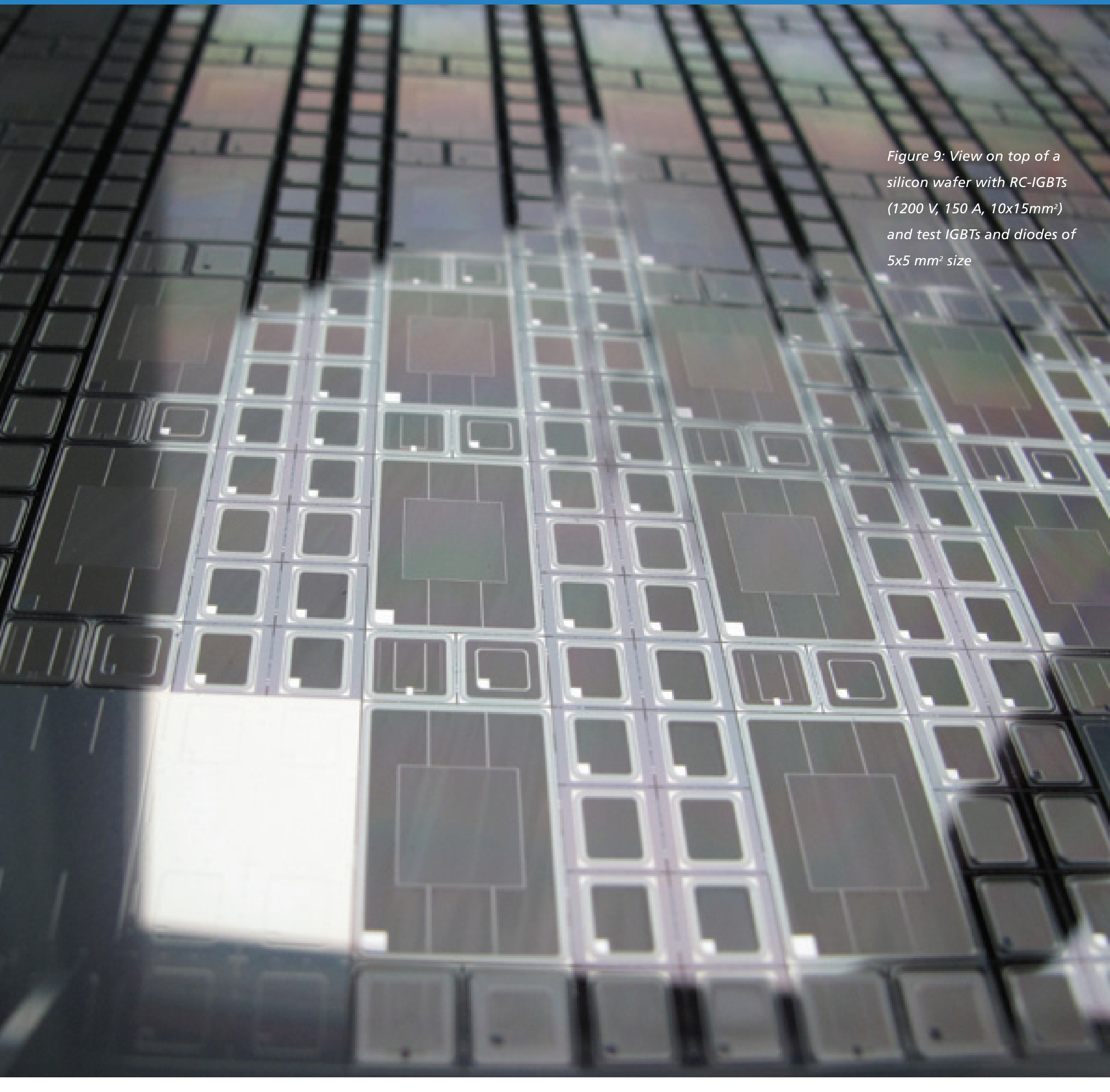


Figure 9: View on top of a silicon wafer with RC-IGBTs (1200 V, 150 A, 10x15mm²) and test IGBTs and diodes of 5x5 mm² size

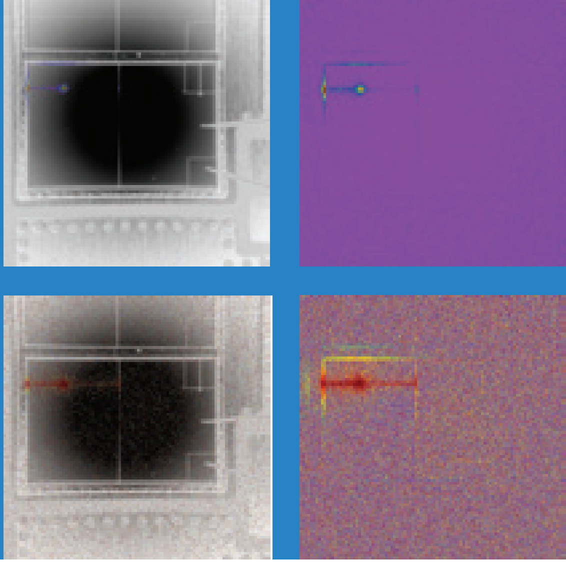


Figure 2: Hot spot detection with lock-in IR thermography: Amplitude and Phase pictures of a power transistor with gate leakage

LOCK-IN IR THERMOGRAPHY FOR FAILURE ANALYSIS OF POWER ELECTRONIC DEVICES

The ISIT IC technology and the power electronics group are investigating new high voltage devices like power diodes, compensation PowerMOS transistors and IGBTs with improved energy efficiency. Defective or low performing power devices often show an anomalous distribution of the local power dissipation (hot spots). This leads to anomalous local temperature increase of the device. For the detection and localization of these defects on wafer level, ISIT built up a lock-in infrared (IR) thermography measurement setup (see figure 1). The system consists of IR camera (detector material: InSb), camera stand, MWIR lenses, 8 inch wafer probe system, computing system, real time measurement software, and voltage sources.

Lock-in thermography (LIT) is a new variant of the well known IR thermography for all applications where the heat of the sample can be pulsed. The lock-in mode enables a much improved signal/noise ratio up to 1000x and a far better lateral resolution down to 5 µm. The temperature resolution of this method is in the range of 10 µK. As a result, locally dissipated power of approx. 1 µW can be detected.
Thus, it replaces hot spot measurements previously carried out using liquid crystals or fluorescent micro thermal imaging. The LIT technique is already an established technique of the non-destructive testing of materials and devices. Its principle consists of introducing periodically modulated heat into an object and monitoring only the periodic surface temperature modulation. The phase is referred to the modulated heat supply. For electronic devices the heat modulation more simply occurs by applying a pulsed bias. The surface temperature is measured with a near infrared camera and the information of each pixel of the incoming images is processed as it was fed into a lock-in amplifier.

Lock-in thermography means that the power dissipated in the object under investigation is periodically amplitude-modulated, the resulting surface temperature modulation is imaged by a thermocamera running with a certain frame rate, and that the generated IR images are digitally processed according to the lock-in principle. Thus, the effect of lock-in thermography is the same as if each pixel of the IR image would be connected with a two-phase lock-in amplifier. Consequently, the two primary results of lock-in thermography are the image of the in-phase signal Sin-phase and that of the out-of-phase signal Sout-of-phase (-90°) (see figure 2). In lock-in thermography often the -90° signal is used instead of the +90° one, since the latter is essentially negative.
From these two signals the image of the phase independent amplitude and the phase image of the surface temperature modulation can easily be derived:

$$\text{amplitude} = \sqrt{\left((S_{\text{in-phase}})^2 + (S_{\text{out-of-phase}})^2 \right)}$$

$$\text{phase} = \arctan\left(S_{\text{out-of-phase}} / S_{\text{in-phase}} \right)$$

It can be very interesting to understand the physical phenomena present in stressful working conditions for power devices, for example at high reverse voltage applied. This is the case of power transistors where the distribution of gate and drain leakage current is an important information in order to improve the process technology and the device layout.
Moreover thermal measurements with lock-in correlation are very helpful to the characterization of power electronic devices to obtain knowledge about the internal physics mechanism and also a suitable method for the failure analysis.
However, up to now this method has rarely been used in the field of power devices.

Figure 1: The lock-in thermography measurement: setup consist of IR camera (b), MWIR lense (d), camera stand (a), x-y-table wafer chuck (c), needle-manipulators (c,e), computing system (f), real time measurement software and voltage source (g)

REPRESENTATIVE RESULTS OF WORK

BIOTECHNICAL MICROSYSTEMS

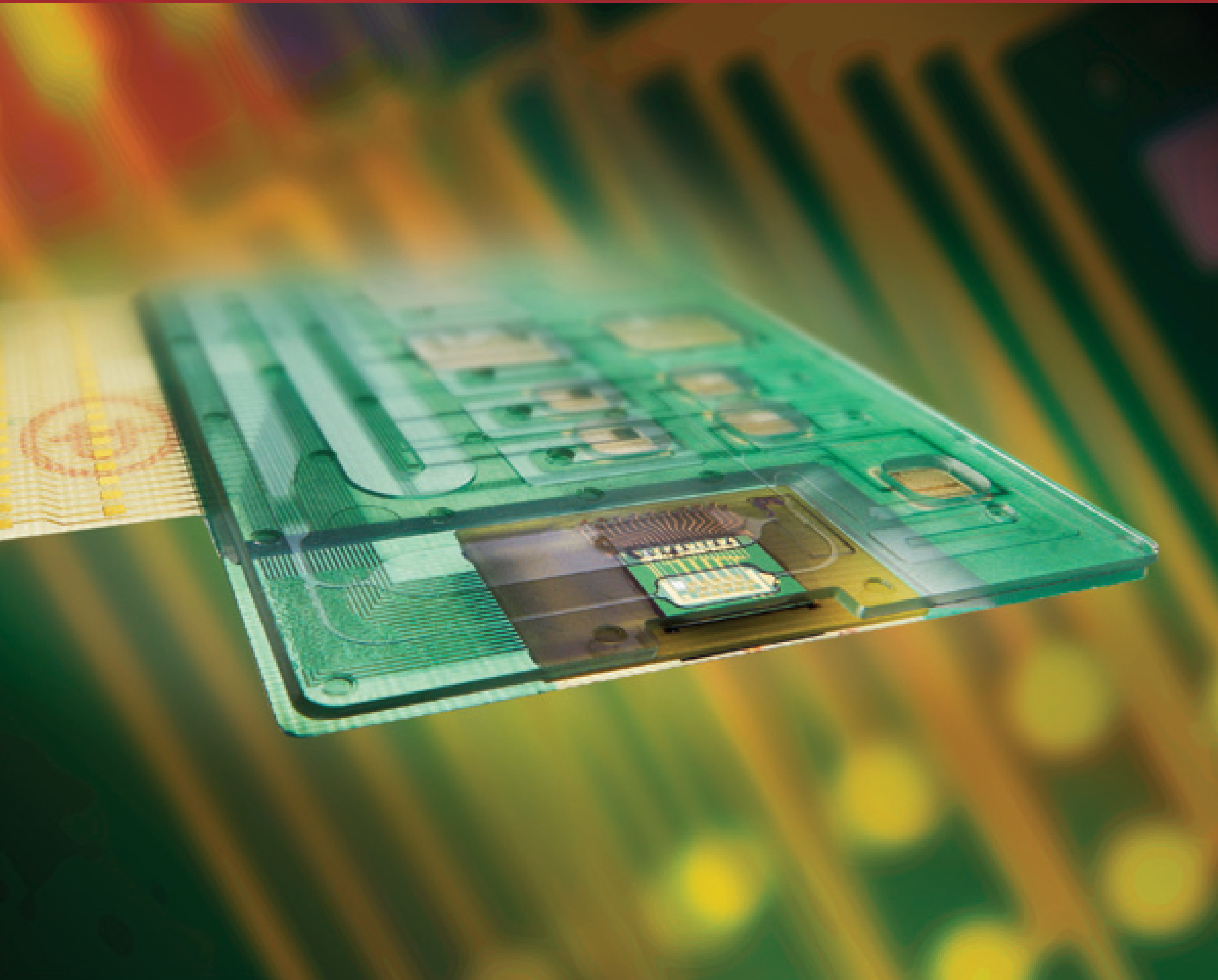


Figure 1: Construction scheme of chromatography chip

CHIP FOR LIQUID CHROMATOGRAPHY

Liquid chromatography with its different separation principles is the most used technique in chemical and biochemical analysis. Typical fields of application in food and medical analysis are the detection of e.g. hormones, antibiotics, mycotoxins, peptides as well as nucleic acids or proteins. Up to now, liquid chromatographs are mainly big laboratory devices. Miniaturized integrated systems for small sample volumes or portable application do not exist. Techniques from microsystem technology have the potential to offer here solutions by allowing the parallel realization of small structures with high reproducibility.

At the department Biotechnical Microsystems new activities are started to develop a chip based miniaturized liquid chromatography system. The work is funded by the BMBF (VDI / VDE) with a project called "MiChroChip" in the frame programme "SIKT 2020-Forschung für Innovationen".

Central feature of the new approach is the construction of a highly porous separation column which will be integrated on wafer level to reach a high chip to chip reproducibility. Aerogel is selected as the material of choice because of its very big surface and high porosity. This will guarantee a good analyte separation capacity for the miniaturized column, comparable to standard ones.

The integration of the separation column requires an adapted chip design, which is the basis for the selection of the further process procedures and process parameters. It is planned, that the integrated chip also provides an analyte detection unit. Based on the working group`s long-time experience with electrical detection on biosensors and the advantage of a high miniaturization potential, it will be done electrochemically by pulsed amperometry. For this, electrodes will be integrated on the chromatography chip. A selection of the appropriate working electrode and reference electrode materials and their sizes has to be evaluated.

For the chip manufacturing a chip design (see figure 1) and technical construction drawings were made. The processing takes place in the ISIT clean room facility, based on 8"-silicon wafer. It is planned that the chromatography chip will consist of a stack of two silicon chips, one layer

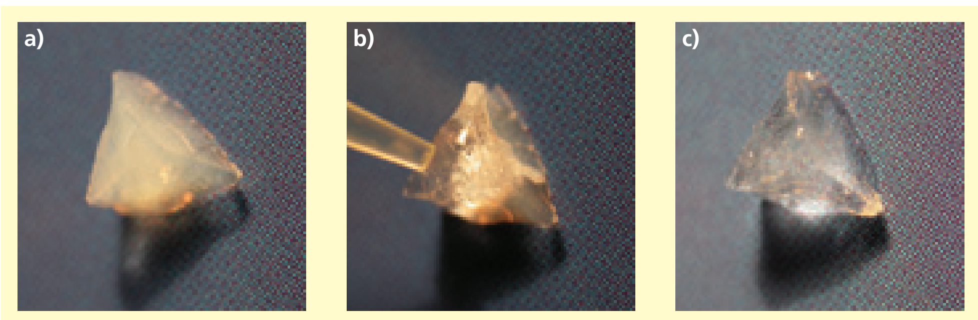


Figure 2:
Rehydration of an aerogel;
a) before rehydration;
b) while rehydration;
c) fully rehydrated

Figure 3

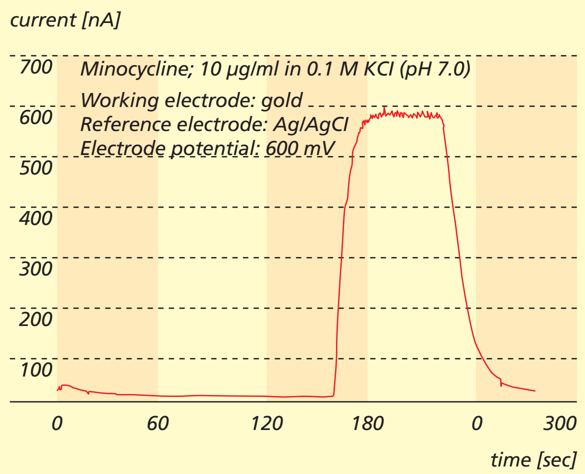


Figure 3: Amperometric signal of the antibiotic minocycline on gold electrode

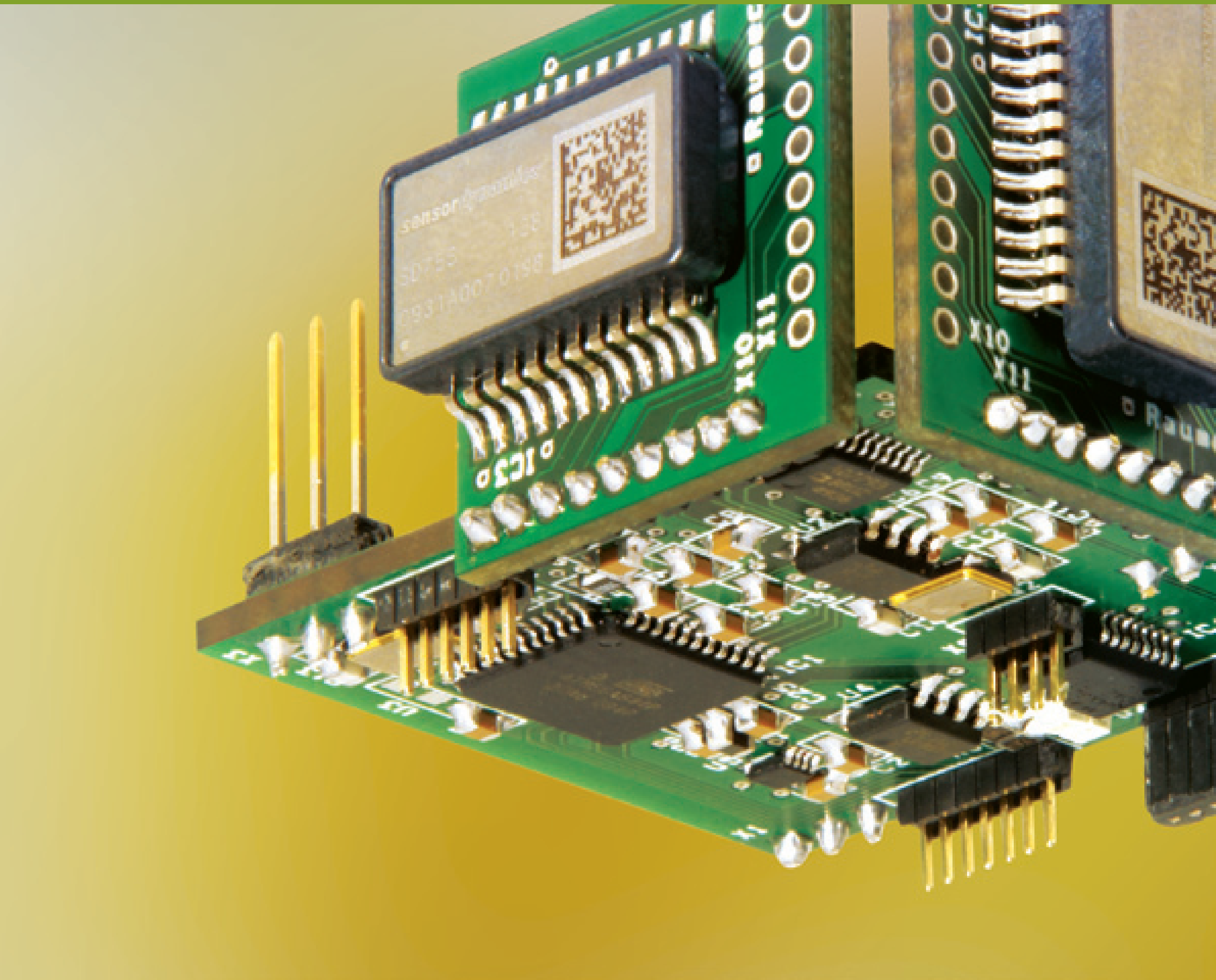
comprising the separation column (manufactured on wafer 1) and one cover layer comprising the electrodes (wafer 2) for the electrochemical detection. The two wafer will be assembled by a bonding process and finally the chromatography chips will be separated via dicing.

Experiments for the optimization of the production process of the aerogel column were carried out. The aerogels were made of TMOS (Tetramethylorthosilicate). The chemistry for hydrogel production was evaluated, including basic as well as acidic hydrolization. The final step in the aerogel production is a supercritical drying step of the hydrogels with liquid CO_2 under pressure in a so called "critical point dryer". The setting parameters of the critical point dryer have to be optimized and adjusted as well. The criteria for final aerogels and their processing are sophisticated.
They have to be stable in size during the manufacturing process, which means no swelling and no shrinking.
Only then the separation channels will be filled completely.
The material must be without stress to prevent cracking.
And as the most severe requirement: they must stand a rehydration. Only few aerogels with a special pore matrix and gel network fulfil this. So, the first experiments were done to find a gel process which results in rehydrable aerogels.

In figure 2 a functional aerogel is shown that stands a rehydration. Here, a piece of aerogel was soaked with several microliters of water without cracking. Additionally the big inner surface of the material gets obvious:
The evaluation of the electrode parameters for the pulsed amperometry was carried out with several substances of the classes of antibiotics (tetracyclines) and of steroid hormones on diamond and gold as working electrode material.
Dependent of the oxidation potential of the substance, different signal heights could be generated. The detection on the diamond surface was more sensitive compared to the Gold surface, because the diamond electrodes had a lower background signal at higher voltages. At the diamond electrodes the measurements could be run at 1400 mV electrode voltage versus Ag/AgCL reference electrode, offering a much better oxidation capacity in comparison to Gold, where the measurements had to be run at 600 - 700 mV versus Ag/AgCl reference electrode. An on-chip iridium oxide reference electrode gave comparable results to the Ag/AgCl reference electrode.

Next steps within the project are the integration of the described components and the realization of functional tests.

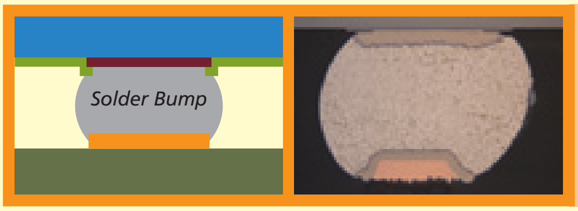
MODULE INTEGRATION



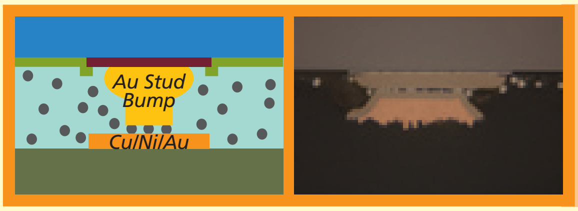
COMPARISON OF FLIP-CHIP TECHNIQUES WITH RESPECT TO RELIABILITY

As part of an engineer thesis different joining techniques (shown in table 1) have been compared with respect to their reliability. Table 2 shows the test matrix of the work. Due to the limited time there was no focus on process optimization, which would increase yield and reliability of each flip-chip technique. Test vehicle was our daisy-chain test chip "FC475 basic" together with NiAu plated FR4 substrates shown in figure 1. At the beginning of the project a number of test boards have been assembled with the different joining techniques. After initial inspection these assemblies have been stressed by temperature-shock cycles, high humidity conditions (85 °C, 85 % rel. hum.), or a pressure cooker test (96 h, 120 °C, 100 % rel. hum.). At all stages of the project the assemblies have been analyzed by electrical tests and cross-section polishing to document aging behavior and failure mechanisms.

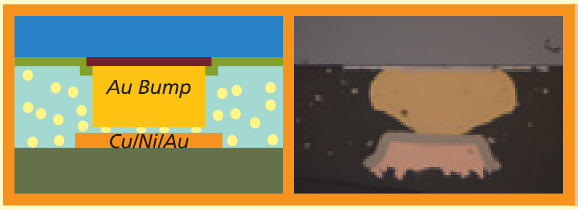
Table 1: Comparison of different flip-chip techniques



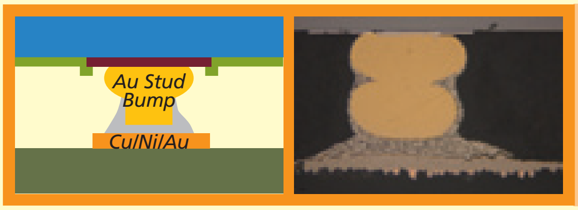
solder flip-chip
- chem. NiAu + solder paste print
  - placement and reflow soldering
  - dispensing of epoxy underfill and oven curing



particle soldering ESC5 (Namics/Panasonic patent)
- stud bump or chem. NiAu
  - temperature and force ramp during placement
  - oven curing
- no underfill required!



anisotropic conductive gluing ACA / ACF
- stud bump or chem. NiAu
  - temperature und force ramp during placement
  - oven curing
- no underfill required!



conductive gluing – stud bump bond (SBB) process
- high (double) stud bumps, pitch > 150 µm
  - placement and oven curing
  - dispensing of epoxy underfill and oven curing

Table 2: Test matrix with different joining techniques and bump types

	ESC5, SnBi	ESC5, SnAGCu	ACA	silver epoxy (ICA)
10µ Ni/Au	Panasonic NM-SB 50A	Panasonic NM-SB 50A		
20µ NI/Au	Panasonic NM-SB 50A	Panasonic NM-SB 50A		
single stud bumps coined 35 µm	Panasonic NM-SB 50A	Fineplacer (manual assembly)	Panasonic NM-SB 50A	Datacom apm 2200
double stud bumps coined 70 µm				Datacom apm 2200
stud bumps not coined				Datacom apm 2200

	SnAGCu	SnPb		
solder bumps	Datacom apm 2200	Datacom apm 2200		

Common flip-chip joining techniques

The majority of the world wide assembled integrated circuits are housed in a plastic or ceramic package to ease automated chip handling and printed circuit board (PCB) design. Nevertheless, some applications require the handling of bare dies. The reasons are usually the requirement to save space or to save the money for the package in very high volume applications. In both cases the common approach consists of backside mounting of the chip, wire bonding, and glop top encapsulation. This way is well approved and very reliable. However, much lateral space is required to place the wire bonds. In cases where the space is very limited an alternative approach is used: The chip is equipped with appropriate bumps which are directly connected to the substrate. Since the chip is placed top down onto the substrate this technique is called flip-chip mounting. Depending on the application a large variety of different methods are applied to connect the flip-chip to the substrate. Each of them has its own advantages and disadvantages, which will be discussed in detail in the following paragraphs. Subsequently, experimental results of reliability tests will be shown, comparing the different flip-chip techniques to each other.

Solder flip-chip

Usually, the pads of integrated circuits consist of Aluminum which can not be soldered in a convenient way. In case the pad layout is well suited for a solder flip-chip process, i.e. the pitch is large enough, a maskless chemical deposition of Nickel and Gold can be used to create solderable bumps. If this is not the case, wafer processing techniques are applied to create a redistributed pad layout with a solderable under bump metallization. In the next step solder has to be applied. Depending on the contact pitch different techniques are used: For fine-pitch applications the solder can only be applied by electroplating, which may be a pure Tin bump or a Copper bump with a Tin cap. If the pitch is a little bit larger, solder paste printing can be used as it was the case in this project. In applications with very large pad distances, e.g. 500 µm, discrete solder balls can be placed onto the pads, enabling standard SMD placement of the resulting components, i.e. placing of the balls into printed solder paste. For small pitch applications the bumps are dipped into a tacky flux film before they are placed onto the circuit board. After reflow, epoxy underfill is dispensed and cured in an oven to improve the mechanical stability of the connection.

Particle soldering and anisotropic conductive adhesive

The connection between liquid crystal displays (LCD) and the flexible PCB used to connect the device is often realized by anisotropic conductive gluing. This special adhesive, which can also be used for flip-chip applications, consists of a non conductive adhesive matrix with distributed conductive particles. Usually, the distance between the particles is large enough to prevent any current flow. However, particles will be squeezed between elevated bump areas and opposed circuit paths. For flip-chip applications typically stud bumps are used, but electroplated Gold bumps or high chemical Nickel Gold bumps are also common. The material of the conductive particles varies from adhesive to adhesive. Gold coated Nickel particle are as well spread as metalized plastic particles.
A special variant patented by Namics and Panasonic is called ESC5 process. In this case the conductive particles consist of solder which melts during the joining process.

The joining process starts with the dispensing of anisotropic conductive paste (ACP) or placement of anisotropic conductive film (ACF). Then the die is placed into the adhesive. For this step a controlled force and heat ramp is required, which makes the process much slower than the alternative approaches discussed in this article. Depending on the adhesive a final oven curing, usually again with some applied pressure, is necessary.

Conductive Gluing

Isotropic conductive adhesive offers an additional way to connect flip-chip devices as long as the pitch is at least 150 µm. The process flow is quite similar to the joining of solder flip-chips. A flip-chip bonder is used to dip the bumps on to a film of silver epoxy. Afterwards the chip is placed on the substrate, followed by an oven curing. Finally an epoxy underfill is dispensed and cured in an oven. Similar to the other adhesive processes a variety of bumps can be used. Since the process is commonly used for prototyping or low volume production, stud bumps are very common.
For this reason the process is also known as stud bump bond (SBB) process.

Experiments and Results

The temperature shock reliability was definitely the best for the isotropic conductive adhesive, followed by conventional solder bumps. The good reliability of the adhesive could be explained by the softness of the Silver epoxy compared to solder. It is well known that a soft bump has a better temperature shock reliability than a hard one.
The difference between the SnPb and SnAgPb solder bumps can be explained by the different solder height, since the mechanical stress is decreased with increasing solder height. Therefore the influence of the alloy can not be seen from this experiment.

The anisotropic conductive adhesive and ESC5 connections have proven to be less reliable under temperature shock conditions. Probably that is the reason why these techniques are often used in consumer products where temperature shock is no issue.

As expected the solder bumps have not been affected by high humidity conditions, i.e. 85 °C 85 % rel. humidity, or even 120 °C 100 % rel. humidity (pressure cooker test). The isotropic conductive adhesive performed also quite well under high humidity conditions but failed during the pressure cooker test. The reason for this behavior is quite unclear since the cross-section polish was quite inconspicuous. Probably a change of the underfill material may solve the issue.
The ESC5 connection performed all very well under high humidity and pressure cooker conditions whereas the ACA connection failed during the pressure cooker test due to degradation of the epoxy resin (chips drop off).

Conclusion

Each joining technique has its own advantages and disadvantages. None of the techniques is perfect in every situation, but each solution has its own range of applications where it is a good choice. Quite good reliability could be

Figure 1: Test chip FC475 and corresponding FR4 substrates

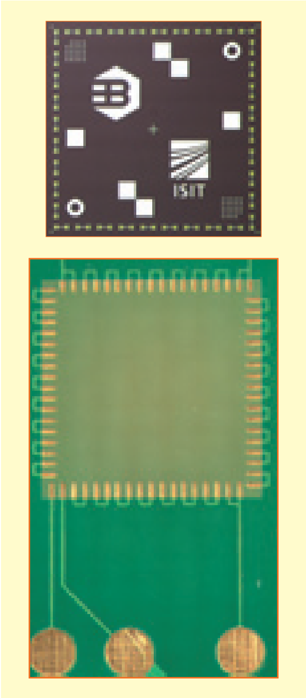
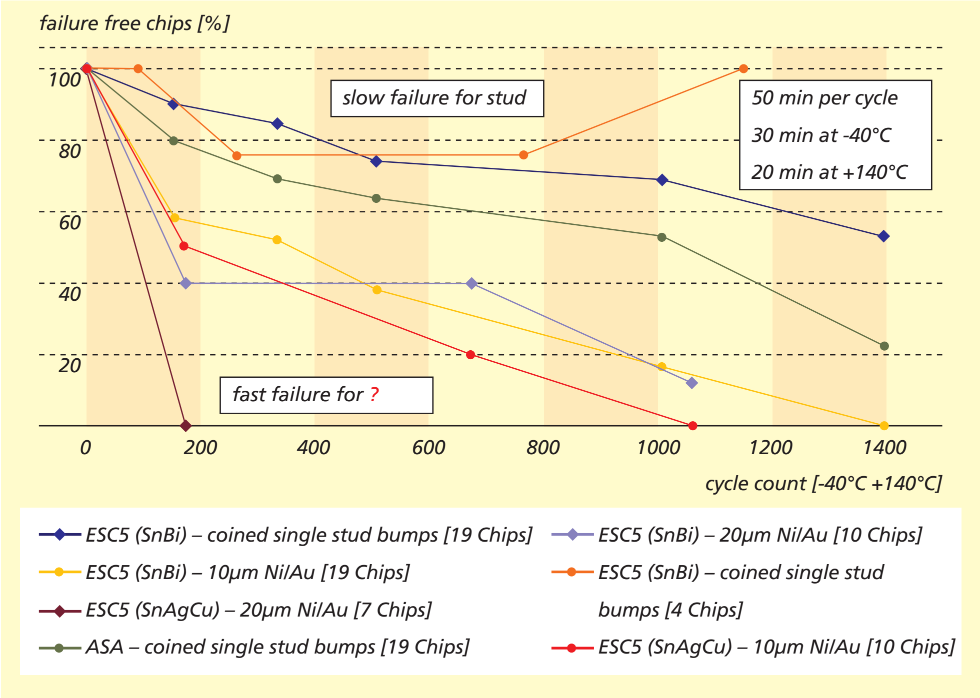


Figure 2: Shock test results for ESC5 and ACA

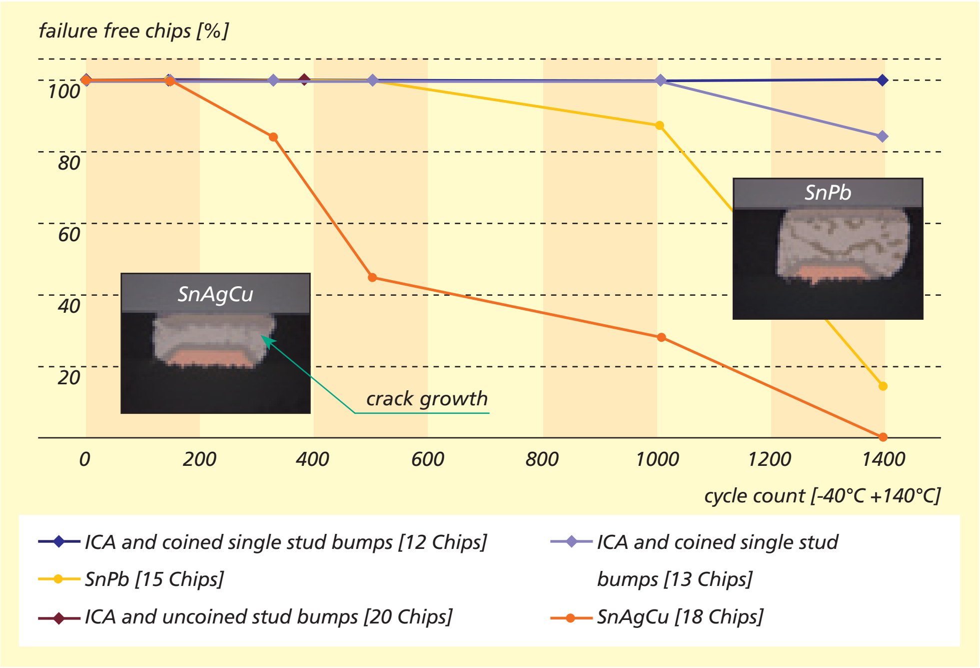


reached with large solder balls. Isotropic conductive gluing suffers from a small process window, but is very reliable under temperature shock and mild humidity conditions. For fine-pitch applications ESC5 and ACA connections are well suited since bridging effects can be neglected as long as the chip placement has been done properly. An alternative solution for fine-pitch applications are Copper pillar bumps which has not been investigated in this project. Since the Copper is quite hard compared to Gold this connection could be expected to be sensible for temperature shock but reliable under humidity conditions.

Outlook

The tests performed in this investigation have been made under storage conditions, i.e. without any applied voltage. At least for the high humidity test we would expect some effect of electric fields. Therefore a new test-chip design "FC475DDC" has been developed with two interlaced daisy chains (see figure 6). With this new design a voltage could be applied between each adjacent contact. Furthermore the contact resistance of selected bumps could be measured in 4 point geometry.

Figure 3: Shock test results for isotropic conductive adhesive (ICA) and solder bumps



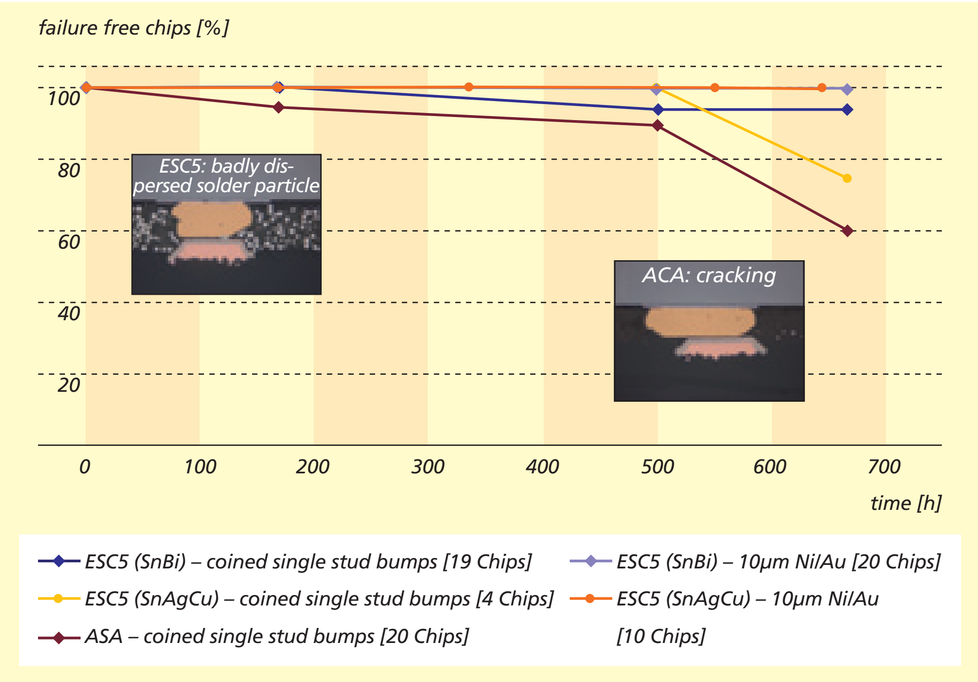


Figure 4: Heat and humidity test results (85 °C / 85 % rel. hum.) for ESC5 and ACA

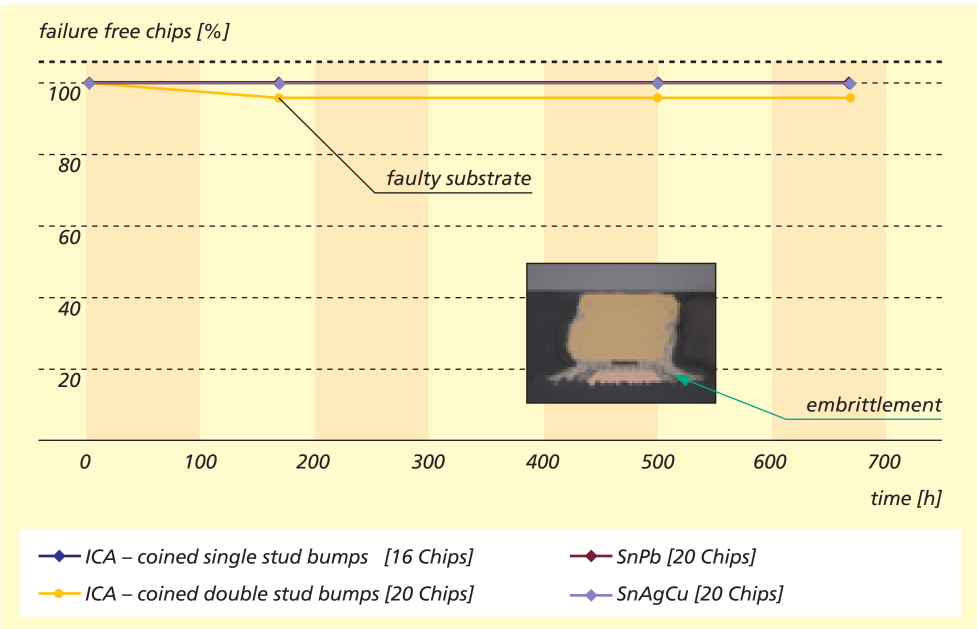


Figure 5: Heat and humidity test results (85 °C / 85 % rel. hum.) for isotropic conductive adhesive (ICA) and solder bumps

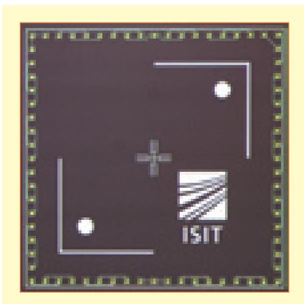


Figure 6: New testchip Design FC 475 DDC with two interlaced daisy chains

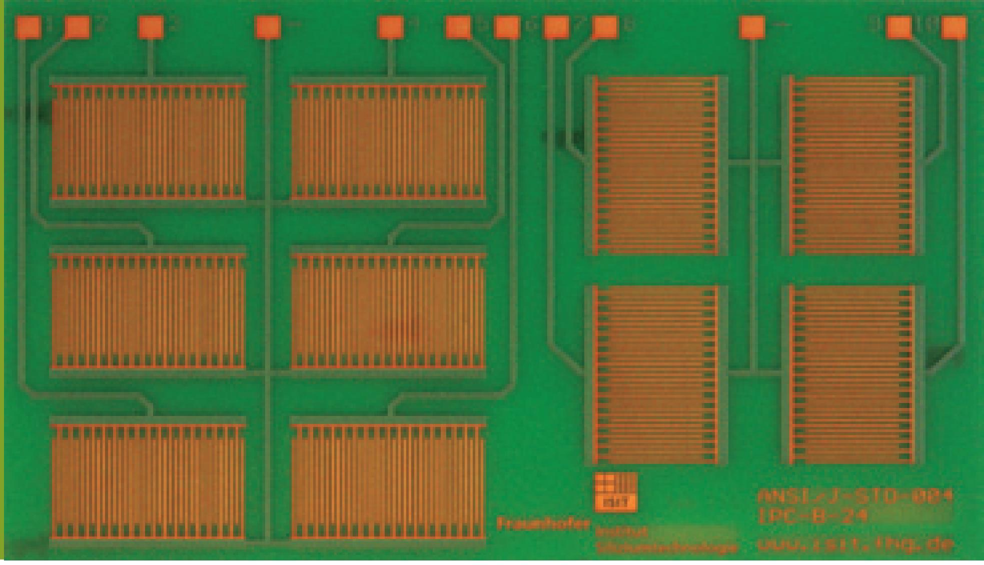


Figure 1: ISIT test board with 10 comb patterns for SIR-measurements

MEASUREMENT SETUP FOR SURFACE INSULATION RESISTANCE

During a diploma thesis a new setup for surface insulation resistance (SIR) tests was developed at Fraunhofer ISIT. With this test, the resistance between two adjacent tracks on a printed circuit board (PCB) is measured. Due to high resistances between these tracks, very long tracks on the PCB or special patterns are required to achieve accurate measurement results. For this purpose comb patterns (figure 1) are suitable. The test is used to analyze the impact of materials like flux, solder and encapsulants or whole process steps like cleaning processes on the insulation resistance.

For the measurement there are two different methods. On the one hand, a constant current is applied to the test pattern. In this case the voltage across the pattern is measured. The other way is to apply a constant voltage to the test pattern and to measure the resulting current through it. For both methods the insulation resistance can be calculated by Ohm's law. Different voltages applied to the test pattern can result in different appearances of dynamic migration between two conductors. A higher voltage can affect a faster dendrite growth and thus the test pattern can faster be shorted by the dendrite. Because of this voltage dependency, the method based on a constant voltage applied to the pattern is used for the test setup. This allows a better comparison between multiple measurements made with a certain voltage.

One of the main components of the test setup is a switching unit. Because of a long test duration, generally one week, as many patterns as possible should be tested within one test run. The switching unit is used to select one test pattern after the other for measuring and can handle up to 80 test patterns (channels). In addition to the voltage applied to the test pattern during measurement, another voltage to polarize can be applied to the pattern between two measurements. The acquisition of resistances up to some Teraohms requires very precise measurements of the resulting current through the test patterns. Hence leakage currents in the test setup have to be avoided and only components with high insulating properties are used, especially for the switching unit. The switching mechanism for each channel consists of two highly insulating reed relays. One relay to connect the pattern to the measurement path and the other to connect it to the polarization path. To connect the pattern to the switching unit, shielded coaxial cables are used. The unit, particularly the relays, is controlled by a microcontroller.

A special program on a windows PC controls the whole test setup. The PC is connected to the switching unit via the serial port (rs232). A Keithley 617 electrometer and an additional voltage source are attached to the PC using the GPIB-BUS to apply the voltages and to acquire the measurement data. The program can manage the test parameters e.g. number of channels, interval between measurements, voltages for test and polarization and test duration. The measured data are stored and also charted by the program.

For a SIR-test the test patterns are soldered to the coaxial cables and are placed in a climate chamber. Typical test parameters for the climate chamber are e.g. 85 °C and 85 % relative humidity or 40 °C and 92% relative humidity. The resistance is measured e.g. each hour for a period of one

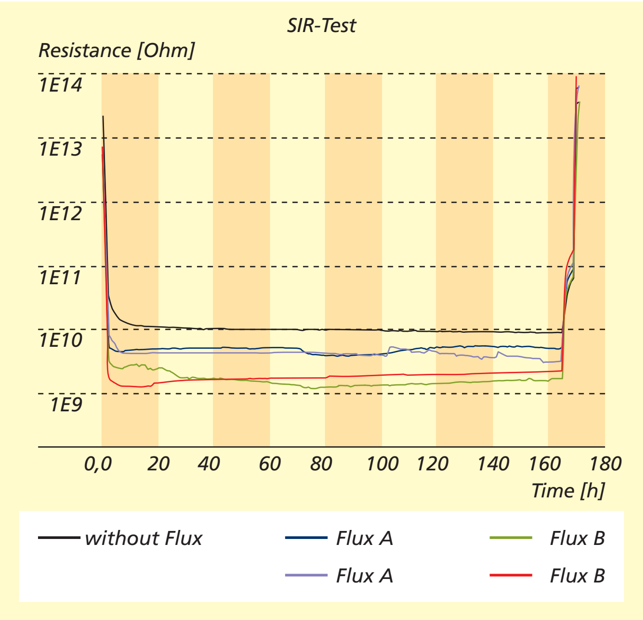


Figure 2: Diagram with test data for two different fluxes. Higher resistances at the beginning and at the end of test because of lower humidity in the climate chamber

week. Shorter intervals between measurements for a higher resolution are possible, too. Before and after the test initial measurements are made at room temperature and lower humidity (e.g. 30 % rel. humidity).

The new measurement setup allows the simultaneous measurement of 80 insulation resistances up to the range of Teraohms during one test run. The software specially developed for this test simplifies the test setup and data management by a graphical user interface.

These SIR-tests are accomplished according to IPC-TM-650 or DIN EN/ISO 9455-17 and are performed as service for the industry.

INTEGRATED POWER SYSTEMS

Figure 1: Coating head of the coater with the detached traversing unit (in the background) for determining the coating weight

Figure 2: A full view of the coating facility for electrode and separator foils

INSTALLATION OF A STATE-OF-THE-ART ELECTRODE FOIL COATING LINE FOR RECHARGEABLE LITHIUM-BATTERIES AT ISIT

The group of Integrated Power Systems (IPS) has been active for over 10 years in developing rechargeable lithium polymer batteries with an emphasis on special user-specific needs. The development work necessary for optimizing electrochemically active foils are first carried out at the laboratory scale.
The electrochemical characterization of the electrode foils are initially done in half-cells. Next, small and scalable full-cells are made to determine the properties of the full system consisting of the anode, cathode, separator and electrolyte. For the final testing, small lots of prototypes in the format required by the customers are produced and examined according to the pre-defined specifications.

The recent developments in the areas of electro-mobility and energy storage solutions for renewable energy sources have placed strong demands for batteries with bigger energy density. The cell formats typically required in projects range from 150 - 400 cm^2 in area with a cell capacity of 5 to 40 Ah per cell. Typical numbers of such cells produced achieve the two-digit range in order to assemble modular batteries with several cells per module. The accompanying demands cannot be met with simple laboratory set-ups for preparing electrode foils.

This discrepancy between the necessity for research-oriented development of laboratory-scale foil recipes on the one hand and the necessity to meet the needs of partners requiring larger cells in higher quantity on the other hand has up to now been a gap in the R&D portfolio of services offered at ISIT and the entire Fraunhofer-Gesellschaft.

Through the acquisition of a roll-to-roll coating line for the production of electrochemically active foils, the ISIT coating center (Beschichtungstechnikum) will be able to prepare well-defined electrode foils in larger amounts up to several hundred meters per coil, thus addressing the new challenges.
The conception, planning, and construction of the coating line and associated periphery were initiated by the release of additional funds from the "Konjunkturpaket 1" (economic stimulation package 1) of November 2008 and was transferred to the implementing phase in May 2009 through commissioning the construction of the coating facility.

Since November 2010 the coating line is in the initial operation phase.

Components of the coating facility

The coating facility (figure 2) consists of three key parts:

- The coating head for precise deposition of the slurry on the carrier foil
- The modular drying line for solvent removing
- The foil calendaring and processing unit

The coating head

Different applications call for both, high specific power and high specific energy lithium ion battery (LIB) type cells. This has to be taken into account during the conception of LIBs. Therefore electrode foils with different capicity load are required. Different coating heads are available which allow continuous adjustment of the coating width, which is of special significance to the individualized test cell construction as well as considering different rheological properties of the slurry.

With the currently installed coating blade system, which has a variable gap thickness, it is possible to prepare foils

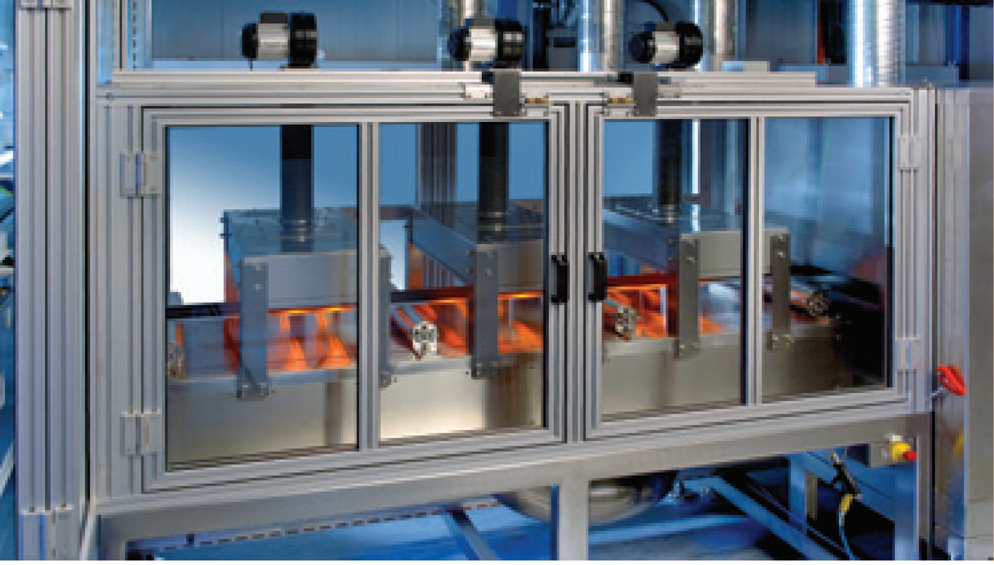


Figure 3: Inline infrared unit for preliminary drying of coated foil strip

with a wet-coat thickness of up to 600 µm. A traversing unit for measuring coating surface weight, which is located immediately behind the coating head and makes contact-free measurements, admits the rapid evaluation of the coating parameters selected, thus enabling fast adjustments without significant material loss. In addition to the continuous coating of substrates, the coating head also allows the intermittent coating with a specifically adjustable geometry. This increases the flexibility in the configuration of the cell geometry and provides the possibility of foil production for rounded cells.

The throughput of the coater is determined by the coating thickness and the material web speed. The coating facility has rollers with a width of 500 mm, which permits a maximum coating width of 400 mm. The foils can be rolled out at a speed of 0.5 to 5 m/min in a continuous manner.

In order to ensure the flexibility required for R&D, the facility is equipped for the usage of different solvents such as acetone, N-methyl-pyrrolidone (NMP) and water. The configuration of the equipment not only takes into consideration the basic properties of the solvents (boiling point, viscosity, condensation, etc.) and the chemical compatibility of the materials, but also factors influencing on the drying process, the VOC (volatile organic compounds) monitoring, as well as substrate handling.

Drying unit

The drying of the foils is carried out in a 3-step process in modules which are independently regulated. An initial infrared drying process (figure 3) is followed by a 2-step hot air drying. The required reproducibility of the coating calls for constant an stable air conditioning. The air conditioner dehumidifies the ambient air to less than 4 g/m^3 and feeds it to the drying zones. Through an external post-drying process, the remaining solvent traces can be removed from the coatings as required. For temporary storage of the foil rolls, possibilities to store them under inert gas conditions have been installed.

Foil processing

In addition to their chemical composition, the morphology of the foils is of great importance in determining their quality. The suitable adjustment of the porosity of the foil, for example, supports the transport and proper distribution of the liquid electrolyte, which is added in a later step during cell production.

The porosity of the dry foils can be set to a defined level by a heatable calender with a maximum force of 40 tons (figure 4). Further inline components are the edge cutter tool and a traversing dry coat thickness sensor which can accurately determine the thickness of different substrate materials and coatings via its double-sided laser distance measurement.

A laboratory environment that is tailored to the requirements of the coater allows the preparation of the necessary slurries directly on location. Storage for air sensitive solids materials and different solvents, solvent filling facilities and accompanying infrastructure have been set up as individual solutions in addition to an IT system for data acquisition.

Figure 4: Final inline foil processing (after the drying stretch) consisting of calendaring unit, dry coat thickness sensor and edge cutting tool

Results

The first experiments have shown the feasibility of good-precision direct coating of NMP-based suspensions on to aluminium substrates. The electrode foils could afterwards be coated on the backside with the same surface load as on the top-side, as evident from the data of the inline sensors.

First half-cells in which these electrode foils had been tested show the expected behavior. An acetone-based slurry recipe with $Li_4Ti_5O_{12}$ as active material shows a good cycle stability in half-cells at 1C charge and discharge rates (figure 6). This marked the starting point of R&D activities in developing complete electrode foils in the ISIT coating facility.

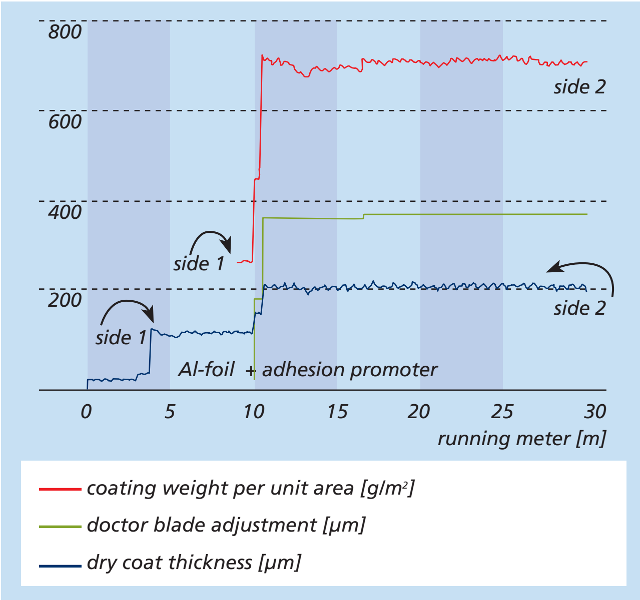


Figure 5: Coating result of a double-sided coating with a NMP based test slurry. The data from the inline sensors show the profiles along the length of the electrode foil

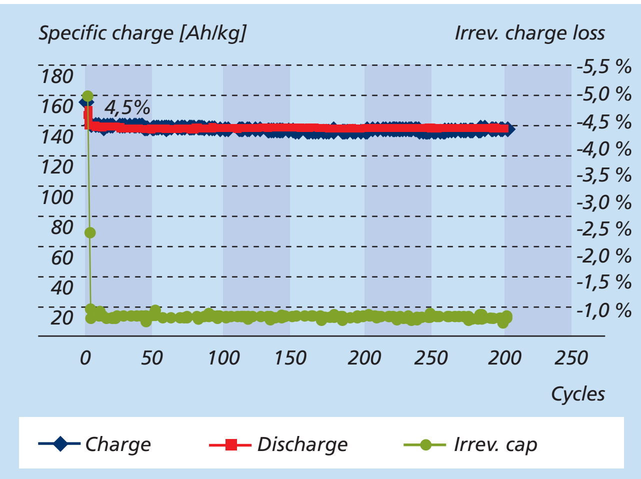


Figure 6: Test cell characteristics of a half-cell with a $Li_4Ti_5O_{12}$ anode foil from the new coating facility showing good cycle stability at 1C (100 % DOD)

IMPORTANT NAMES, DATA, EVENTS

LECTURING ASSIGNMENTS AT UNIVERSITIES

W. Benecke
Lehrstuhl Technologie Silizium-basierter Mikro- und Nanosysteme, Technische Fakultät, Christian-Albrechts-Universität, Kiel

R. Dudde
Mikrotechnologien (8168), Fachbereich Technik, FH Westküste, Heide

O. Schwarzelbach
Mikroelektromechanische Systeme (MEMS), Institut für elektrische Messtechnik und Mess-Signalverarbeitung, Technische Universtität Graz, Austria

B. Wagner
Lehrstuhl Prozesse und Materialien der Nanosystemtechnik, Micro- and Nanosystem Technology I and II, Technische Fakultät, Christian-Albrechts-Universität zu Kiel

MEMBERSHIPS IN COORDINATION BOARDS AND COMMITTEES

R. Dudde
Coordinator of KLSH Kompetenzzentrum Leistungselektronik Schleswig-Holstein

D. Friedrich
Coordinator of KLSH Kompetenzzentrum Leistungselektronik Schleswig-Holstein

P. Gulde
Member of Allianz Energie of the Fraunhofer-Gesellschaft

J. Janes
Member at MEMUNITY, The MEMS Test Community

T. Knieling
Member of Organic Electronics Association (OE-A)

T. Knieling
Member of Gesellschaft für Korrosionsschutz (GfKorr)

T. Knieling
Member of ZVEI – AK Zuverlässigkeit von Leiterplatten

T. Knieling
Member of Netzwerk organische Elektronik Nord

P. Merz
Member of MEMS Executive Congress Steering Committee

R. Mörtel
Member of Forschungsgemeinschaft Erneuerbare Energien (FEE)

R. Mörtel
Innovations-Allianz Elektromobilität: National Technology Roadmap Lithium-Ion-Batteries 2030

K. Pape
Member of BVS, Bonn

K. Pape
Member of FED

K. Pape
Member of VDI

M.-H. Poech
Mitarbeit im Arbeitskreis "Zuverlässigkeit, bleifreie Systeme" des Fraunhofer IZM

M.-H. Poech
Member of Arbeitskreis "Voids" of Fraunhofer IZM

W. Reinert
Member of Arbeitskreis A2.6, "Waferbonden", DVS

W. Reinert
Member of Technical Committee of Electronics Packaging Technology Conference (EPTC)-Singapore

W. Reinert
Member of Technical Committee of Conference Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP)

M. Reiter
Member of "Arbeitskreis Bleifreie Verbindungstechnik in der Elektronik"

H. Schimanski
Member of VDE / VDI Arbeitskreis „Prüftechniken in der Elektronik-produktion"

H. Schimanski
ZVEI Fachverband Arbeitsgruppe „Zuverlässigkeit von Leiterplatten"

H. Schimanski
Member of VDI Fachausschuss Assembly Test, VDI, Frankfurt

H. Schimanski
Member of ZVEI Ad-hoc Arbeitskreis "Repair und Rework von elektronischen Baugruppen"

H. Schimanski
Member of DVS Fachausschuss Löten

H. Schimanski
Member of Hamburger Lötzirkel

B. Wagner
Member of GMM-Fachausschuss 4.1 „Grundsatzfragen der Mikrosystemtechnik und Nanotechnologie", VDE / VDI-Gesellschaft für Mikroelektronik, Mikro- und Feinwerktechnik

COOPERATION WITH INSTITUTES AND UNIVERSITIES

C. Wijayawardhana
Member of The Electrochemical Society

A. Würsig
Member of AGEF (Arbeitsgemeinschaft Elektrochemischer Forschungsinstitutionen e. V.)

A. Würsig
Member of Netzwerk „Elektrochemie" of the Fraunhofer- Gesellschaft

G. Zwicker
Head of Fachgruppe Planarisierung / Fachausschuss Verfahren / Fachbereich Halbleitertechnologie und –fertigung der GMM des VDE/VDI

G. Zwicker
Member of International Executive Committee of International Conference on Planarization/CMP Technology (ICPT)

RWTH Aachen Universität, *Aachen*

RWTH Aachen Universitätsklinik, *Aachen*

Centro National Microelectronics, *Barcelona, Spain*

Universitätsklinik Essen, Abt. für Urologie und Uro-Onkologie, Robert-Koch-Insititut (RKI), *Berlin*

Slovac Academy of Sciences, *Bratislava, Slovakia*

University of Cardiff, *Great Britain*

Fachhochschule Vorarlberg Dornbirn, *Austria*

Technische Universität Dresden, Institut für Aufbau- und Verbindungstechnik, *Dresden*

Technische Universität Dresden, Institut für Halbleiter- und Mikrosystemtechnik

Technische Universität, *Eindhoven, Netherlands*

VTT, Espoo, *Finland*

University of Exeter, *Great Britain*

Fachhochschule Flensburg

LETI, CEA (Commissariat à L'Energie Atomique), *Grenoble, France*

LITEN, CEA (Commissariat à L'Energie Atomique) *Grenoble, France*

Hochschule für Angewandte Wissenschaften, *Hamburg*

Technion, *Haifa, Israel*

Universität Hamburg

Helmut-Schmidt-Universität *Hamburg*

TUHH Technische Universität *Hamburg Harburg*

Fachhochschule Westküste, *Heide*

Technische Universität, *Ilmenau*

Christian-Albrechts-Universität, Technische Fakultät, *Kiel*

Fachhochschule *Kiel*

IMEC, *Leuven, Belgium*

IEMN, *Lille, France*

Fachhochschule Lübeck

DLR, *München*

Westfälische Wilhelms-Universität, *Münster*

Sintef ICT, *Oslo, Norway*

University of Oulu, *Finland*

École Polytechnique, *Paris, France*

University of Perugia, *Italy*

University of Pisa, *Italy*

Süddänische Universität, *Sonderburg, Denmark*

IMS Chips, *Stuttgart*

VTT, Technical Research Center of Finland, *Tampere, Finland*

FBK, Trento, *Italy*

Fachhochschule Wedel

Institut für Polymertechnologien, *Wismar*

DISTINCTIONS

Benjamin Karstens
Distinction of being best apprentice as „Werkstoff-prüfer - Halbleitertechnik“ at IHK Kiel for which he was awarded by the Fraunhofer-Gesellschaft, München,

November 22, 2010

TRADE FAIRS AND EXHIBITIONS

International Rechargeable Battery Exposition
March 2 – 5, 2010,
Tokio, Japan

SID-ME Chapter Spring Meeting 2010
Society for Information Display, March 18 – 19, 2010, Dresden

Analytica
22. International Trade Fair for Laboratory Technology, Analyses, Biotechnology and Analytica
March 23 – 26, 2010,
München

Hannover-Messe Industrie 2010
April 19 – 23, 2010,
Hannover

PCIM 2010
International Exhibition & Conference, Power Conversion Intelligent Motion,
May 4 – 6, 2010, Nürnberg

SMT 2010
Hybrid Packaging System Integration in Micro Electronics,
June 8. – 10, 2010, Nürnberg

SMM Hamburg
(in cooperation with TIETEK-project partners)
September 7 – 10, 2010,
Hamburg

WindEnergy 2010
September 21 – 23, 2010,
Husum

electronica 2010
24. International Trade Fair for Components, Systems and Applications in Electronics,
November 9 – 12, 2010,
München

Vision 10
24. International Trade Fair for Machine Vision,
November 9 – 11, 2010,
Stuttgart

MISCELLANEOUS EVENTS

Aspekte moderner Siliziumtechnologie
Public lectures, monthly presentations, Fraunhofer ISIT, Itzehoe

Die beherrschbare Baugruppenfertigung
Seminar: February 10 – 12 and October 27 – 29, 2010, Fraunhofer ISIT, Itzehoe

Zerstörungsfreie Prüftechnik, Technologietag
Seminar: March 03,2010, Fraunhofer ISIT, Itzehoe

ISIT-Presentation in the framework of „Forschung erforschen – die Innovationstour der Metropol-IHKs", *organized by IHK Schleswig-Holstein, April 20, 2010, ISIT Itzehoe*

Treffen des Hamburger Lötzirkels
April 20,2010, Fraunhofer ISIT, Itzehoe

24. CMP Users Meeting
April 30, 2010, CEA-Leti, Grenoble, France

GMM Diskussionstagung, Fachgruppe 4.9 ‚Entwurf von Mikrosystemen'
May 02,2010, ISIT, Itzehoe

Kompetenzzentrum Leistungselektronik Schleswig-Holstein *Second workshop. June 1, 2010, Fraunhofer ISIT, Itzehoe*

Treffen der FED Regionalgruppe Hamburg
June 16,2010, Fraunhofer ISIT, Itzehoe

ISIT Presentation in framework of „Macht mit bei Mint – Zukunftsberufe für Frauen"
Information day for schoolgirls, initiated by Volkshochschulen Kreis Steinburg, July 6, 2010, Fraunhofer ISIT, Itzehoe

Kommission Elektromobilität
Wirtschaftsrat Deutschland der CDU, August 30, 2010, Fraunhofer ISIT, Itzehoe

ISIT Presentation in framework of "Science Summer School Itzehoe", *initiated by Hightech Itzehoe, September 10, 2010, Fraunhofer ISIT, Itzehoe*

25. CMP Users Meeting
October 22, 2010, Technical University Dresden

Neue Meilensteine zur Akkumulatorentwicklung in Itzehoe
Festive event on the occasion of start up the new ISIT coating center and the settlement of Dispatch Energy Innovations next to Fraunhofer ISIT, Speaker: Jost de Jager, Minister for Economic Affairs in Schleswig-Holstein, November 5, 2010, Dispatch Energy Innovations, Itzehoe

Praxisorientierte Prozessoptimierung in der elektronischen Baugruppenfertigung
Seminar, Nov. 15 - 19, 2010, Fraunhofer ISIT, Itzehoe

Der optimierte Rework-Prozess
Seminar: November 24 - November 26, 2010, Fraunhofer ISIT, Itzehoe

DOCTORAL THESES

Stephan Warnat
Technologies for the integration of Through Silicon Vias in MEMS packages. Christian-Albrechts-Universität zu Kiel, December 2009

DIPLOMA, MASTER'S AND BACHELOR'S THESES

Thorsten Giese
Entwicklung einer FPGA-basierten Signalprozessierung zur Auswertung von mikromechanischen Sensoren. Diploma thesis, FH HAW Hamburg, January 2010

Florian Grabbe
Hardware-Software-Co-Design zur Ansteuerung eines Laserprojektions-Displays. Bachelor's thesis, FH Wedel, September 2010

Shanshan Gu
Entwurf einer integrierbaren, flexiblen Kapazitäts-Spannungs-Wandlerschaltung für die Auswertung von mikromechanischen Sensoren und Aktuatoren. Diploma thesis, Universität Bremen, April 2010

Steffen Janßen
Entwicklung eines Herstellungsverfahrens von Mikrolinsen aus alkalifreiem Glas. Diploma thesis, Universität Bremen, 2010

Marco Kalkhorst
Entwicklung eines Batteriemanagementsystems für ein autonomes Unterwasserfahrzeug. Bachelor's thesis, FH Kiel, December 2010

Timm Florian Kraft
Zuverlässigkeitsanalyse von gelöteten und geklebten Flipchips auf Testsubstratleiterplatten. Abschlussarbeit zum staatlich geprüften Techniker, RBZ Kreis Steinburg, June,2010

Jan Lingner
Entwicklung eines Messaufbaus für Oberflächenwiderstandsmessungen. Diploma thesis, Technische Universität Hamburg-Harburg, May 2010

Michael Pleßen
Umsetzung eines Batteriemanagementsystems für ein Unterwasserfahrzeug. Bachelor's thesis, FH-Westküste, February 2010

Volker Röbisch
Auswahl und Charakterisierung von wasserlöslichen Bindern für die Herstellung von Anoden in Lithium-Ionen-Batterien. Bachelor's thesis, Christian-Albrechts-Universität Kiel, October 2010

Fabian Stoppel
Entwicklung, Herstellung und Erprobung miniaturisierter piezoelektrischer Energiewandler. Diploma thesis, Fachbereich Elektro- und Informationstechnik, Universität Bremen, June 2010

Venkat Hemanth Kumar
Examination of Highly-Selective Ceria-Based Slurries for Chemical-Mechanical Planarization. Master's thesis, Technische Fakultät der Christian-Albrechts-Universität zu Kiel, February 2010

Jiyuan Wang
Entwicklung eines integrierbaren schnellen A/D-Umsetzers als Teil einer flexiblen Systemplattform zur Auswertung von mikromechanischen Sensorsignalen. Master's thesis, FH Westküste, July 2010

Sebastian Weihausen
Programmierung einer hochauflösenden FFT auf einem FPGA-Board der Firma National Instruments mit LabView. Bachelor's thesis, FH Westküste, April 2010

JOURNAL PAPERS, PUBLICATIONS AND CONTRIBUTIONS TO CONFERENCES

R. Dudde, D. Kaden, H.-J. Quenzer, B. Wagner
Preparation of Functional PZT Films on 6" and 8" Silicon Wafers by High Rate Sputtering. Proceedings of Nanotech 2010, June 21 – 24, Anaheim, CA, USA, 2010

H. Greve, E. Woltermann, H.-J. Quenzer, B. Wagner, E. Quandt
Giant Magnetoelectric Coefficients in (Fe90Co10) 78Si12B10 - AlN Thin Film Composites. Applied Physics Letters 96, 182501, 2010

H. Greve, E. Woltermann, R. Jahns, S. Marauska, B. Wagner, R. Knöchel, M. Wuttig, E. Quandt
Low Damping Resonant Magnetoelectric Sensors. Applied Physics Letters 97, 152503, 2010

U. Hofmann, J. Janes, L. Ratzmann, S. Muehlmann, B. Wagner, W. Benecke
Scanning Laser Projection Display based on High-Q Vacuum Packaged MEMS Scanning Mirrors, SID-ME Chapter Spring Meeting, Dresden March 18 – 19, 2010

U. Hofmann
The flexible Control Panel. Information in the Passenger Cabin wherever requested. VDI-Forum „Innovations for Industry", Hannover Messe, April 19 – 23, 2010

U. Hofmann, J. Janes, L. Ratzmann, O. Schwarzelbach
Hermetically sealed 2D-MEMS Scanning Mirrors for High Resolution Imaging Applications.7th ESA Round-Table on MNT for Space Applications & 6th CANEUS Workshops, Noordwijk/ The Netherlands, September 13 – 17, 2010

H. Jacobsen, K. Prume, B. Wagner, K. Ortner, T. Jung
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D. Kähler
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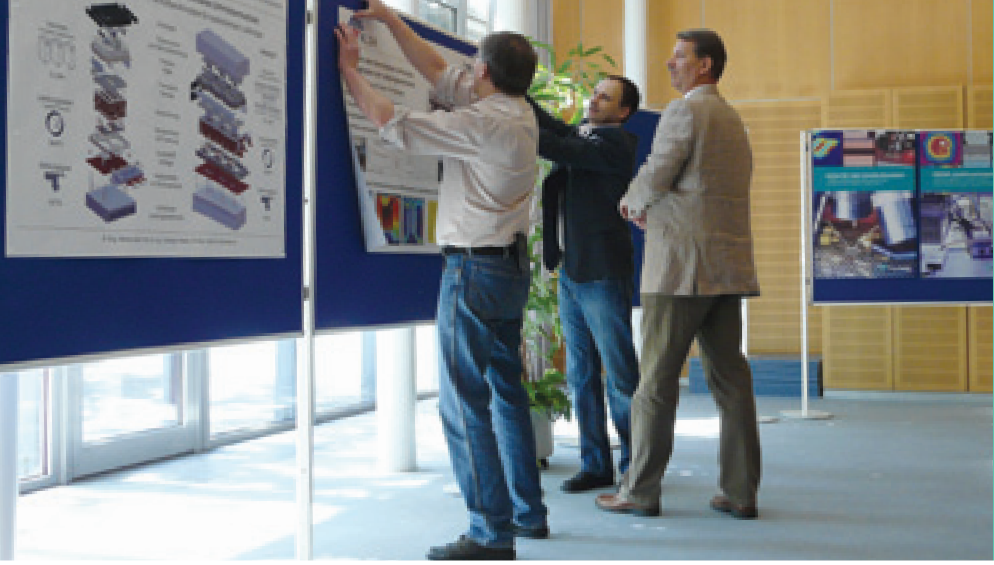

TALKS AND POSTER PRESENTATIONS

R. Dudde
MEMS Manufacturing Services, MEMS Foundry Itzehoe GmbH. International Nanotechnology Conference, INC6, Grenoble, France, May 17 – 20, 2010

R. Dudde
MEMS Foundry Itzehoe GmbH, Tech Connect Summit. Nanotech 2010, Anaheim, CA, USA, June 21 – 24, 2010

R. Dudde
Industrialization of Micro- and Nanomanufacturing, Foundry Model for MEMS Manufacturing. Chinano 2010, Suzhou, China, November 13 – 15, 2010

D. Friedrich
Das Kompetenzzentrum Leistungselektronik SH. 2. Workshop Kompetenzzentrum Leistungselektronik Schleswig-Holstein, Fraunhofer ISIT, Itzehoe, June 1, 2010

H. Hanssen
Prozessentwicklung von energie-effizienten Hochvolt-PowerMOS-Bauelementen nach dem Feldplatten-Kompensationsprinzip. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, June 02, 2010

U. Hofmann
Auf dem Weg zum Handy-Beamer – Neue Entwicklungen zu Mikrospiegeln für kompakte Laserprojektionssysteme. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, February 03, 2010

D. Kähler
Optimierung der Herstellungsprozesse für elektronische Module und Zuverlässigkeitsuntersuchungen basierend auf Testwafern. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, November 03, 2010

D. Kähler, W. Reinert
Test Chips For Advanced Packaging. Electronics Packaging Technology Conference (EPTC 2010) Singapore, December 8 – 10, 2010

T. Knieling
Mechanismen der Whisker-Entstehung und Folgen für die Funktionalität elektronischer Baugruppen. Arbeitskreis Zuverlässige, bleifreie Systeme, Fraunhofer IZM, Berlin, October 27, 2010

T. Knieling
Study of Mechanism of WhiskerGeneration. JISSO European Council Seminar, Nürnberg, June 09, 2010

K. Kohlmann
Kundenspezifische Leistungsbauelemente. 2. Workshop Kompetenzzentrum Leistungselektronik Schleswig-Holstein, Fraunhofer ISIT, Itzehoe, June 01, 2010

P. Lange
Massenfluss-Sensoren für Anwendungen in der Wasserwirtschaft, in der Medizin- und der Prozesstechnik. Seminar: „Forschung erforschen – die Innovationstour der Metropol-IHKs“, Fraunhofer ISIT, Itzehoe, April 20, 2010

P. Lange
Sensoren für die Bestimmung von Massenströmen in gasförmigen u. flüssigen Medien. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, September 01, 2010

E. Nebling
Portables Array-Biochip-System für die Infektionsdiagnostik vor Ort. Workshop „Infektiologische Fortbildung“, Universitätsklinikum Eppendorf (UKE), Hamburg, March 10, 2010

E. Nebling
Siliziumchips für die biochemische Sensorik, Workshop „Norddeutsche Initiative Nanomaterialien (NINa) - Nanomaterialien in der Sensorik“, Universität Kiel (CAU), Kiel, June 18, 2010

E. Nebling
Chip Technology in Diagnostics. 5th Hanseatic India Colloquium, Hamburg, Nov. 11 – 12, 2010

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G. Neumann
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Elektromobilität in der Fraunhofer-Gesellschaft: Erwartungen, Realität, Alternativen Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, March 03, 2010

G. Neumann
Landesfachkommission Elektromobilität: Präsentation des Fraunhofer ISIT. Fraunhofer ISIT, August 30, 2010

G. Neumann
Batterien der Zukunft – Fahren wir bald alle mit Elektroautos? Science Summer School Itzehoe, September 6 – 10, 2010

G. Neumann
Sicherheitsaspekte von Lithiumbatterien. Fachgruppentagung Elektronik und EDV, Hamburg, September 30 – October 02, 2010

G. Neumann
Lithium-Akkumulatoren für unterschiedliche Anforderungen. Einweihung Dispatch Energy Innovations GmbH, Itzehoe, Nov. 05, 2010

H.-C. Petzold
QM-System des Fraunhofer-ISIT mit Schwerpunkt auf Internen Audits. Workshop „Qualitätsmanagement“ der PTB, Berlin, March 26, 2010

G. Piechotta
MiChroChip - MEMS Chromatographiechip für portable Analysesysteme. VDI/VDE Forschungsrahmenprogramm Mikrosysteme - MST Vision, BMBF-Statusseminar, Berlin, Nov. 25, 2010

M. H. Poech
*1) Modellierung der thermischen Vorgänge im Reflow-Lötprozess.
2) Zuverlässigkeit bleifreier Lötverbindungen.
3) Hochstrom-Leiterplatten und geeignete Verbindungstechnologien. Seminar: Die beherrschbare Baugruppenfertigung, Fraunhofer ISIT, Itzehoe, February 10 – 12, 2010*

M. H. Poech
How Materials Behaviour affects Power Electronics Reliability. CIPS 2010, Nürnberg, March 16 – 19, 2010

M. H. Poech
Power Electronics Reliability – The Materials Behaviour is the Key. PCIM 2010, Nürnberg, May 04 – 06, 2010

M. H. Poech
*Zuverlässigkeit und Test von Leistungsmodulen.
2. Workshop Kompetenzzentrum Leistungselektronik Schleswig-Holstein, Fraunhofer ISIT, Itzehoe, June 01, 2010*

M. H. Poech
*1) Case Study: Soldering Process Compatibility.
2) Thermo-mechanics & Failure Modes.
ECPE Workshop Power Electronics Substrates - Materials, Performance, Processing and Reliability, München, June 17 – 18, 2010*

M. H. Poech
Löten im Bleifrei–Zeitalter. Fachhochschule Westküste, Mikroelektronische Systeme - Entwurf und Messtechnik, Heide, September 21, 2010

M. H. Poech
Entwärmung in Theorie und Praxis. Forum Pro-Active Design-In, Linz, Austria, October 21, 2010

M. H. Poech
1) Das Reflow-Lötprofil bei eingeschränktem Prozessfenster. 2) Hochstrom-Leiterplatten und geeignete Verbindungstechnologien. Seminar: Die beherrschbare Baugruppenfertigung, Fraunhofer ISIT, Itzehoe, October 27 – 29, 2010

M. H. Poech
*1) Werkstoffe der AVT I & II.
2) Passive Bauelemente, Schaltungsträger, Kühlkörper.
3) AVT für Systeme kleiner und mittlerer Leistung.
4) Fehlermechanismen.
Cluster – Schulung Aufbau- und Verbindungstechnik (AVT) in der Leistungselektronik, München, December 07 – 08, 2010*

K. Reimer
MILEPOST - MEMS IMU for Long-Term Position Stability and High Precision Rate Monitoring. Informationsveranstaltung Forschungsförderung für KMUs, IHK Kiel, October 13, 2010

W. Reinert
Packaging für fortschrittliche (inertial) Multi-Sensorikmodule. Fresenius Elektronik am Limit, Dortmund, October 01, 2010:

M. Reiter
Baugruppen und Fehlerbewertung, Inspektionskriterien, bleifreie Lötstellen. ISIT-Seminars: Die beherrschbare Baugruppenfertigung, Fraunhofer ISIT, February 11, and October 27, 2010

H. Schimanski
Lötqualität und Reflow-Lötverfahren. ISIT-Seminars: Die beherrschbare Baugruppenfertigung, Fraunhofer ISIT, Itzehoe, February 10 – 12 and October 27 – 29, 2010

H. Schimanski
Qualitätsprüfung an Leiterplatten. ISIT-Seminars: Die beherrschbare Baugruppenfertigung, Fraunhofer ISIt, Itzehoe, February 10 – 12 and October 27 – 29, 2010

H. Schimanski
Baugruppen schonende Reworkprozesse. 2. Elektronik-Technologie-Forum Nord, Hamburg, Feb. 24 – 25, 2010

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H. Schimanski
Kostenoptimiertes Leiterplattendesign aus Sicht der Elektronikfertigung. Workshop "Kostenoptimiertes Leiterplattendesign", Letron Electronic, Osterode, May 06, 2010

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H. Schimanski
*Bleifreies Löten von elektronischen Baugruppen.
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Lötqualität - Lötmetallurgie und Lötoberflächen, Lötbarkeit und Flussmittel. ISIT-Seminar: Praxisorientierte Prozessoptimierung in der elektronischen Baugruppenfertigung -Fehlervermeidung durch sicher beherrschte Fertigungsschritte, Fraunhofer ISIT, Itzehoe, November 15 – 19, 2010

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TALKS AND POSTER PRESENTATIONS

H. Schimanski
1) Metallurgie des Weichlötens. 2) Baugruppen schonende Reparatur komplexer SMT-Baugruppen. 3) Baugruppen- und Fehlerbewertung. ISIT-Seminar: Der optimierte Rework-Prozess, Fraunhofer ISIT, Itzehoe, November 24 – 26, 2010

O. Schwarzelbach
Technologietag Baugruppentest in Jena; "Schneller Mehrkanal-Endtest von mikromechanischen Inertialsensoren auf Waferebene unter Verwendung von FPGA-Modulen der R-Serie" March 10, 2010

R. Siegmund
Röntgen und Ultraschallprüfung. ISIT-Seminar: Zerstörungsfreie Prüftechnik, Fraunhofer ISIT, Itzehoe, March 03, 2010

T. C. Thönnessen
Pastenaufbereitung und Elektrodenherstellung im ISIT-Technikum. Einweihung Dispatch Energy Innovations GmbH, Itzehoe, Nov.05, 2010

T. C. Thönnessen
Beschichtungstechnikum für Lithium-Polymer-Akkumulatoren am ISIT. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, December 01, 2010

B. Wagner
Technology Platforms for Micro-Nanoelectromechanical Systems. Seminar University of Southern Denmark Sonderborg, October 15, 2010

S. Warnat
Nanostrukturierte Materialien für neuartige Mikrosysteme. Aspekte moderner Siliziumtechnologie, Fraunhofer ISIT, Itzehoe, April 07, 2010

C. Wijayawardhana
High power and low temperature behavior of NMC cathode materials. 218th Electrochemical Society Meeting, Las Vegas, USA, October, 2010

A. Würsig
Activities of Fraunhofer ISIT in Lithium Ion Batteries. NEDO Japan, March 2 – 3, 2010

A. Würsig
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PATENTS

H.-J. Quenzer, A. Schulz-Walsemann, B. Wagner, P. Merz
Method for structuring a flat substrate consisting of a glass-type material JP 4480939

T. Lisec, B. Wagner
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Method for producing single microlenses or an array of microlenses, US 7,726,154 B2

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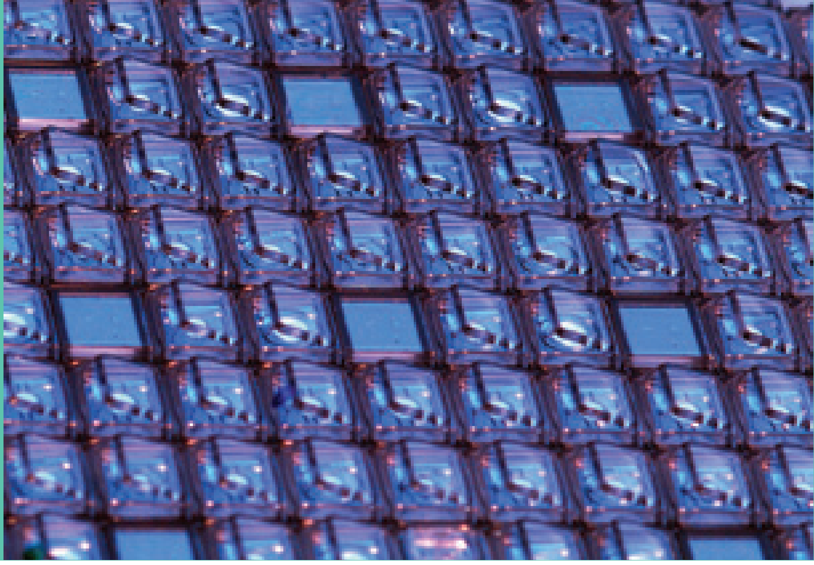
OVERVIEW OF PROJECTS

- *Ultrakompakte Leistungsmodule höchster Zuverlässigkeit ULTIMO*
- *Simulationsstudie für Fast Recovery Dioden*
- *Energie-Effiziente Elektrische Antriebstechnik: Neue Umrichterkonzepte*
- *Lochmembranen im sub-0,5µm Bereich*
- *Entwicklung neuer Ansätze für RC-IGBTs*
- *Optimierung von AMR Winkelsensoren*
- *Super Junction PowerMOS*
- *Ultrathin Trench IGBTs on sub-100 µm Si-Substrates*
- *Untersuchung von Ceroxid-Dispersionen für CMP*
- *Entwicklung von poly-Si CMP Prozessen für die MEMS Herstellung*
- *Untersuchung an mikromechanischen Drehraten-Sensoren*
- *Entwicklung von kapazitiven HF-Schaltern*
- *Entwicklung von piezoelektrischen Schichten für Si-Mikroaktuatoren*
- *Herstellung mikrooptischer Linsenarrays aus Glas*



- *Mikrolinsen aus Borosilikat glas*
- *RF-MEMS Packaging*
- *Zero- and First – Level Packaging of RF MEMS*
- *Piezoelektrischer Messkopf für die Ultraschallanalytik*
- *High volume piezoelectric thin film production process for Microsystems, piezo Volume*
- *Entwicklung von PZT-Schichten*
- *Mikroscann-Systeme für Display Anwendungen*
- *Herstellung mikrotechnischer analoger Ablenkeinheiten*
- *Magnetoelektronische Sensoren (Sonderforschungsbereich 855 der Uni Kiel)*
- *Entwicklung von LIDAR Systemen MiniFaros*
- *Development and Fabrication of 256k CMOS Blanking Chips for Maskless Lithography*
- *Maskless lithography for IC manufacturing, MAGIC*
- *Maskless Nanolithography, RIMANA*
- *Development of an ASIC for the control of BLDC-motors*
- *Dünnfilm Transducer PIETRA*
- *MEMS-Chromatographiechip für portable Analysesysteme MiChroChip*
- *Zellfreie Bioproduktion*
- *Vollautomatische Detektion biologischer Gefahrstoffe mit integrierter Probenaufbereitung, BioPROB*
- *Analysesystem für die markergestützte intraoperative Tumordiagnostik*
- *USDEP, Ultrasensitive Detection of Emerging Pathogens*
- *ivD-WISA, in vitro Diagnostik Plattform*
- *MIT-Modularer In-Mould Transponder*
- *Pyroelectric IR Motion Sensor*
- *ZIM-Projekt im Rahmen des Konjunkturprogramms II der Bundesregierung*
- *Stressoptimierte Montage und Gehäusetechnik für mikromechanisch hergestellte Silizium-Drehratensensoren*
- *Glassfritt Vacuum Wafer Bonding*
- *Glaslotbonden mit strukturierten Capwafern und Musterwafern*
- *Wafer Level Packaging*
- *Process Development for Hermetic AuSn Vacuum Sealing of µ Bolometer Sensors on Wafer Level*
- *Wafer Level Balling for 100 µm up to 500 µm Spheares*
- *Neon Ultra Fine Leak Test for Resonant Micro Sensors*
- *Solder Flip Chip on Flex*
- *Flip chip Embedding Study and Demonstration*
- *Qualitätsbewertung an bleifreien Baugruppen*
- *Lötwärmebeständigkeit und Zuverlässigkeit neuer Konstruktionen im manuellen Reparaturprozess bleifreier elektronischer Baugruppen (AiF-Projekt)*
- *Tin-Whisker Evaluation of Components and Assemblies with Tin Finishes*
- *Prozessoptimierung beim Selektivlöten für Anwendungen in der Leistungselektronik*
- *Assistance for Electronics Manufacturers in the Transformation to RoHS Compliant Products and Processes*
- *Untersuchung zu den thermischen und prozesstechnischen Eigenschaften von Flussmitteln für bleifreie Lötlegierungen auf hochzuverlässigen Baugruppen*
- *ZuSi- Zuverlässiger Ag-sinterkontaktierte Halbleiterbauelemente für die regenerative Energietechnik*
- *Ionische Liquide für elektrochemische Applikationen (IL-Echem)*
- *Amagnetische Lithiumzellen*
- *Flottenversuch Elektromobilität*
- *Hochenergie-Lithiumbatterien für die Zukunft-HE-LION*
- *Hochleistungslithiumbatterien mit Nanopartikeln in Core-Shell-Technologie LINACOR*
- *Entwicklung einer Zelltechnologie für Solarstrom-Zwischenspeicherung*
- *TIETEK Tiefsee-Inspektion und Explorations-Technologiekonzept*

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CONTACT

Please contact us for further information.
We would be glad to answer your questions.

FRAUNHOFER-INSTITUT FÜR SILIZIUMTECHNOLOGIE, ITZEHOE

Fraunhoferstraße 1
D-25524 Itzehoe
Telephone +49 (0) 48 21 / 17-42 11 (Secretary)
Fax +49 (0) 48 21 / 17-42 50
info@isit.fraunhofer.de
www.isit.fraunhofer.de

PRESS AND PUBLIC RELATIONS

Claus Wacker
Telephone +49 (0) 48 21 / 17-42 14
claus.wacker@isit.fraunhofer.de