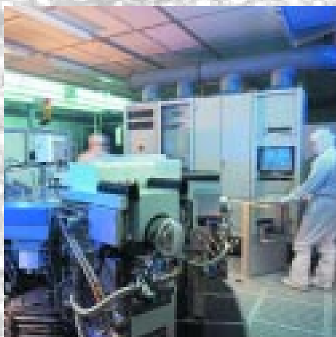
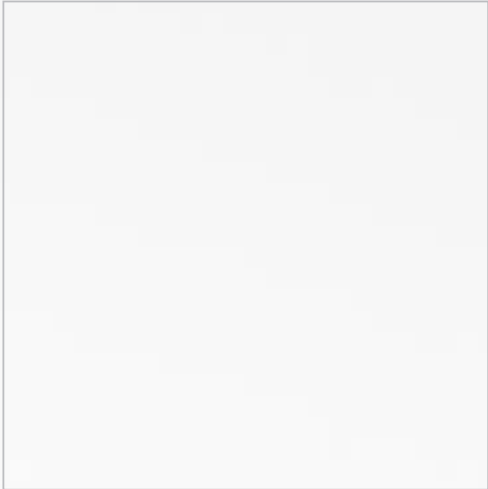
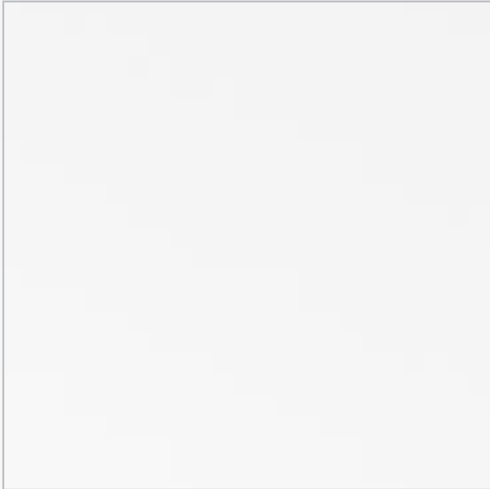
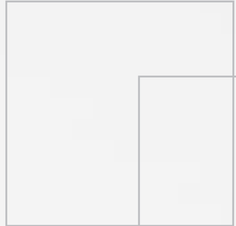
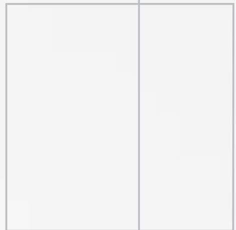
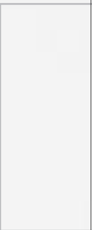
Fraunhofer Institut Siliziumtechnologie

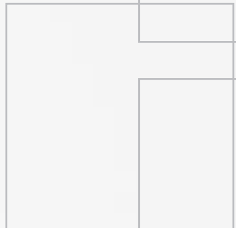
Achievements and Results
Annual Report 2002



Modern work places at Fraunhofer ISIT: employee in the cleanroom environment.



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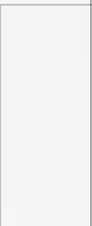
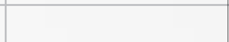

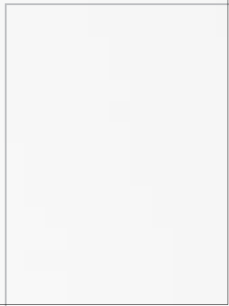

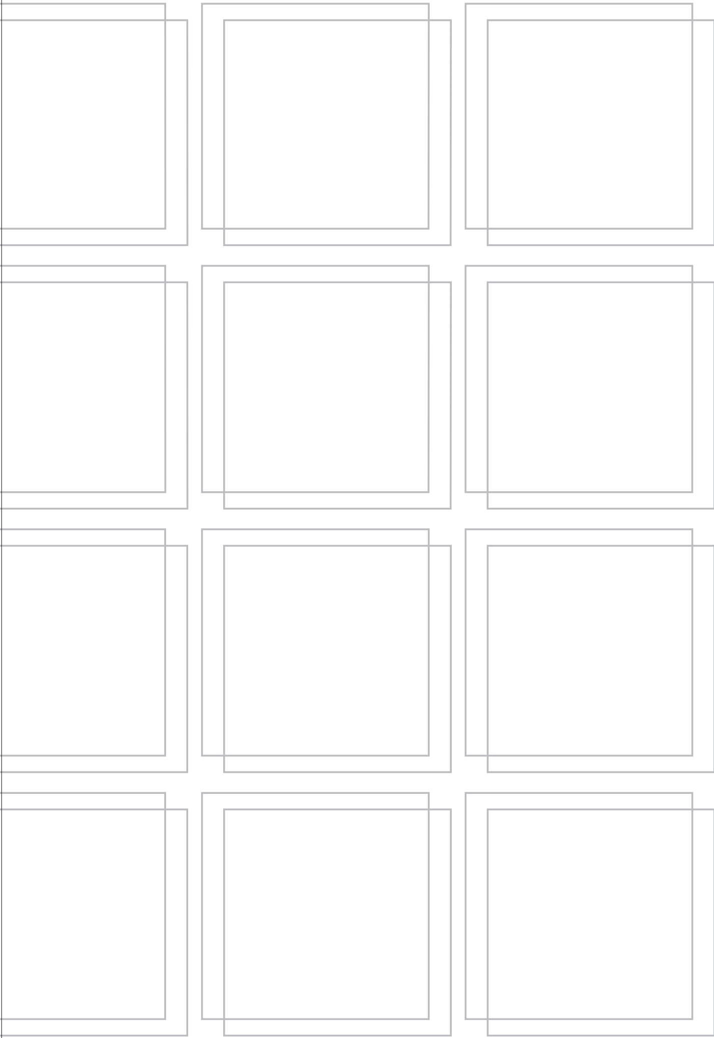

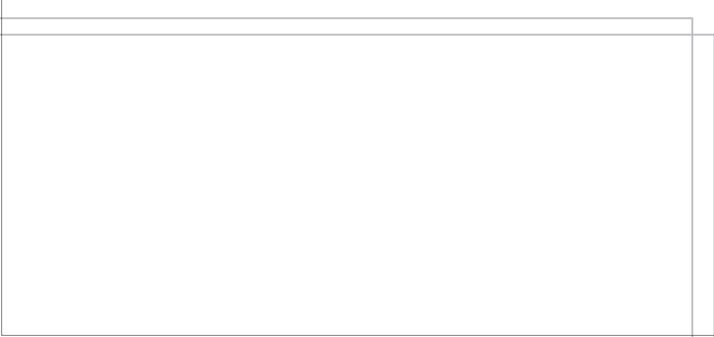

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Annual Report 2002

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Fraunhofer ISIT, a chrystalisation point for different companies in Itzehoe: (from front to rear: Prokon, IZET, Fraunhofer ISIT, SMI, Solid Energy and Condias.

New production hall for Solid Energy and Condias.

New spin-off companies in Itzehoe play a major role in this context, in cases where it has been contractually agreed that a large part of their product development work will take place in cooperation with ISIT.

In 2002 important landmarks were achieved for ISIT and the high-technology location of Itzehoe. During the summer a new production hall for the companies Solid Energy and Condias in the direct vicinity of the Fraunhofer ISIT was completed and officially opened by economics minister Dr. Bernd Rohwer and member of parliament Dietrich Austermann.

The new building complex includes a production hall of 1,875 square meters and a connected two-story administration wing providing 600 square meters of office space.
The cost of the building totalled 1.8 million euros. A further 5.4 million euros was invested in additional hall infrastructure and production facilities, of which 3.7 million euros were raised by Solid Energy and 1.8 million euros by Condias. In the medium term these companies will together create 75 jobs.

Both firms are without doubt among the biggest and technically most advanced new spin-off companies of the Fraunhofer-Gesellschaft in recent years. Condias, which was established by the Fraunhofer Institute for Surface Engineering and Thin Films, Braunschweig, has installed a production unit for the manufacture of conductive diamond coatings in the new hall, from where it supplies its customers. These diamond coatings find use in a wide range of applications, such as in the environmental sector, where they are employed in the ecologically beneficial processing of substances that are otherwise difficult to dispose of safely. Solid Energy, a business spin-off from the ISIT, intends to build a production line in the hall to make lithium batteries for the telecommunications market.

Solid Energy is highly regarded in the state of Schleswig-Holstein as an example of successful technology transfer. In November the company was presented with the Schmidt-Römhild Technology Award 2002 by economics minister Dr. Bernd Rohwer. This award was inaugurated by Lübeck-based publishing house Schmidt-Römhild to honor pioneering developments by small firms in Schleswig-Holstein.

But the opening of the new production hall was not the only event to generate optimism, and it was also good to see the resumption of building work at the neighboring firm SMI GmbH.

Be glad about two new companies in Itzehoe: Dr. Ingo Hussla head of IZET, Condias founder Dr. Matthias Fryda and Dr. Thorsten Matthée, mayor of Itzehoe Harald Brommer, ISIT-curator and member of parliament Dietrich Austermann, minister of economic affairs in Schleswig-Holstein Dr. Bernd Rohwer, Prof. Anton Heuberger head of ISIT and Solid Energy founder Dr. Gerold Neumann.

The construction of a new silicon chip factory had been halted in spring 2001 owing to the general recession in the semiconductor industry. Now the management of Philips has decided to resume the planned activities. As a first step the development and administration building is being completed. The work is now almost finished.

Naturally, an applied research institute such as ISIT can only occupy a firm long-term position in the market if it is able to produce a steady stream of innovative ideas and tech-

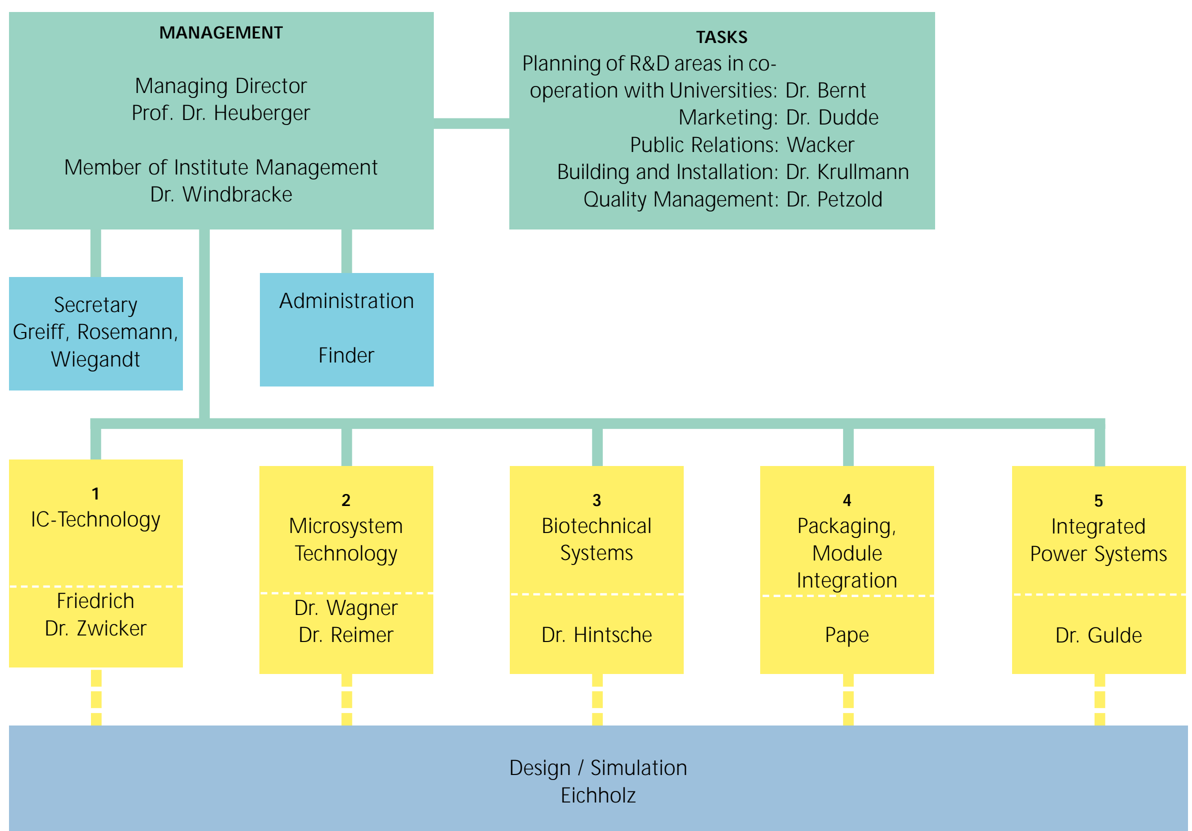
Impressions of the opening of the new factory building for Solid Energy and Condias right next to the Fraunhofer ISIT on June 24, 2002.
Founded Condias: Dr. Matthias Fryda, Dr. Thorsten Matthée;
ISIT-curator Dietrich Austermann;
take care for music: Iris Kramer and Hròlfur Vagnsson.

nologies. Without this capability the appealing technological concept of ISIT, based on its close links to production, would be ineffective. Adequate application-oriented basic research is therefore required which covers a time-frame of between five and ten years.
The result of this advance research must, however, be to create products as quickly as possible and to transfer them to industrial use. In the absence of such a strategy, advance research can become indistinct from basic research of no entrepreneurial value.
The major subject areas of long-term advance research currently pursued by ISIT are as follows:

- Power electronics:
  New integration techniques for power components used in mains-operated applications with a blocking ability of up to 1200 V. The aim here is to develop monolithic integration techniques in silicon in order to supply the foreseeable high-volume new markets with miniaturized components at acceptable cost.
- Microsystem technology:
  Development of improved surface micromechanics which can be integrated with CMOS, mainly with the objective of realizing the next generations of mirror arrays (for example, large array fields with 1,000 positions for fiber-optic technology, or more-robust mirror systems for use in portable systems, such as GPS in mobile phones).
- Biosensor systems: Development of a wafer-scale biocoating technology on the basis of inkjet printing for the manufacture of application-specific biosensors.

The application goals pursued by ISIT,

ISIT Organigram



together with its spin-off firm eBiochip Systems GmbH, focus on special subjects in medical engineering, food monitoring and the development of measuring systems for the continuous detection biological warfare agents.

- Assembly and interconnection technology: Further development of wafer-scale packaging techniques incorporating 'balling' technologies, serving as the basis to set up a service company in this field in Itzehoe. The main aim here is to make a contribution towards the successful return of advanced AVT techniques from the Far East to Europe.
- Lithium batteries: Development of lithium-polymer cells which are specially optimized for traction applications (42 V on-board supply system and hybrid drives). The basis for this is the development and deployment of new coating systems incorporating lithium-manganese-oxide spinels.

Prof. Anton Heuberger, Dietrich Austermann (from left).

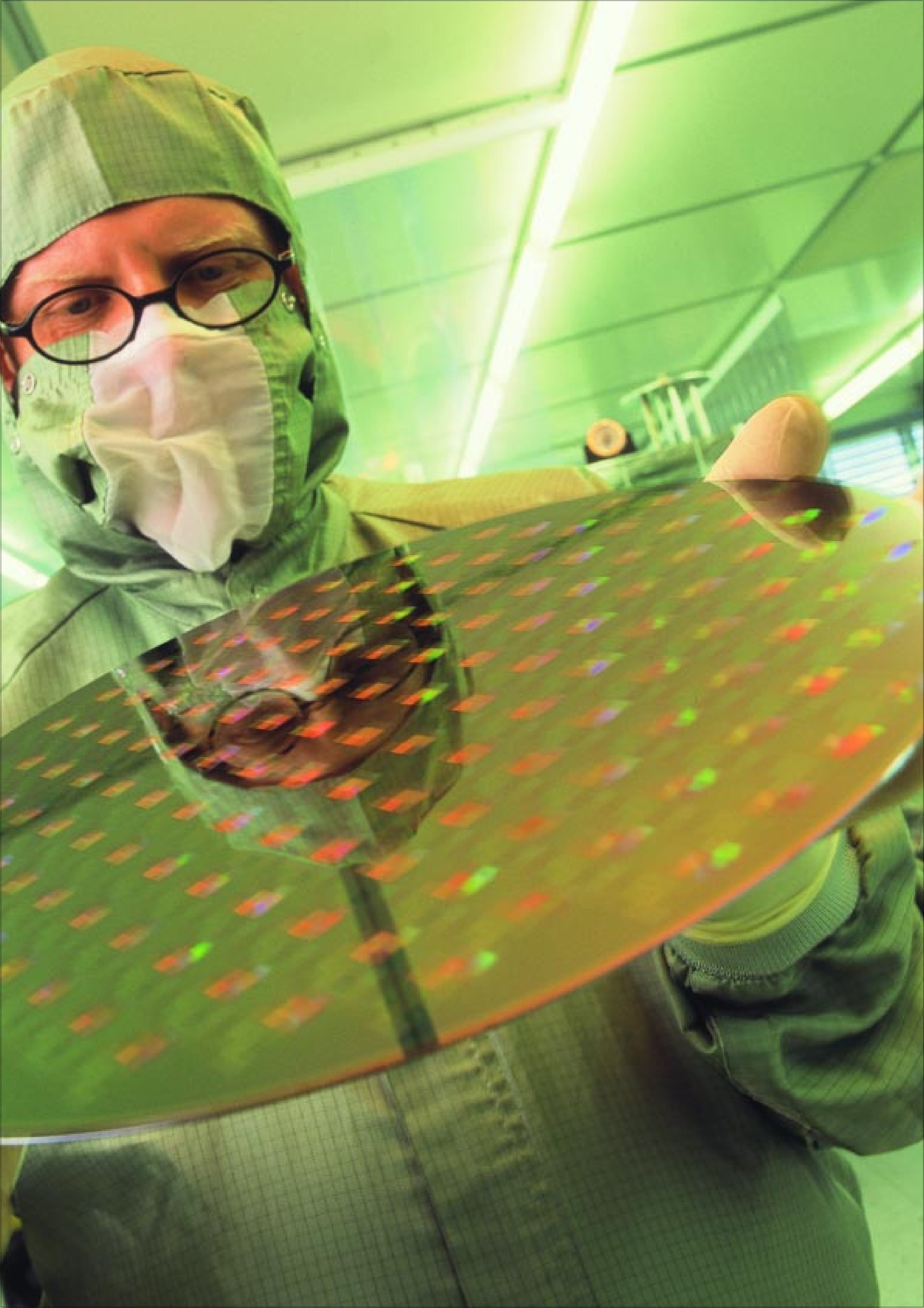
This summarizes an ambitious R&D program which, if successful, will without doubt attract considerable demand form industry.

Apart from the perpetual issues of financing, the quality of staff and their ability to contribute innovative ideas is of decisive importance. That ISIT and its staff possess this ability is impressively confirmed by the work conducted up until today by the Institute. I would like to take the opportunity at this point to thank all staff for their commitment and sunstantial efforts.

Dr. Gerold Neumann, mangaging director of Solid Energy.

Solid Energy GmbH was honoured with the Schmidt-Römhild Technology Award 2002.

Anton Heuberger



Brief Portrait

The Fraunhofer-Institut für Siliziumtechnologie (ISIT), Itzehoe, works on design, development and production of microelectronic components as well as on microsensors, microactuators and other components for microsystems technology. All devices of this kind can be delivered either being prototypes or customer specific series.

Among the Fraunhofer institutes working on microelectronics ISIT is concentrating upon the development of new process technologies for semiconductor silicon based components and microsystems.

In cooperation with the adjacent Innovationszentrum (IZET) ISIT also aims at creating new jobs within the high-tech field.

The institute is running a professional semiconductor production line together with the company Vishay Semiconductor Itzehoe GmbH. This line is used for the production of microelectronic devices (PowerMOS) and microsystems by Vishay as well as for R&D projects for new components and technological processes by ISIT.

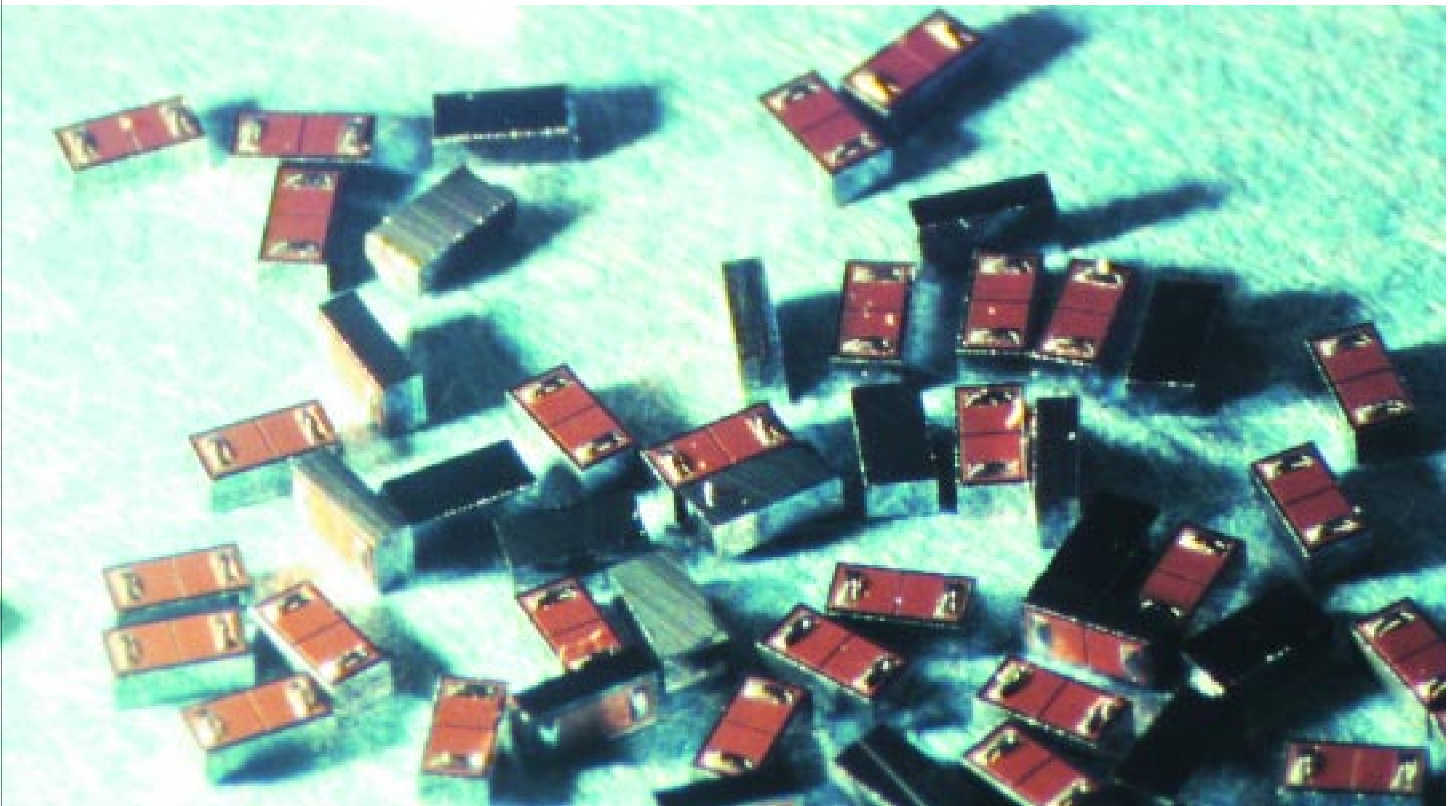
In view of its current and future production and development activities, especially for automotive industries, ISIT is establishing a quality management system which is going to be ISO 9001 certified in spring 2003.

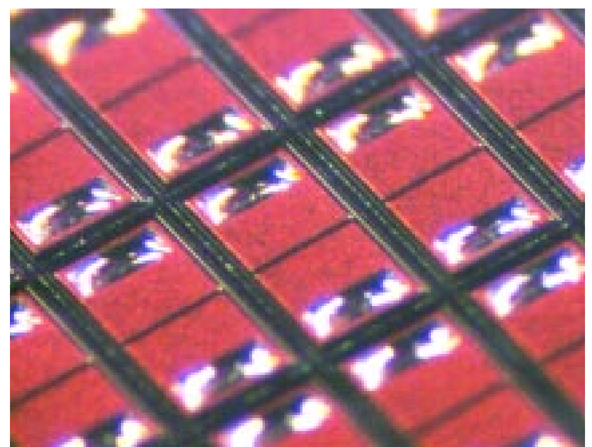
Further services offered by the institute are the analysis and development of technology pertaining to the quality and reliability of electronic assemblies as well as packaging and mounting technology for microsystems, sensors and multichip modules. A focal point of work in this field involves new packaging techniques for large-area microsystems.

A new activity is the development of advanced power-supply components for electronic systems.

The complete institute staff consists of about 150 employees.

Chemical-mechanical polishing (CMP), a process step for microelectronic and microsystem applications.





RF chip capacitors with solder bump termination, in size 500 µm by 1000 µm.

Main fields of Activity

IC-Technology

The IC-Technology department is focused on the development and fabrication of active and passive silicon based devices.

In the field of active devices IGBTs, PowerMOS and diodes are of special importance. Here, ISIT can rely on a qualified core technology for power devices provided by our industrial partner. Customer specific development of power devices is supported by simulation, design and electrical characterisation.

Further, ISIT has many years of experience in developing advanced CMOS processes with appropriate simulation and circuit design capability.

Passive components like chip-capacitors, -resistors and -coils are another field of ISIT activities. Evaluation of new materials and its integration in complete processes is one important topic for passive IC develpoment.

In addition ISIT offers customer specific wafer processing in small and medium quantities based on standard IC and MST technology.
This includes the development of new single processes and process modules for all relevant fields of semiconductor technology.

Chemical-Mechanical Polishing

Planarisation by means of chemical-mechanical polishing (CMP) is a key process for the fabrication of advanced ICs. The institute's CMP application lab is equipped with CMP cluster tools, single- and double-sided polishers and post-CMP cleaners for substrate diameters of up to 300 mm and offers services on all aspects of CMP development like

- Testing of CMP equipment
- Development of CMP processes for
  - dielectrics (oxide, low-k materials, ...)
  - metals (tungsten, copper, ...)
  - silicon
- Testing of polishing slurries and pads
- Post-CMP cleaning
- CMP-related measurement
- Custom-specific CMP services for device manufacturing

In the field of CMP ISIT co-operates closely with equipment and pad/slurry manufacturers, production CMP users and the wafer industry.

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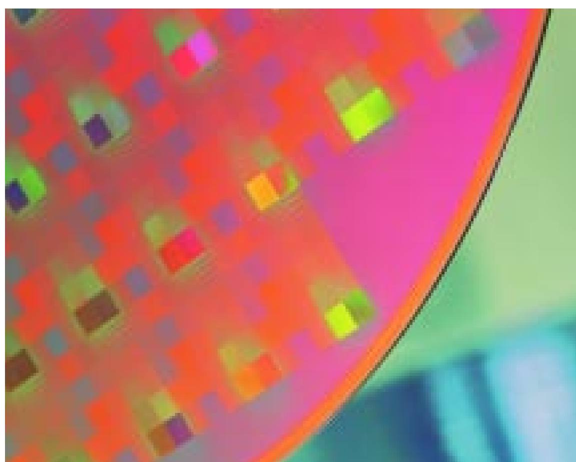
Test structures for the development of new CMP processes.



Wet chemistry section.

IC-Design

Besides the main tasks of designing and testing mixed-signal ASICs, mainly in co-operation with in-house departments for microsystem development, the IC-Design department offers the design of micromechanical and microoptical elements using analogue HDL for modelling and IC-layout and IC-verification tools.

State of the art IC-Design, FEM and mathematics software is used. For test purposes laboratories equipped with hardware for electrical measurements in time and frequency domain and for mechanical and optical standard tests are available.

Over the years a number of helpful designtools have been developed to accelerate the designflow from the idea to masklayout. Those tools are part of special MEMS-design-kits to support the designer using micromechanical processes, including features like DRC, HDLA-models, cross-section viewer, layout generators and easy-to-handle user interfaces to mechanical simulators.

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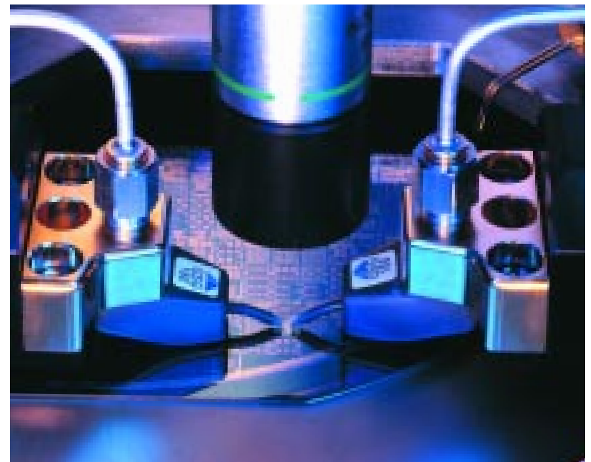

MEMS wafer on
RF probe station.

Microsystems – MEMS

The MEMS department focuses on the application specific development of physical, optical, fluidic, and RF-MEMS components and the integration to microsystems. We have access to the 6-inch silicon frontend technology of the in-house industrial semiconductor production.
In addition, qualified MEMS processes are offered in a foundry service, e.g. wet etching and deep RIE of silicon, thick resist lithography, grey-scale lithography, electroplating, epitaxial polysilicon, SOI-micromachining, glass micromachining, replication technologies, wafer bonding and chemical-mechanical polishing. In the EUROPRACTICE frame we provide design-house service also for external MEMS foundry processes.
The MEMS department works in close collaboration with the ASIC-Design and the packaging departments in order to offer integrated microsystem solutions.

The physical sensor work focuses mainly on automotive applications, especially sensors for angular rate, acceleration, pressure and air flow. The optical MEMS activities are driven by applications for optical communication and measuring systems. Examples are fiber-optic switching systems, laser scanners, digital micromirror arrays, spectrometers, and also passive optical components, e.g. refractive and diffractive microlenses. RF-MEMS components, such as RF-switches, tunable capacitors and micro-relays are developed for wireless communication applications. Examples of fluidic microsystems are pneumatic microvalves, sensor-controlled micro-pipettes and micropumps.

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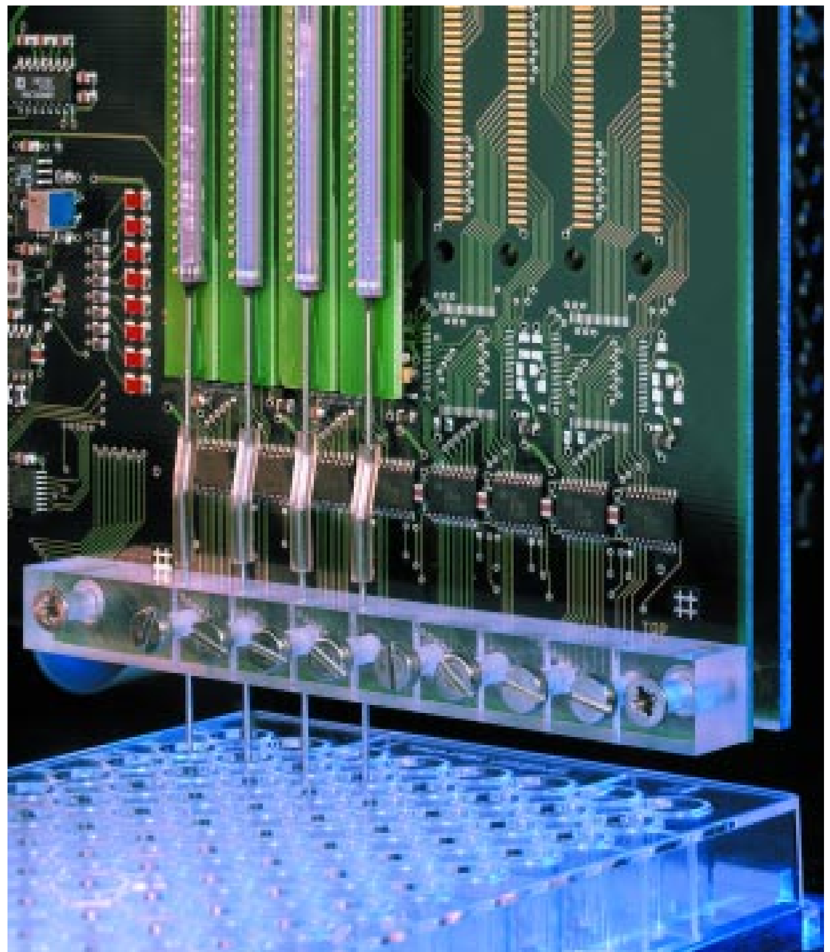

Automated
sensor controlled
micro pipetting system for
micro titer plates.

Biotechnical Microsystems

The department Biotechnical Microsystems is focusing its activities in the field of electrical biosensor technologies. Our activities aim at the design and construction of novel sensing arrays in miniaturized formats. The development of ultramicroelectrodes arrays enable novel biosensor constructions and the evaluation of highly sensitive and new approaches of selective detecting principles, e.g. the redox recycling of ELISA based assay products and impedance spectroscopy.

The integration of the transducers made in silicon technology and microfluidic systems with electrical manipulation of biomolecules opens new applications in biochemical assays, medical diagnostics and environmental analytics.

Sub-µm-electrode arrays have been developed as the widely applicable eBiochip technology platform for different analytic approaches. In combination with microfluidic components on chip and miniaturized or integrated electronics these components form the basis of smart portable analytical systems. There are low density highly sensitive array chips with external electrical read out and fully integrated electronic biochips with medium density, which have been developed together with industrial partners.

The department Biotechnical Microsystems offers R&D and services in the multi-channel sensor array technology as an attractive feature for fully electrical nucleic acid and protein chips. Also a novel micromachined glucose sensor enables long term online monitoring of human body fluids. For highly sensitive continuos monitoring the electrical chips have been combined with the magnetic beads technology.

The eBiochips may be used as parts of "lab-on-chips" and micro-total analysis systems.
For market activities a spin off company (www.ebiochipsystems.com) have been positioned to improve the way of biochemical and molecular biological analysis and to manufacture the eBiochiop TM measuring devices and analytic systems.

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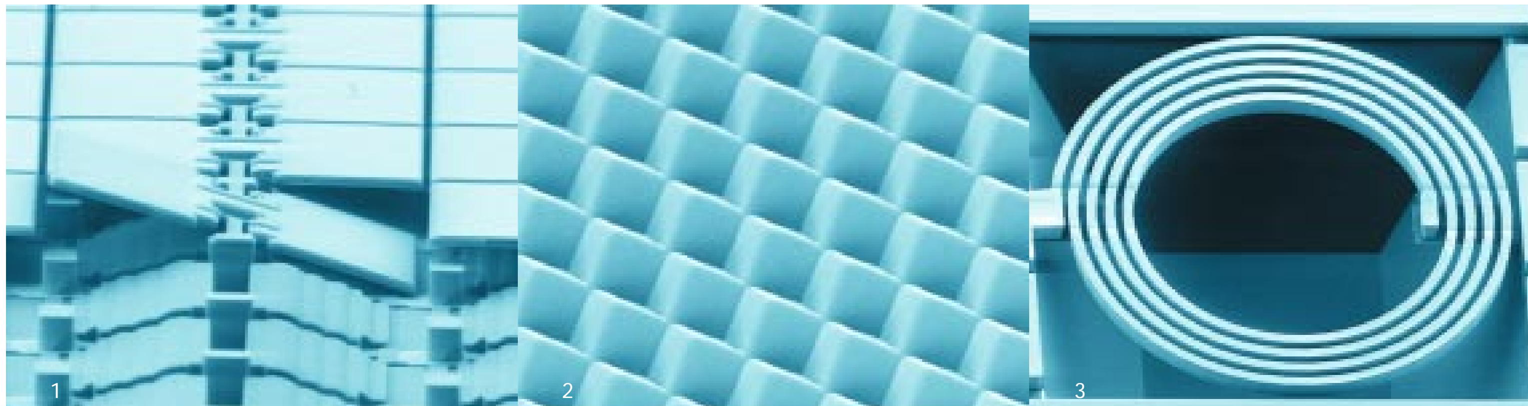

Foundry Service

Devices for UV-laser ablation and polishing the cornea surfaces of human eyes.

The technological services of ISIT extend from the development of single proccess steps and single devices to the set-up of complete microsystems. In close cooperation with the industrial partners Vishay and SMI, Fraunhofer ISIT is also offering serial production of microsystem devices with advanced silicon production technologies. For this foundry services ISIT assures ists customers strict confidentiality concerning production processes and products. The same methods of quality control and qualification are applied that were introduced into the ISIT for the qualified and certified running Vishay production. For microsystem foundry production all technologies are available on 6" wafers that were developed and introduced by ISIT. These are especially:

- Bulk Micromachining,
- Surface Micromachining,
- Metal Surface Micromachining,
- High Aspect Ration Microforming,
- CMOS and DMOS Technologies.

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Digital micro mirror (1), different retroreflectors in polycarbonat coated with aluminium (2, 4 and 6), nickel coil on top of a KOH etched cavity (3), nickel-master for replication of retroreflectors (5).

Power module with 90 µm thin diodes and IGBTs manufactured in cooperation with Danfoss Silicon Power GmbH, Schleswig.

Transponder modules with ultra-thin solder flip chip attach.

Assembly and Packaging Technology for Microsystems, Sensors and Multichip Modules

In advanced packaging technology ISIT focuses on wafer level packaging (WLP) and direct chip attach techniques for multichip modules (MCMs) and for MEMS components. For WLP a 150 mm wafer pilot line for small to medium volume runs has been established with following features: under bump metallization, BCB passivation, solder balling, grinding, backsite metallization, parameter test and dicing. The bonding of bare dice and microsensors is realised by applying chip-on-board (COB) and especially flip-chip technology, where bare ICs are mounted and simultaneously interconnected face down onto the substrate. The processes available at ISIT include wafer preparation with chemical deposition of NiAu, different bumping techniques (printed solder bumps, Au stud bumps), wafer grinding, wafer dicing, flip-chip placement and inter-connection by adhesive joining or soldering. Furthermore, ISIT deals with mounting and packaging technology of power electronic components and modules.

Standard processes for hermetic package sealing are available, e.g. metallic packages are sealed by laser welding in inert gas atmosphere.

Furthermore, ISIT works on wafer level encapsulation of MEMS devices using glass frit and metallic seal bonding. Automatic equipment facilitates to enable the production of demonstration series under industrial conditions.

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Quality and Reliability of Microelectronic Assemblies

The main competence is attributed to the evaluation of the manufacturing quality and the reliability of microelectronic assemblies and modules including the as-delivered quality of components and circuit boards. Methods are destructive metallographic as well as non destructive (e.g. x-ray) principles. The evaluation of the long-time behaviour of the assemblies is based on the matrix of requirements using model calculations, environmental and load tests up to failure analyses. For optimisation of manufacturing processes the institute applies process models and fabricates samples on in-line equipment including mass production as well as rework systems. Furthermore, in the field of thermal management and reliability ISIT works on customer specific power modules.

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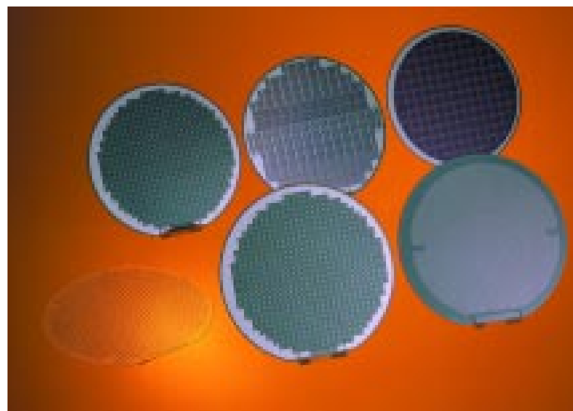

Customer specific test wafer for packaging process assessment.

Integrated Power Systems

The increasing demand for portable systems calls for new types of rechargeable batteries. Besides high energy density and long service life, safety and environmental compatibility also play an important role. For these requirements ISIT offers a new concept of battery based on lithium ions, which has been developed by ISIT. The new batteries contain a solid-state electrolyte. The high energy density typical for lithium systems is in no way compromised. As the materials used are sufficiently inert, there is no need for the usual elaborate leakproof metal casing. The raw materials are available in paste form, and the batteries are produced using inexpensive thick-film technologies. They can be laid down on rigid or flexible substrates, but it is also possible to extrude the pastes as films which can be laminated to form flexible foil batteries requiring no substrate. A large number of shapes can be created by cutting and rolling; the battery is then sealed and encapsulated in metallized plastic.

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Lithium polymer rechargeable batteries: low weight, scalable, powerful, flexible in design.

Equipment

For the ISIT activities at Itzehoe, a complete 150/200 mm silicon technology line in a clean room area of 2000 m^2 (Class 1) including a combined mini-environment- and SMIF-concept for 0.5 µm CMOS technology and microsystems technology is used. The equipment was chosen in accordance to the latest state-of-the-art in semiconductor industry. For specific processes of microsystems and multichip module technology an additional clean room area of 450 m^2 (class 100) with appropriate equipment is used.
A seperate 200 m^2 clean room laboratory was set up for chemical mechanical polishing (CMP) and post CMP cleaning processes.

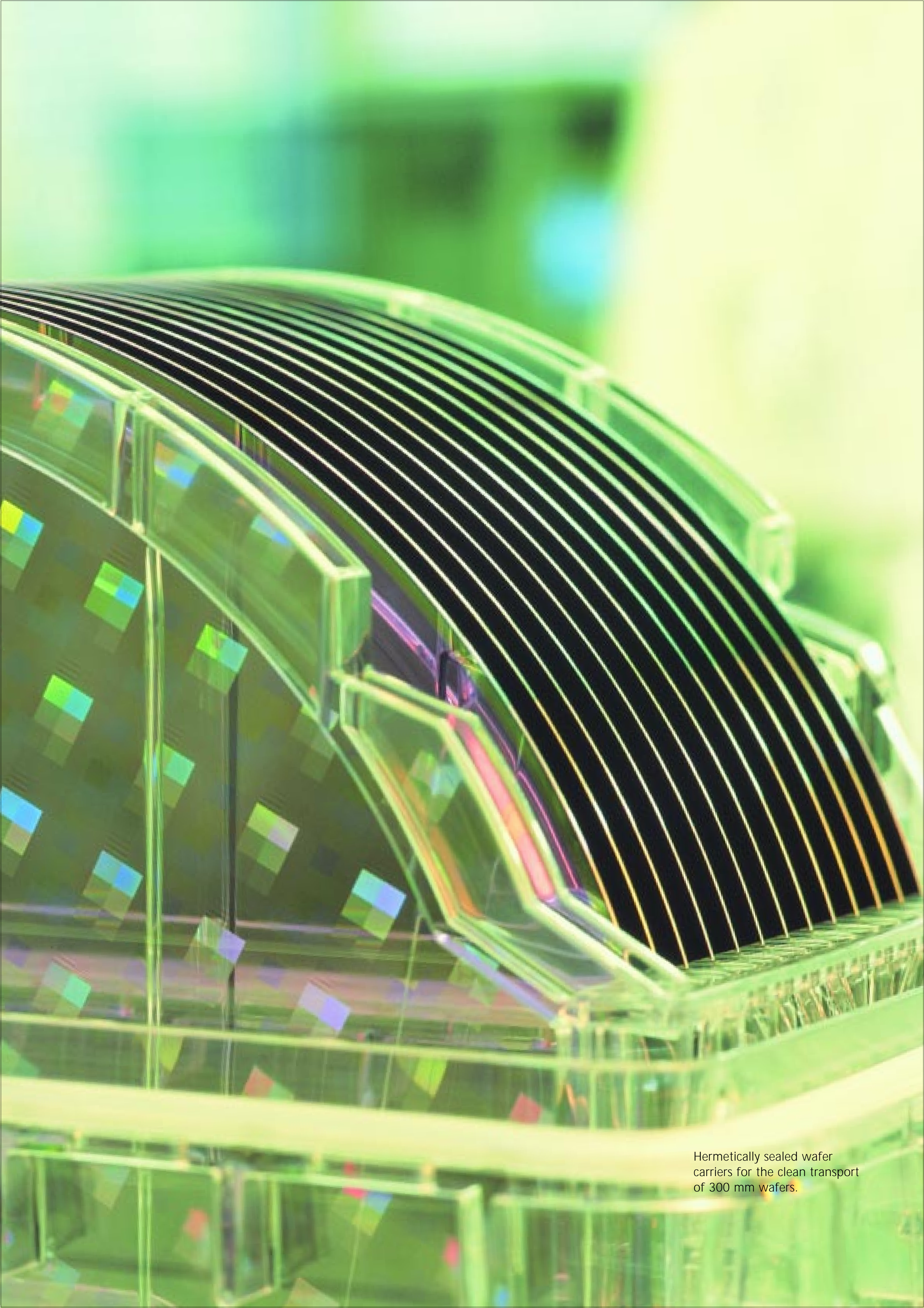
Additionally, a laboratory area of 1500 m^2 is utilised for the development of chemical, biological and thermal processes, for electrical, mechanical and thermomechanical characterisation of components and systems, for assembly and packaging and for multichip module technology.

For the production of lithium solid polymer cells in the capacity range of 100 – 2000 mAh a pilot line has been established. A complete test environment for batteries is available.

Both for the simulation and the design of components and systems different commercial software tools are installed on our in-house computer network.

ISIT cleanroom:
lithography area.

Wide field stepper for
MEMS lithography.


Hermetically sealed wafer carriers for the clean transport of 300 mm wafers.

Service Offers

Microelectronic components and microsystems are used in a multitude of products.

The institute offers its service to different branches of industry and cooperates with small and medium sized firms as well as with big companies.

From single components to complete systems ISIT offers design, simulation and manufacturing to their customers. The customers specifies the field of application of the desired products and the profile of requirements.

The execution of the tasks is accomplished in close cooperation with the client. After the realisation of demonstration models and prototypes, the technology developed within the project will be transferred to the customer. Confidentiality of results and exchanged intellectual property is ensured.

The services of ISIT are very profitable for small- and medium-sized enterprises which cannot afford the big capital investments of a technological infrastructure. They can utilise the competence of the institute for development, testing and introduction of necessary technological innovations.

The close cooperation of ISIT with the nearby Innovationszentrum Itzehoe (IZET) allows additional services for start-ups and young companies: IZET provides office and laboratory areas, supports the finding of products needed by the market, helps in preparing marketing strategies and informs about financial support.

The auditorium and lecture rooms of ISIT cover an area of circa 1000 m^2 and are available for conferences, workshops and other events for up to 400 participants.

Service Offers of ISIT in Detail

Studies for development of application-specific sensors, actuators, optical and mechanical components, microsystems, MCMs as well as for the basics of future integration technologies.

Contract research for the development of demonstrators to verify the feasibility of components and systems.

Production of prototypes of integrated subsystems for the development of systems and products.

Design and manufacturing of components and assemblies in pilot- and customer specific series by ISIT.

Design of components and systems utilising industrial foundries (analogue/ mixed-signal ASICs and microsystems).

Transfer of the developed technologies, components and subsystems to industrial technology suppliers for the production phase or the manufacturing in ISIT following industrial quality standards, respectively.

Development of production tools and process technologies for the fabrication of semiconductors and microsystems in co-operation with equipment manufacturers.

Development of individual processes for the production of integrated circuits and microsystems.

Integration of semiconductor components with biological materials.

Module integration of microelectronic systems and preparation of sample series for MCM and Chip-Size packages (CSP).

Mounting and packaging technologies for microsystems, sensors and MCMs.

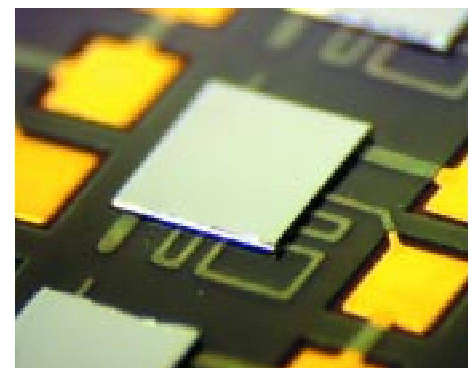
Evaluation of quality and reliability of microelectronic assemblies and power modules.

Failure and process analysis in soldering technology.

Consulting and support for setting up technological production facilities.

Technology-oriented seminars with practical training sessions and customer specific in-house courses.

Ultra-thin flip chip assembly on flexible substrate.



Customers

ISIT cooperates with companies of different sectors and sizes.
In the following some companies are presented as a reference:

ABB, Heidelberg

Alcatel Kirk, Ballerup, Denmark

Alcatel Vacuum Technology, Annecy, France

Alcatel, Stuttgart

APPLIED MATERIALS Santa Clara, USA

Astrium, München

Atotech Deutschland GmbH, Berlin

Basler Vision Technologies, Ahrensburg

Bayer AG, Leverkusen

Beiersdorf AG, Hamburg

BioGaia Fermentation AB, Lund, Sweden

Biotronik GmbH, Berlin

Bodenseewerk Gerätetechnik, Überlingen

Borg Instruments, Remchingen

Bosch, Reutlingen

Bullith Batteries AG, München

Bundesanstalt für Materialforschung und -prüfung, Berlin

Braun AG, Kronberg

CamLine, Petershausen

Cavendish Kinetics B. V., LA´s-Hertogenbosch, Netherland

Condias GmbH, Itzehoe

Conti Temic, Ottobrunn

Corning Frequency Control GmbH & Co. KG, Neckarbischofsheim

Daimler Benz Aerospace, Bremen

DancoTech A/S, Ballerup, Denmark

Danfoss Lighting Controls, Nordborg, Denmark

Danfoss Drives, Graasten, Denmark

Danfoss Silicon Power GmbH, Schleswig

Datacon, Radfeld/Tirol, Austria

Degussa AG, Hanau

Disetronic Medical Systems AG, Burgdorf, Switzerland

Drägerwerk AG, Lübeck

Dräger Electronics GmbH, Lübeck

EADS, Ottobrunn

EADS, Ulm

eBiochip Systems GmbH, Itzehoe

Elmos Semiconductor AG, Dortmund

Epcos AG, München

Eppendorf-Netheler-Hinz GmbH, Hamburg

ESW-EXTEL Systems GmbH, Wedel

EVGroup, Schärding, Austria

Excenga Technologies GmbH, Pfronten

EZL, Limburg

Flextronics International, Althofen, Austria

Fresnel Optics, Apolda

Fuba GmbH, Gittelde

GALAB Products, Geesthacht

GKSS, Geesthacht

Heidelberger Druckmaschinen, Kiel

Heidenhain, Traunreut

HC Planartechnik GmbH, Dortmund

H. C. Starck, Leverkusen

Hella KG, Lippstadt

IBM-Speichersysteme GmbH, Mainz

IC-Haus GmbH, Bodenheim

ICT, München

IDB Technologies, North Somerset, UK

IMS, Wien, Austria

Incoatec, Geesthacht

Infineon Technologies GmbH, München

ISiltec GmbH, Erlangen

JLS Designs, Somerset, UK

Judex Datasystems A/S, Aalborg, Denmark

Kapsch, Wien, Austria

Kember Assiciates, Bristol, United Kingdom

KID Systeme, Buxtehude

Kolbenschmidt Pierburg AG, Neuss

Kugler GmbH, Salem

Kuhnke GmbH, Malente

LEICA, Jena

Litef, Freiburg

Mair Elektronik GmbH, Neufahrn

Max Stegmann GmbH, Donaueschingen

MED – EL, Innsbruck, Austria

microParts GmbH, Dortmund

Miele & Cie., Gütersloh

Motorola GmbH, Flensburg

MRT – Micro-Resist-Technology, Berlin

MST Systemtechnik GmbH, Donauworth

m-u-t GmbH, Wedel

Nanophotonics AG, Mainz

NanoPierce Card Technologies GmbH, Hohenbrunn

Nokia Research Center, Nokia Group, Helsinki, Finland

November AG, Erlangen

Novo Nordisk A/S (NOVO), Bagsvaerd, Denmark

NU-Tech GmbH, Neumünster

OK Media Disc Service GmbH & Co.KG, Nortorf

Orga Kartensysteme GmbH, Flintbeck

Oticon, A/S, Hellerup, Denmark

PAV Card GmbH, Lütjensee

Pohlmann & Partner GmbH, Quickborn

Perkin Elmer Optoelectronics, Wiesbaden

Pharmacia & Upjoh AB (Pharmacia), Strängnäs, Sweden

Philips Semiconductors, Gratkorn

Philips Semiconductors, Hamburg

QinetiQ Ltd, Worcestershire, UK

Quintenz Hybridtechnik, Neuried bei München

Raytheon Anschütz GmbH, Kiel

Robert Bosch GmbH, Salzgitter

RWTH, Aachen

SAES Getters S.p.A., Lainate/Milan, Italy

Scana Holography Company GmbH, Schenefeld

Schott, Landshut

Sentech Instruments GmbH, Berlin

SEF Roboter GmbH, Scharnebek

SensLab GmbH, Leipzig

SensoNor, Horten, Norway

Sentech Instruments GmbH, Berlin

Siemens AG, Bocholt

Siemens AG, Zentrale Technik, Erlangen

Siemens AG, München

Siemens VDO Automotive AG, Karben

SMA Regelsysteme GmbH, Niestetal

SMI GmbH, Itzehoe

Smith Meter GmbH, Ellerbeck

Solid Energy GmbH, Itzehoe

Sparkolor, Inc., Santa Clara, USA

ST Microelectronics, Mailand, Italy

SÜSS Microtec AG, Garching

Technolas, München

Technovision GmbH, Feldkirchen

Tesa AG, Hamburg

Thales Avionics, Valence, France

Thales, Paris, France

Thomsen Bioscience, Aalborg, Denmark

Trioptics GmbH, Wedel

Tronic´s, Grenoble, France

VDMA Fachgemeinschaft Fluidtechnik, Frankfurt

Vega, Schiltach

Vishay, Holon, Israel

Vishay Semiconductor GmbH, Itzehoe

Wabco Fahrzeugbremsen, Hannover

Peter Wolters CMP Systeme GmbH, Rendsburg

Woowon Technology, Korea

W. S. I. Wafer Service International, Evry Cedex, Paris, France

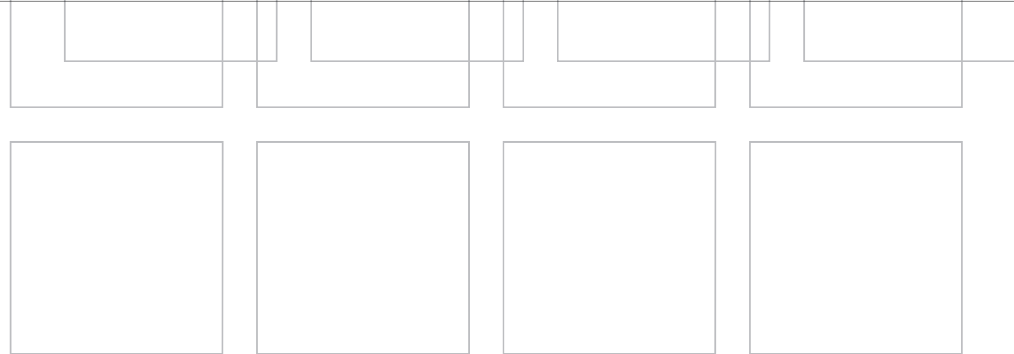
YAGEO EUROPE GmbH, Elmshorn

Offers for Research and Service

Innovation Catalogue

ISIT offers its customers various products and services already developed for market introduction. The following table presents a summary of the essential products and services. Beyond that the utilisation of patents and licences is included in the service.

Product / Service	Market	Contact Person
Testing of semiconductor manufacturing	Semiconductor equipment manufacturers	Dr. Gerfried Zwicker + 49 (0) 48 21 / 17-43 09, zwicker@isit.fhg.de
Chemical-mechanical polishing (CMP), planarization	Semiconductor device manufacturers	Dr. Gerfried Zwicker + 49 (0) 48 21 / 17-43 09, zwicker@isit.fhg.de
Wafer polishing, single and double side	Si substrates for device manufacturers	Dr. Gerfried Zwicker + 49 (0) 48 21 / 17-43 09, zwicker@isit.fhg.de
IC processes CMOS, PowerMOS, IGBTs	Semiconductor industry IC-users	Detlef Friedrich + 49 (0) 48 21 / 17-43 01, friedrich@isit.fhg.de
Single processes and process module development	Semiconductor industry semiconductor equipment manufacturers	Detlef Friedrich + 49 (0) 48 21 / 17-43 01, friedrich@isit.fhg.de
Customer specific processing	Semiconductor industry semiconductor equipment manufacturers	Detlef Friedrich + 49 (0) 48 21 / 17-43 01, friedrich@isit.fhg.de
PowerMOS devices	Electronic industry	Dr. Ralf Dudde + 49 (0) 48 21 / 17-42 12, dudde@isit.fhg.de
Plasma source development	Semiconductor equipment manufacturers	Christoph Huth +49 (0) 48 21 17-46 28, huth@isit.fhg.de
Plasma diagnostics	Semiconductor equipment manufacturers	Joachim Janes + 49 (0) 48 21/17-46 04, janes@isit.fhg.de
Etching and deposition process control	Semiconductor industry	Joachim Janes + 49 (0) 48 21/17-46 04, janes@isit.fhg.de
Ion projection lithography open stencil mask technology and resist processes	Semiconductor industry	Dr. Wilhelm Brünger + 49 (0) 48 21 / 17-42 28, bruenger@isit.fhg.de
E-beam circuit testing and e-beam induced deposition	Semiconductor industry	Dr. Wilhelm Brünger + 49 (0) 48 21 / 17-42 28, bruenger@isit.fhg.de
Inertial sensors	Motorvehicle technology, navigation systems, measurements	Dr. Bernd Wagner + 49 (0) 48 21 / 17-42 23, wagner@isit.fhg.de
Design for commercial MST processes	Micro sensors and actuators	Dr. Bernd Wagner + 49 (0) 48 21 / 17-42 23, wagner@isit.fhg.de
Microvalves for gases and liquids	Analytic, medical technology measurement	Hans Joachim Quenzer + 49 (0) 48 21 / 17-45 24, quenzer@isit.fhg.de
Microoptical scanner	Biomedical technology, optical measurement industry, telecommunication	Ulrich Hofmann + 49 (0) 48 21 / 17-45 29, hofmann@isit.fhg.de
Microoptical components	Optical measurement	Dr. Klaus Reimer + 49 (0) 4821/17-4506, reimer@isit.fhg.de
Mastering and replication of micro structures in plastic	Microoptics, microfluidics	Dr. Klaus Reimer + 49 (0) 48 21 / 17-45 06, reimer@isit.fhg.de

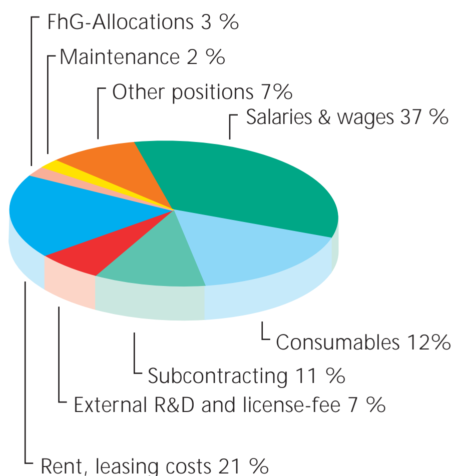


Product / Service	Market	Contact Person
Design and test of analogue and mixed-signal ASICs	Measurement, automatic control industry	Jörg Eichholz + 49 (0) 48 21 / 17-45 37, eichholz@isit.fhg.de
Design Kits	MST foundries	Jörg Eichholz + 49 (0) 48 21 / 17-45 37, eichholz@isit.fhg.de
RF-MEMS	Telecommunication	Dr. Bernd Wagner + 49 (0) 4821/17-4223, wagner@isit.fhg.de
MST Design and behavioural modelling	Measurement, automatic control industry	Jörg Eichholz + 49 (0) 48 21 / 17-45 37, eichholz@isit.fhg.de
Electrodeposition of microstructures	Surface micromachining	Martin Witt + 49 (0) 48 21 / 17-45 41, witt@isit.fhg.de
Digital micromirror devices	Communication technology	Dr. Klaus Reimer + 49 (0) 48 21 / 17-45 06, reimer@isit.fhg.de
Electrical protein and DNA chips	Biotechnology, medical diagnostics, environmental analysis	Dr. Rainer Hintsche + 49 (0) 48 21 / 17-42 21, hintsche@isit.fhg.de
Electrical biochip technology	Biotechnology, related electronics, medical diagnostics, environmental analysis, Si-Chipprocessing	Dr. Rainer Hintsche + 49 (0) 48 21 / 17-42 21, hintsche@isit.fhg.de
Systemintegration	Smart card industry	Wolfgang Pilz +49 (0) 48 21 / 17-42 22, pilz@isit.fhg.de
Secondary lithium batteries based on solid state ionic conductors	Mobile electronic equipment, medical applications, automotive, smart cards, labels, tags	Dr. Peter Gulde +49 (0) 48 21 / 17-46 06, gulde@isit.fhg.de
Battery test service, electrical parameters, climate impact, reliability, quality	Mobile electronic equipment medical applications, automotive, smart cards, labels, tags	Dr. Peter Gulde +49 (0) 48 21 / 17-46 06, gulde@isit.fhg.de
Quality and reliability of electronic assemblies (http://www.isit.fhg.de)	Microelectronic and power electronic industry	Karin Pape + 49 (0) 48 21 / 17-42 29, pape@isit.fhg
Material and damage analysis	Microelectronic and power electronic industry	Dr. Thomas Ahrens + 49 (0) 48 21 / 17-46 05, ahrens@isit.fhg.de
Thermal measurement and simulation	Microelectronic and power electronic industry	Dr. M. H. Poech + 49 (0) 48 21 / 17-46 07, poech@isit.fhg.de
Packaging for microsystems, sensors, multichip modules (http://www.isit.fhg.de)	Microelectronic, sensoric and medical industry	Karin Pape + 49 (0) 48 21 / 17-42 29, pape@isit.fhg
Wafer level and ultra thin Si packaging	Microelectronic, sensoric and medical industry	Wolfgang Reinert + 49 (0) 48 21 / 17-46 17, reinert@isit.fhg.de
Direct chip attach using flip chip techniques	Microelectronic, sensoric and medical industry	Thomas Harder, + 49 (0) 4821/17-4620, harder@isit.fhg.de

Representative Figures

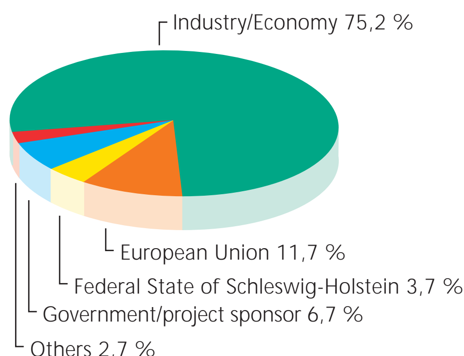
Expenditure

In 2002 the operating expenditure of Fraunhofer ISIT amounted to kEuro 16.420,5. Salaries and wages were kEuro 6.075,5, consumables and other costs were kEuro 10.345,0.



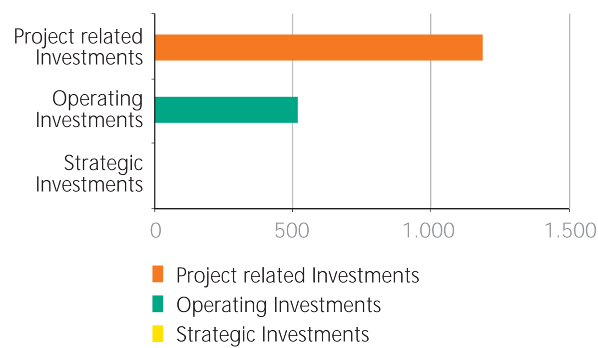
Income

The budget was financed by proceeds of projects of industry/industrial federations/small and medium sized companies amounting to kEuro 12.078,0, of government/project sponsors/federal states amounting to kEuro 1.659,0 and of European Union/others amounting to kEuro 2.316.



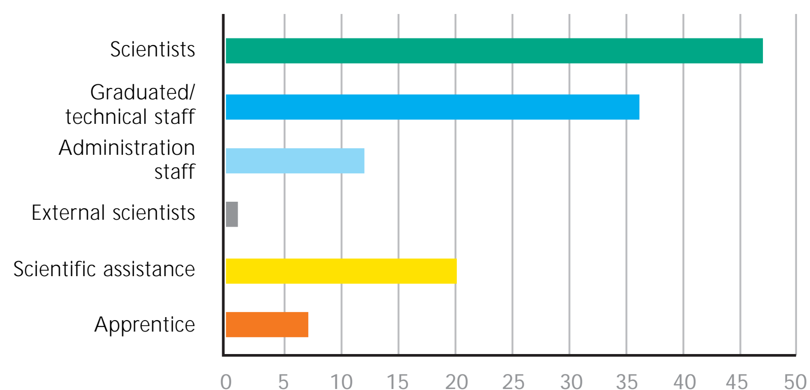
Capital Investment

In 2002 the institutional budget of capital investment was kEuro 1.705,9. The amount of operating investment was kEuro 519,3, project related investments were amounted to kEuro 1.186,6.



Staff Developement

In 2002, on annnual average the staff constisted of 95 employees. 47 were employed as scientific personnel, 36 as graduated/technical personnel and 12 worked within organisation and administration.
1 scientists, 20 scientific assistents and 7 apprentice supported the staff as external assistance.

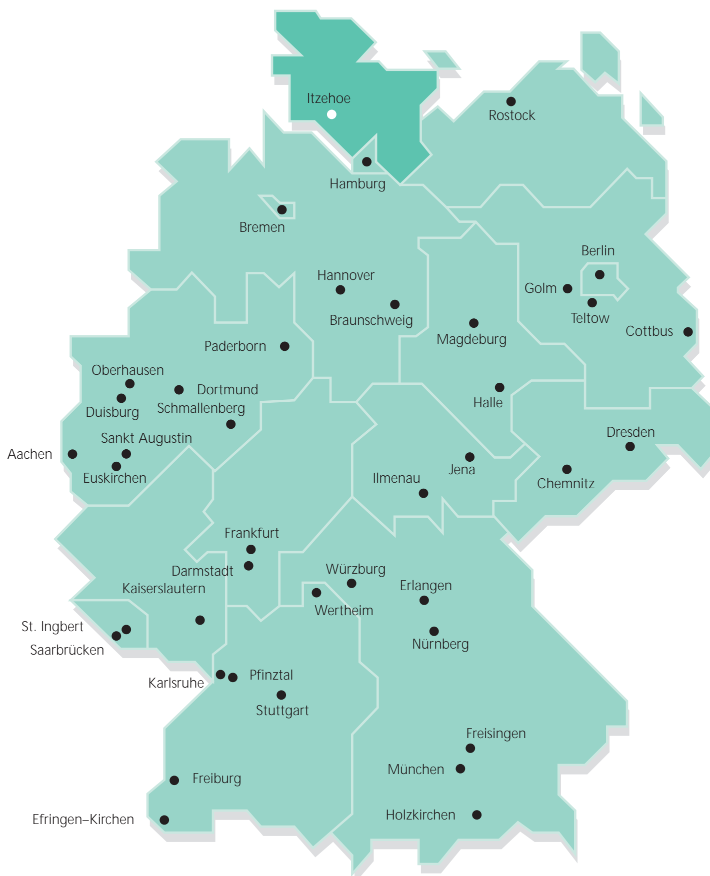


The Fraunhofer-Gesellschaft at a Glance

The Fraunhofer-Gesellschaft

The Fraunhofer-Gesellschaft undertakes applied research of direct utility to private and public enterprise and of wide benefit to society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration. The organization also accepts commissions and funding from German federal and Länder ministries and government departments to participate in future-oriented research projects with the aim of finding innovative solutions to issues concerning the industrial economy and demands faced by society in general.

Locations of the Research Establishments



By developing technological innovations and novel systems solutions for their customers, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. Through their work, they aim to promote the economic development of industrial society, paying particular regard to social and environmental concerns. As an employer, the Fraunhofer-Gesellschaft offers a platform that enables its staff to acquire the necessary professional and personal qualifications to assume positions of responsibility within their Institute, in industry and in other scientific domains.

At present, the Fraunhofer-Gesellschaft maintains roughly 80 research units, including 57 Fraunhofer Institutes, at over 40 different locations in Germany. A staff of some 13,000, predominantly qualified scientists and engineers, work with an annual research budget of around one billion euros. Of this sum, approximately € 900 million is generated through contract research. Roughly two thirds of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. The remaining one third is contributed by the German federal and Länder governments, as a means of enabling the Institutes to pursue more fundamental research in areas that are likely to become relevant to industry and society in five or ten years' time.

Affiliated Research Centers and Liaison Offices in Europe, the USA and Asia provide contact with the regions of greatest importance to future scientific progress and economic development.

The Fraunhofer-Gesellschaft was founded in 1949 and is a recognized non-profit organization. Its members include well-known companies and private patrons who help to shape the Fraunhofer-Gesellschaft's research policy and strategic development. The organization takes its name from Joseph von Fraunhofer (1787 - 1826), the illustrious Munich researcher, inventor and entrepreneur.

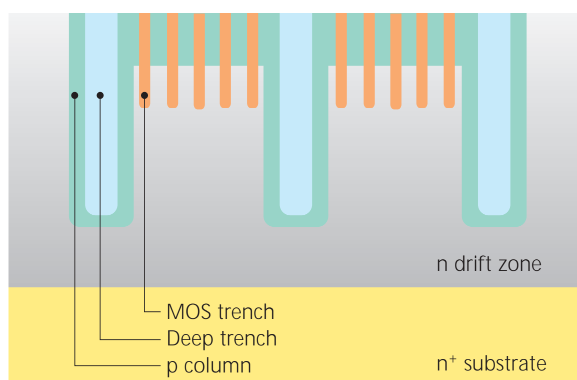
Representative Results of Work

Super Junction Devices for High Voltage PowerMOS

Most of power switching applications in the voltage range up to 200 V are covered by PowerMOS transistors. The conduction loss and thus the On-resistance of a PowerMOS transistor increases with higher blocking voltage requirements. Under blocking conditions, a lower drift zone doping concentration is necessary to allow the space charge region to expand without electrical break down. But the lowering of the doping concentration also increases the drift zone resistance and therefore increases the conduction losses.

In order to overcome this physical effect and to increase the possible voltage range for PowerMOS transistors the so called "Super Junction" (SJ) device was proposed. The principle is based on charge compensation by vertical p-doped columns realized in a n-doped drift zone as shown in figure 1. Under blocking condition the entire volume in-between the p-boped columns has to be fully depleted. By this approach it is possible to increase the concentration of the n-doped drift zone without lowering the maximum break down voltage. Here the critical parameters are the depth and distance as well as the doping concentration of the p-doped columns. By appropriate adjustment of those parameters it is possible to increase the concentration of the drift zone by e.g. a factor of ten.

Figure 1:
Schematic of a Super Junction trench PowerMOS transistor with p-doped columns within the n-doped drift zone.



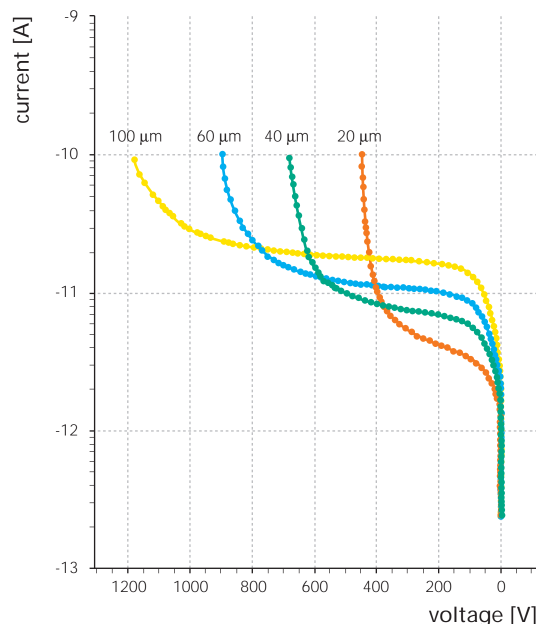


Figure 2:
Calculated diode characteristics for a substrate concentration of 10^{15} cm^{-3} and trench depths of 20 µm, 40 µm, 60 µm and 100 µm respectively. Compared to a planar p-n junction, the breakdown voltage increases from approx. 270 V to about 1000 V at a trench depth of 100 µm.

This means Super Junction PowerMOS transistors showing improved conduction behaviour with lower On-resistance.

Up to now there is only one type of SJ-device (CoolMOS) available at the market. The technological approach is based on multi epitaxial Si growth for the built up of the p-doped columns. In contrast ISIT is developing an alternative method for the realisation of the p-doped columns which is based on dopant outdiffusion from a boron glass deposited along the egdes of deep trenches.

In order to demonstrate the blocking capability of a SJ-device simulations have been carried out for different depths of the p-doped regions. From the simulated diode characteristics shown in figure 2 it is obvious that PowerMOS application a trench depth (p-column) of 60 µm is required with a drift zone concentration of 10^{15} cm^{-3}.

Compared to standard devices the bulk concentration level is one order of magnitude higher. In case of PowerMOS transistors this would result in significant lower On-resistance.

To fabricate Super Junction structures, deep silicon trenches with smallest possible openings have to be provided. For this purpose, the so called Bosch-process, which is mainly used for MEMS applications, was optimized. For trench openings in the micron range, depths up to 60 µm were achieved. The side wall roughness and the CD-loss both are less than 30 nm and 100 nm, respectively. This roughness is removed by an oxidation step with subsequent wet etch in buffered oxide etch.

The required boron concentration of the p-doped columns is in the range of 10^{16} cm^{-3}. The commonly used technique to achieve this doping concentration is ion implantation. However, ion implantation is not recommended since the trench side walls have to be doped also which becomes critical in case of high aspect ratio trenches. In order to realize the required doping level a highly doped boron glas based on BBr_3 or boron nitride was deposited on an oxide which is covering the side walls of the trenches. Since the boron glas behaves as an unlimited doping source special diffusion processes were needed in order to reach the specified doping concentration of 10^{16} cm^{-3} for the p-columns by outdiffusion. The doping profiles for the p-doped columns are displayed in figure 3. The profiles have been measured by spreading resistance probe for different outdiffusion temperatures in the range of 1000 °C - 1200 °C. By appropriate adjustment of the thermal budget for the outdiffusion process the required doping profile can be tailored.

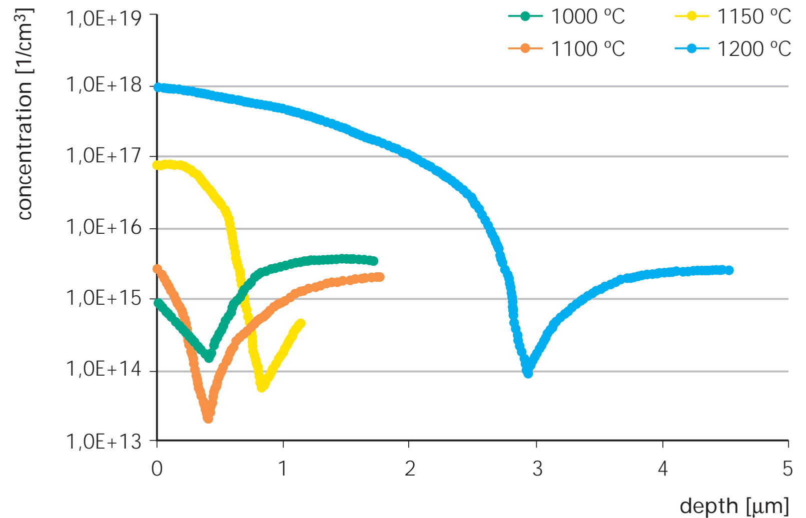


Figure 3:
Doping profiles measured by preading resistance probe for different outdiffusion temperatures.

The filling of the trenches is realized by Poly-Si deposition with a LPCVD process. As depicted in figure 4 conformal step coverage and excellent filling behaviour have been achieved even for trench depths of 60 µm.

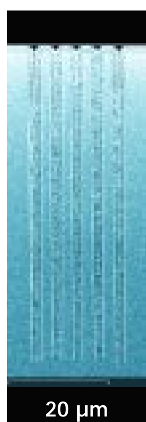


Figure 4:
Filling of 60 µm deep and 2 µm wide trenches with poly-silicon.

In a next step first SJ-devices will be fabricated for design rule verification. The geometrical rules like pitch and depths of the trenches have to be correlated with doping profiles of p-columns and drift zone in order to reach the charge compensation requirement for a specified breakdown voltage.

Representative Results of Work: IC Technology

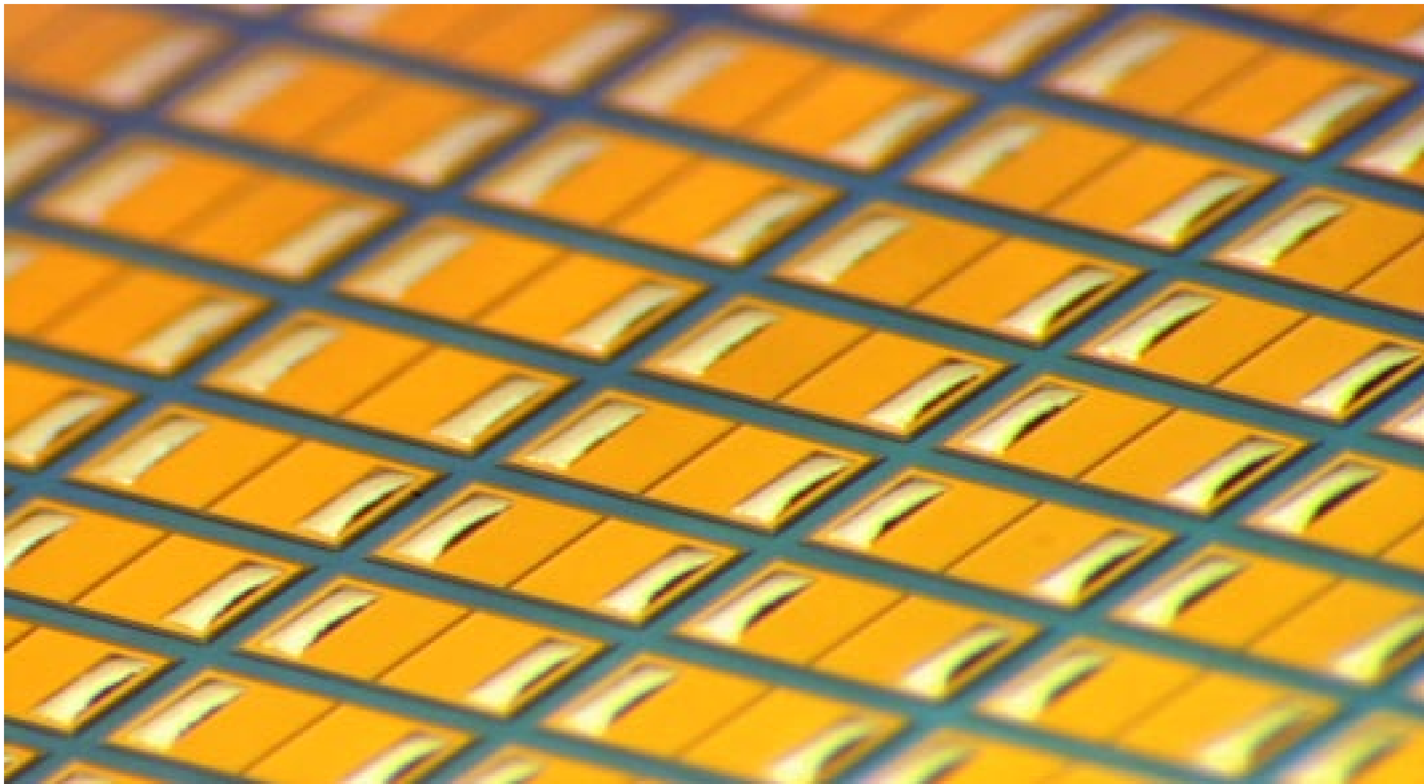


Figure 2
Top view of chip capacitors 20 mils by 40 mils in size. The outer termination is defined by solder bumps.

Passive Components: High precision chip-capacitors for GHz-application

The implementation of resistors or capacitors into standard IC-processes is quite common and being used since many years. In typical IC-processes resistors and capacitors are defined by doped poly-Si or diffusion regions and intermetal or interpoly-Si dielectrics, respectively. The tolerance values are mainly related to the layer thickness uniformities and the geometrical pattern transfer precision by lithography and etch structuring. In standard IC-processes the tolerances of passive devices are typically in the 5 - 10 % range.

The special capacitors discussed here are focused on RF-applications for e.g. mobile phones and contactless smard cards. Here the use of high precision and high Q-value capacitors is mandatory for antenna impedance matching in order to avoid costly trimming of the device. Also, high self resonant frequency SRF is a further requirement by minimizing L-C parasitics with advanced assembly techniques.

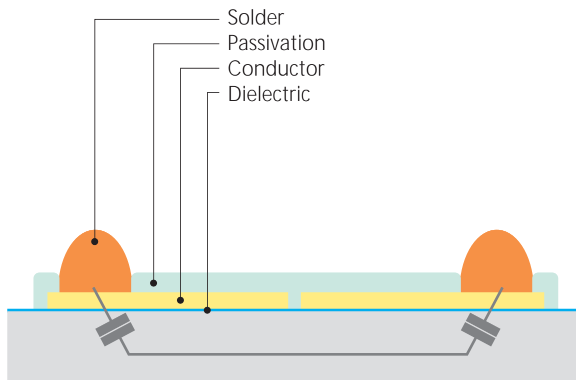


Figure 1:
Cross sectional drawing of a chip capacitor with solder bumps.

The device principle is shown in the cross sectional drawing of figure 1. The base plate of the capacitor is defined by a highly doped Si-substrate with SiO_2 as the dielectric layer on top. Depending on the capacitance value used the oxide thickness is varied in the range of 50 - 2500 nm with a min-max tolerance of +-1 %. The top plate of the capacitor consists out of a 3 layer metal stack with a solderable Cu-layer on top. The low-k passivation is specified for low pin-hole density and prevention of lateral solder diffusion along the capacitance top plate. The outer termination of the device is realized by solder bumps based on solder paste printing and reflow. The capacitor is designed for upside down flip chip assembly on printed circuit boards. With geometrical dimension of 20 by 40 mils (approx. 500 x 1000 µm) a capacitance range of 0.2 pF up to 180 pF have been reached. For smart card applications the devices are thinned down to 150 µm compared to a standard thickness of 320 µm. The typical appearance of capacitor devices with solder bump termination is illustrated in figure 2.

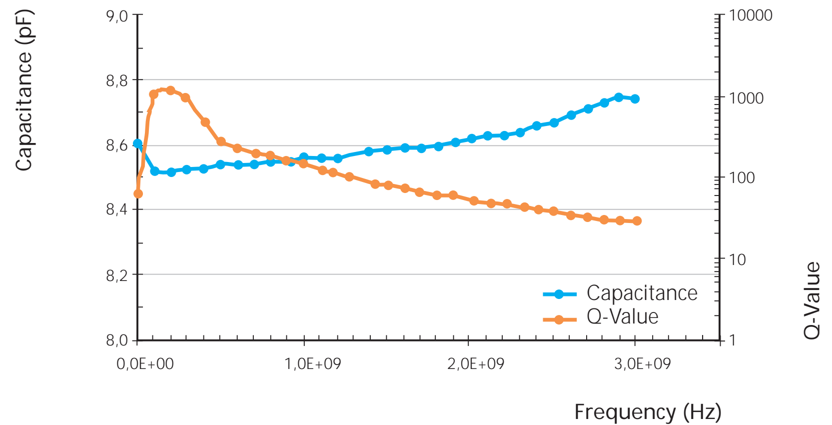


Figure 3
Characteristic of capacitance and Q-value versus frequency for a RF chip capacitor with nominal 8.5 pF.

For practical application the capacitance stability versus frequency as well as a high Q- and SRF-value are of most importance. Especially the capacitance value shows an excellent stability up to 3 GHz, compared to other leading RF-devices. The performance of the Q-value is excellent also, reaching more than 20 at a frequency of 3 GHz. The RF-capacitor performance in terms of capacitance stability and Q-value versus frequency is displayed in figure 3.

The fabrication of chip–capacitors for RF-applications is based on standard semiconductor processes. Compared to other technologies chip capacitors are beneficial in term of cost efficient fabrication methods, high reproducibility with tight tolerances and flexible for product variations.

Representative Results of Work: IC Technology

Patterning of Magnetic Hard Disks with Ion-Projection

The rapid increase of areal storage densities in magnetic hard disk drives may in future be limited by the thermal instability of small magnetic domains which is known as superparamagnetism. Storage media featuring magnetically independent bit cells consisting of prepatterned single magnetic domains would allow to further postpone this limitation.

Patterning of these nano magnetic dots by using ion irradiation of an ion projection system was the aim of a research activity between companies: IBM, IMS-Vienna, Leica-Jena, together with research institutions: IMS-Chips Stuttgart and Fraunhofer-ISIT.

Co/Pt multilayer thin films with strong perpendicular anisotropy and out-of-plane coercivities of 5-11 kOe were magnetically altered in areas of local ion beam interaction. The ion irradiations were performed by ion projection through silicon stencil masks fabricated by silicon on insulator (SOI) membrane technology. The ion projector at ISIT was operated at 73 keV ion energy and with a 8.7-fold demagnification. Different ion species (He, Ne, Ar, Xe) have been used. Magnetic islands smaller than 100 nm in diameter were resolved in the Co/Pt films by means of magnetic force microscopy.

Monte-Carlo simulations of the intermixing process with the T-dyn software code resulted in

Figure 1:
IBM microdrive disk.

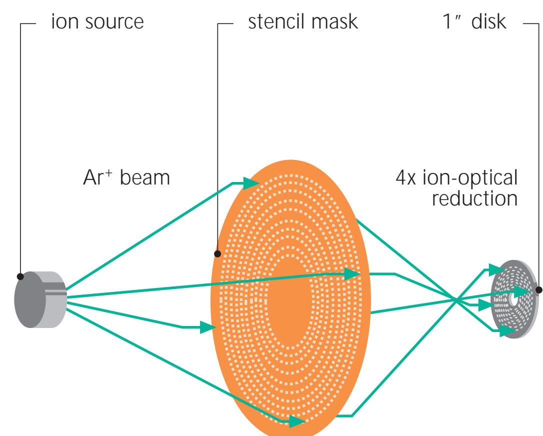


Figure 2:
Ion projection direct structuring (IPDS) for patterned magnetic media.

the required ion doses to create predefined losses of Co at the Co/Pt multilayer interfaces. The amount of these Co vacancies is responsible for the reduction of coercivity giving the necessary magnetic contrast. The simulation predicted that the intermixing efficiency of 73 keV Ar+ ions is 100 times stronger compared to 73 keV He^+ ions. This has been confirmed by experiment and subsequent evaluation of the Co/Pt films by means of magnetic force microscopy.

Using the ion projection technique concentric data tracks including head positioning servo informations were patterned onto a 1″ glass disk as used in the IBM microdrive™ which was coated with Co/Pt multilayers. In a single exposure step multiple tracks within an exposure field of 17,5 mm in diameter were structured by 4 x 10^{13} Ar^+/cm^2 at 45 keV using a 4 - fold demagnification.

The high intermixing efficiency of Ar^+ or Xe^+ ions and the high speed parallel pattern transfer of ion projection give a significant advantage with respect to machine throughput which will be mandatory for an economic mass fabrication process for prepatterned magnetic media.

This work has been supported by the German Ministry of Education, Science, Research, and Technology (BMBF) under grant number 13 N 7837.

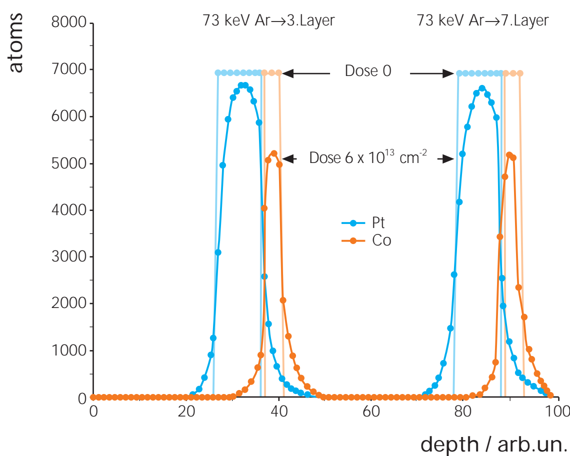


Figure 3:
T-Dyn simulation of ion intermixing of 10 Å platinum / 3 Å cobalt sandwich layers. Plotted are the atom dstributions of the 3rd and 7th sandwich layer after bombardment with a dose of 6 x 10^{13} A^+/cm^2 at 73 keV energy. The number of atoms correspond to an atomic mono layer within an area of 500 nm^2.

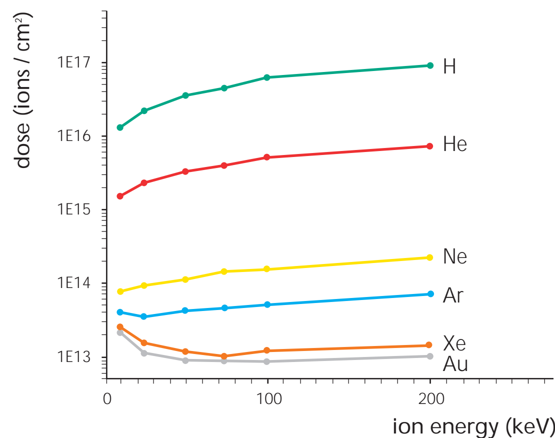


Figure 4:
Ion doses for different ion species and energies leading to the same degree of ion intermixing, revealed by T-dyn simulations. The intermixing is defined by the cobalt-concentration at the 5th interlayer (in the middle of the stack, 82 Å below the surface) beeing reduced to 80 %.

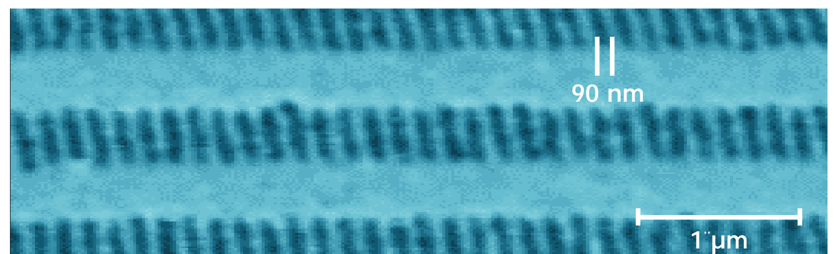


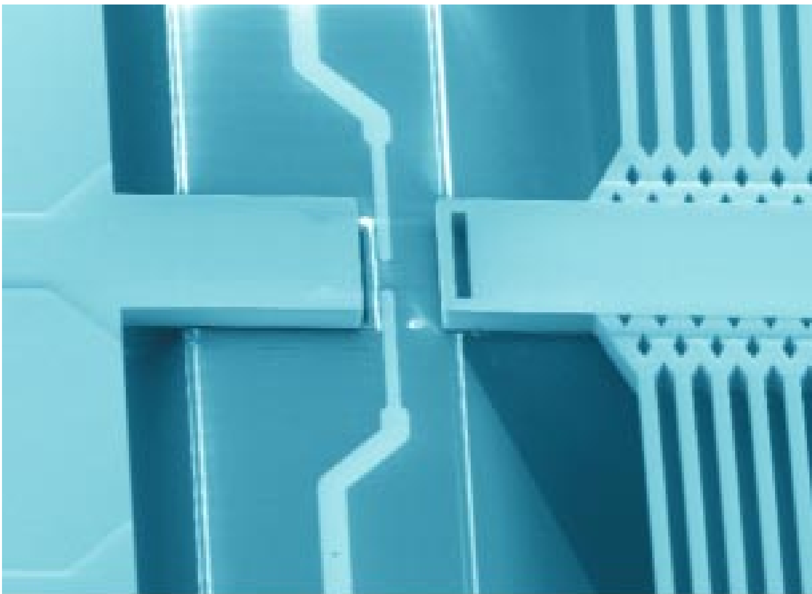
Figure 5:
Magnetic force microscopy of IPDS exposed tracks on microdrive disk. 45 keV argon ions; exposure dose 4x10^{13} ions/cm^2.

Study on Bistable Thermomechanical Drives

Since the introduction of thermomechanical drives to MEMS in 1988 different applications have been proposed. Thermally driven micro actators have been realised up to now normally for the construction of micro devices which requires a maximum of force. Typical examples are micro valves and micro switches. Beside the simple construction and process integration, the generation of high mechanical forces and large actuation distances are great advantages of these kind of micro actuators. Despite of the big advantages of thermoelectrically drives, the specific restrictions of this kind of driving principles inhibits very often their use.

Since these devices consumes an electrical power of at least 200 mW (micro switch) up to 1000 mW (micro valves) in the "on" stage, those devices could be used only in some applications. Due to the large thermal energy dissipation array arrangements and small area devices could be not realised.

Figure. 2:
Centre area of a µ-relay. The complete µ-relay consist of two actuators, the first actuator moves laterally over the substrate surface, the second actuator moves vertically up and down.



A bistable approach can overcome these limits. In these concepts only during the short switching period the power is necessary. In our concept the bistable behaviour is achieved by using an additional actuator which clamps the switching device in the on stage. (Project: MELODICT funded by the EC, project number: IST-1999-10945) The use of two actuators in one µ-relay offers the opportunity to combine both, large stroke length and high contact forces. The arrangement of the two actuators allows the construction of µ-relay which could be fixed in two stable stages without further power consumption. Therefore the µ-relay requires only electrical power during the switching cycle.

The complete relay consists of two thermally driven actuator, the first actuator moves horizontally over the surface while the second actuator moves perpendicular to the surface up and down. Both actuator are arranged in a way, that the lateral actuator can be moved under the activated vertical actuator and can be clamped by the vertical actuator when this actuator moves downwards.

The electrical contacts are located beside the vertical actuator and can be closed by the clamped lateral actuator. (z-actuator figure 1).

For switching the µ-relay into the on stage, both actuators will be activated. Therefore the central plate of the lateral actuator will be moved under the central plate of the vertical actuator (figure 2).

For complete closing the electrical contacts the vertical actuator will be switched off and moves downwards to the substrate and clamps the lateral actuator on the contacts. Finally the lateral actuator can be also switched off (figure 3).

For switching into the off state also both actuators will be first activated but switching off will start with the lateral actuator. The movement of the lateral actuator into the initial position opens also the electrical contacts.

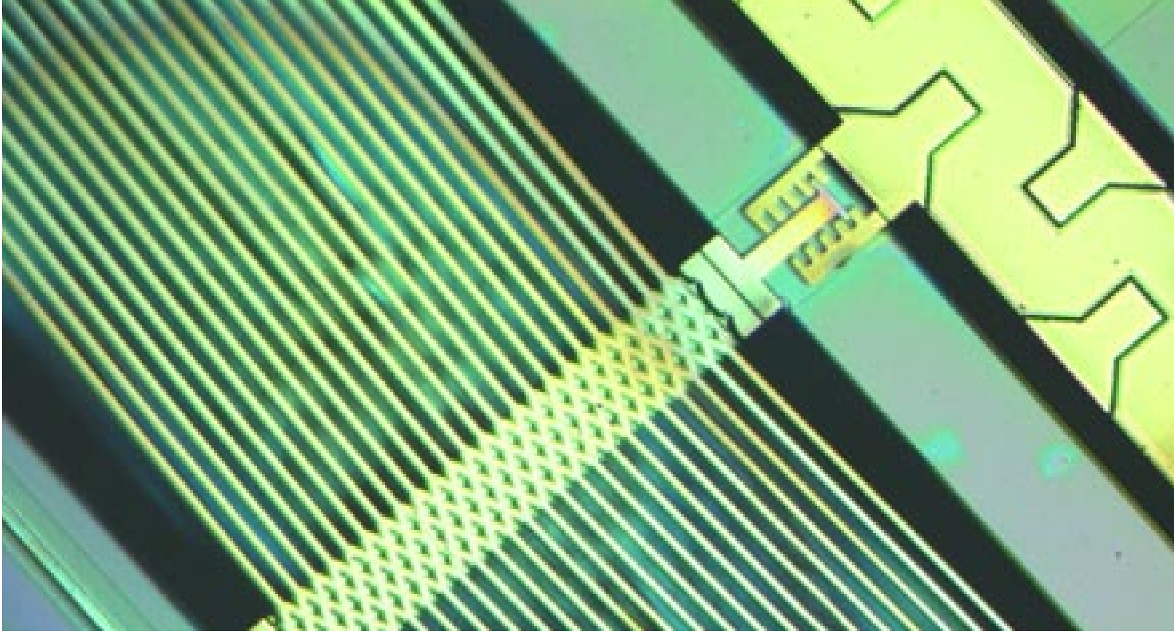


Figure. 3:
The picture shows a clamped lateral actuator by the vertical one. In this example the lateral contacts are closed by the actuator.

Due to the use of two actuator relatively large strokes of the relay can be combined with a high contact forces. For the calculations a model based on the model of a double side clamped bridge was used. Using the lateral actuator a relay stroke of up to 60 - 70 µm has been measured, while contact forces which are generated by the vertical actuator of 10 - 15 mN per contact are achieved. The required chip area for realising both micro actuators is about 0.5 mm x 2.5 mm, and therefore as small as the smallest electrostatically driven µ-relays. Depending from the accurate dimensions of the relay switching time faster than 25 ms and a power consumption of lower than 200 - 300 mW during switching are possible. The electrical power is only required during switching.

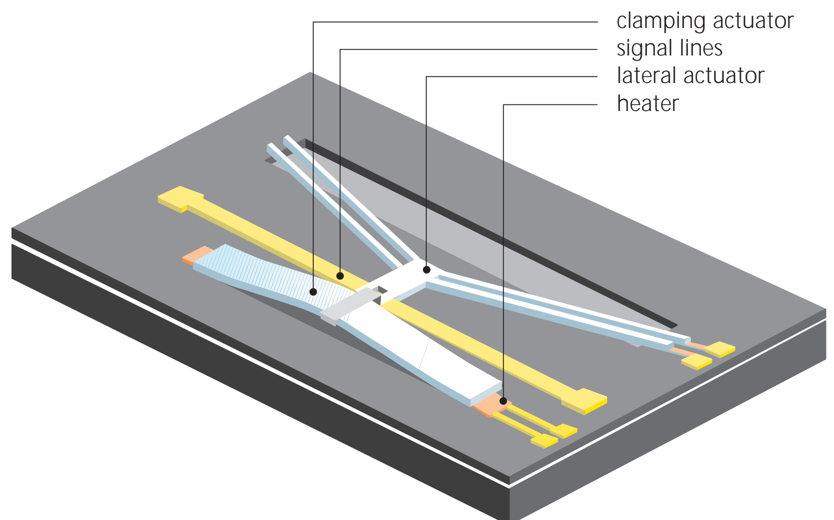


Figure 1:
3D-view of the µ-relay. The complete µ-relay consist of two actuators, the first actuator moves laterally over the substrate surface, the second actuator moves vertically up and down. Both actuators are thermally driven by a heater located under the nickel structures. The µ-relay is here shown in the on-state.

Glass Flow Process GFP
A Novel Micromachining Technology for Structuring Borosilicate Glass Substrates

For the manufacturing of microstructured glass substrates a novel clean room compatible micromachining process technology has been developed. With this Glass Flow Process (GFP), which is based on viscous deformation at temperature above the glass transition temperature Tg, any surface topography available on a silicon substrate, like e.g. microfluidic channel structures (figure 1), can be moulded into bondable alkali-borosilicate glasses. Beside complete replication of silicon structures into glass this technique allows also the fabrication of optical micro lens arrays with high aspect ratios and minimal spacings (figure 2).

Figure 1:
Microfluidic channel structures in borosilicate glass: substrate with step height of 150 µm and minimum channel width of 20 µm.

The GFP technology is based on standard MEMS processes (figure 3). First a pattern is etched into silicon using deep reactive ion etching (DRIE). Then an alkali-borosilicate substrate (Schott BOROFLOAT®33) is hermetically sealed to the silicon preform by anodic bonding under vacuum. The bonding process is followed by an annealing step in an atmospheric furnace system. The temperature for this GFP step is typically well above the glass transition temperature of Tg = 525°C. Thus, the viscosity of the glass is drastically lowered. The pressure difference leads to slumping of glass material into the silicon cavity (figure 4) until the cavity is completely filled so the original silicon topography is moulded into glass. The minimum feature size as well as the structure height is hereby limited only by the previous silicon structuring process. Finally the silicon wafer is removed by wet etching and the backside of glass substrate is mechanically planarized.

Table 1:
GFP microlens specification.

lens material	alkali-borosilicate glass (Pyrex, Borofloat)
refractive index n	n = 1,473
optical transmission	325 ... 2600 nm
lens radius r_L lens height h_L lens profile minimal spacing	5 ... 5000 µm up to 500 µm spherical, parabolic 10 µm
focal length uniformity Δf surface roughness rms lens abberation lateral adjustment accuracy	< 2,5 % < 2,5 nm < λ/2 < 1 µm

If the slumping process is stopped before reaching the bottom of the cavity, the resulting shape of the glass surface is spherical and can be used as a microlens. These lenses can be fabricated with high aspect ratios and central heights up to 200 µm without costly and time consuming dry etching of glass substrates. This contactless forming process results in a very low surface roughness. The resulting lens profiles are characterised by line scan measurements and show a slight elliptical deviation in the outer region of the lenses. All relevant optical parameters are summarized in table 1.

Introducing this GFP technology to MEMS processing enables the deep structuring of glass

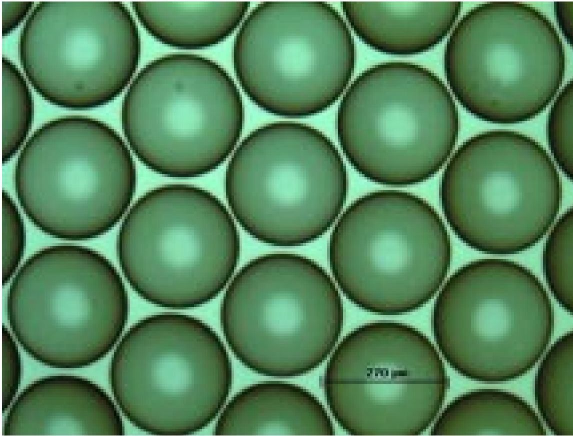
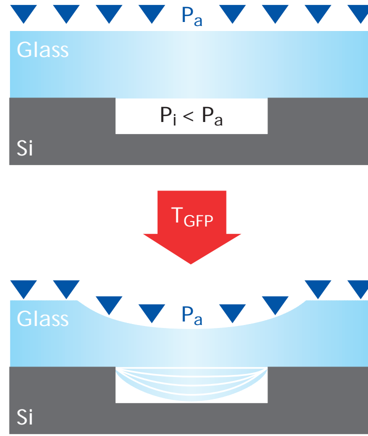


Figure 2:
With GFP technology the high volume manufacturing of dense micro lens arrays with high aspect ratios is possible (lens radius r_L = 270 µm, lens height h_L = 65 µm).



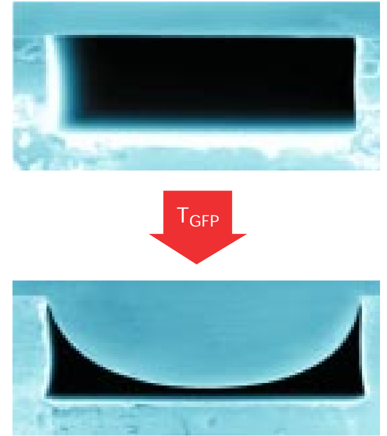


Figure 4:
Schematic (left) and actual SEM picture (right) before and after the thermal treatment of the bonded glass-silicon stack. The glass forming takes place at temperatures well above Tg, where the viscosity of the borofloatglass is drastically lowered. The pressure difference between silicon cavity (vacuum) and oven atmosphere (~1 bar) leads to a continuous movement of the glass material: the interfacial glass surface slumps into the silicon cavity.

substrates and opens up a wide range of new applications. Since whole glass substrates can be fabricated by this new technique complete microoptical stacks can be mounted by anodic bonding of silicon and microstructured glass wafers. New types of optical packaging solutions or complete stacked microoptics can be realised in this new process.

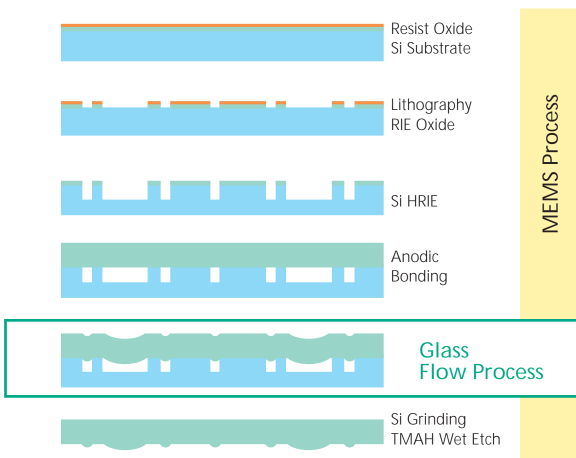


Figure 3:
All GFP technolgy steps are based on standard MEMS processes.

Representative Results of Work: Microsystems Technology

Silicon Etching of Deep Trenches with High Aspect Ratio

The utilisation of deep silicon etching in MEMS and IC-Technology becomes more and more important for various device purposes. For MEMS deep reactive ion etching (DRIE) is already been used mainly for surface mechanical applications in the field of sensoric, actuatoric and micro-optical components. Also for IC-Technology new device architectures are taking advantage of deep trenches for e.g. lateral isolation, trench power devices, passive components and DRAM applications. Typical requirements for the etching of deep trenches in Silicon are ranging from tens-up to hundreds of microns. The use of conventional Silicon dry etch processes based on chlorine or bromine chemistry attain nearly vertical structures, however the achieved etch rates are typically in the order of 200 nm/min only. Those etch rates are insufficient for deep trench etching in mass production.

Applying dry etch processes using fluorine chemistry etch rates in the range of microns per minute are reached. Here, the etch process suffers from low selectivity against resist and silicon oxide at room temperature. The well-known Bosch-process is characterized by alternating etch and polymer deposition cycles. Both, high etch rates and high selectivities against the masking layers were achieved in this case.

In standard MEMS applications the so called Bosch-process is utilized to generate structures with dimensions of several tens of microns. For this purpose the process induced sidewall roughness of about 200 nm and a CD-loss in the range of microns is tolerable. For more advanced applications with structures in the micron and sub-micron range, those CD-variations are not acceptable. Aiming at these dimensions ISIT improved the Bosch-process for high aspect ratio deep trench etching in the sub-µm regime. For trench openings in the µm-range we achieve a side wall roughness and a CD-loss of less than 30 nm and 100 nm, respectively. In the sub-µm range the losses are less than 20 nm. Moreover, we enabled the control of the side wall slope from nearly vertical to a conical profile, which is important for trench filling purposes.

The work performed at ISIT demonstrates the possibility to etch trenches with aspect ratios up to 60:1. Figure 1 shows trenches of 1 µm and 2 µm widths with vertical and conical profiles etched with an improved Bosch-process. Especially DRIE for trenches with dimensions down to 0.4 µm has to be highlighed as shown in figure 2. It has to be mentioned that special etching strategies are required to achieve those excellent results. In our experiments the critical dimension was limited by lithografic resolution. It is expected that the etch process has the potential to be used for further down scaling of geometrical dimensions.

With the availability of a DRIE process for high aspect ratio Silicon structuring in the sub-µm range a powerful tool for the development of new device architectures is provided.

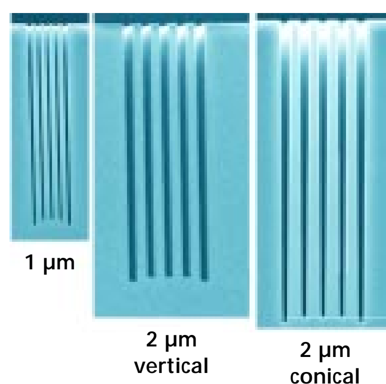


Figure 1:
DRIE for Silicon trenches of 1 µm and 2 µm widths with vertical and conical profiles.

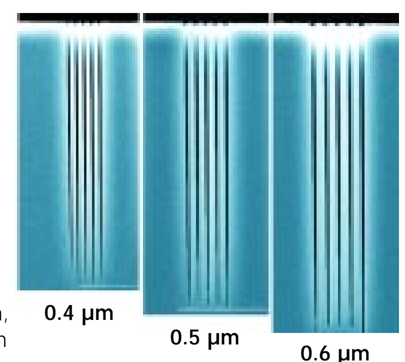
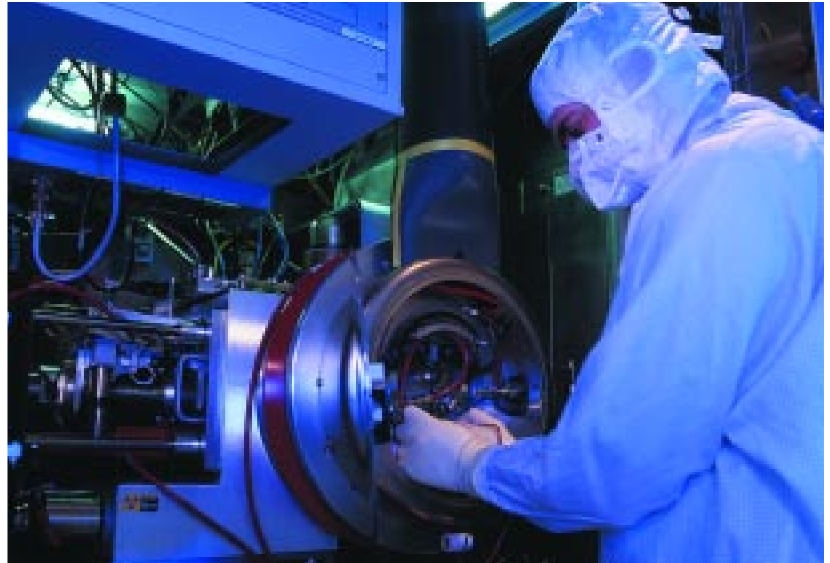


Figure 2:
DRIE for Silicon trenches of 0.4 µm, 0.5 µm and 0.6 µm widths with aspect rations up to 60:1.

Access to Microsystem Production, Co-operation within EUROPRACTICE

New products based on microsystem technologies (MST) lead to an annual growth rate of the MST market that is comparable to the growth rate of the world-wide semiconductor market (on average 15-20 % p.a.). Since the overall MST market still amounts to approx. 10-15 % of the semiconductor turnover, this high growth rate makes Microsystems to a very promising market. Additionally, in more and more areas MST is becoming a major enabling technology that is decisive for the introduction of new and advanced products and services. The actual development of MST markets will be determined by how accessible that technology will be to the user community, how well these techniques can be transferred into new products and how many engineers are skilled and experienced enough to apply these new techniques.



Maintenance at semiconductor process equipment.

Since several years the European Union is supporting the transfer of MST developments into actual new products and services. Together with Bosch and HLPlanar ISIT is partner in the project AMICUS to offer manufacturing services for new Microsystems.

Within AMICUS the following activities have started:

- Providing a market- and product-oriented access to Microsystems technology. A defined route from first prototypes to a product is given and the customer is accompanied on this way. Standardised technologies and processes are offered for product development within a reasonable time. Hence, small and medium-sized enterprises can rely on well-proven processes and may concentrate on the functionality and application of their devices.

- Adding new developments in the production processes to the existing services. Ongoing projects as well as new users can profit from these adjustments by reaching a higher accuracy and quality level of their systems.

- Supporting users in the development of complete systems beyond the underlying functionality of the device. The knowledge of the EUROPRACTICE partners helps the customers to expedite the market introduction of their products and to adjust their developments to dedicated applications.

- Using established process steps for the generation of a new standardised process sequence. Once a standard flow is established, new products can be developed and introduced to the markets.

The AMICUS project and the work of ISIT as a competence centre in sensor technologies is aiming to accelerate the uptake of existing and emerging microsystem technologies in new market areas by combining existing MST manufacturing and application Know How. Meanwhile ISIT could realise several new contracts for technical studies, MST prototyping and production transfer. In 2002 the AMICUS activities during fairs and workshops have lead to five new contracts. Several promising contract negotiations are still ongoing and will finally lead to additional projects. Also customer support starting from application knowledge in the field of physical sensors that is organised within ISIT in the EUROPRACTICE part of a competence center has already initiated several new industrial projects.

Representative Results of Work:
IC-Design

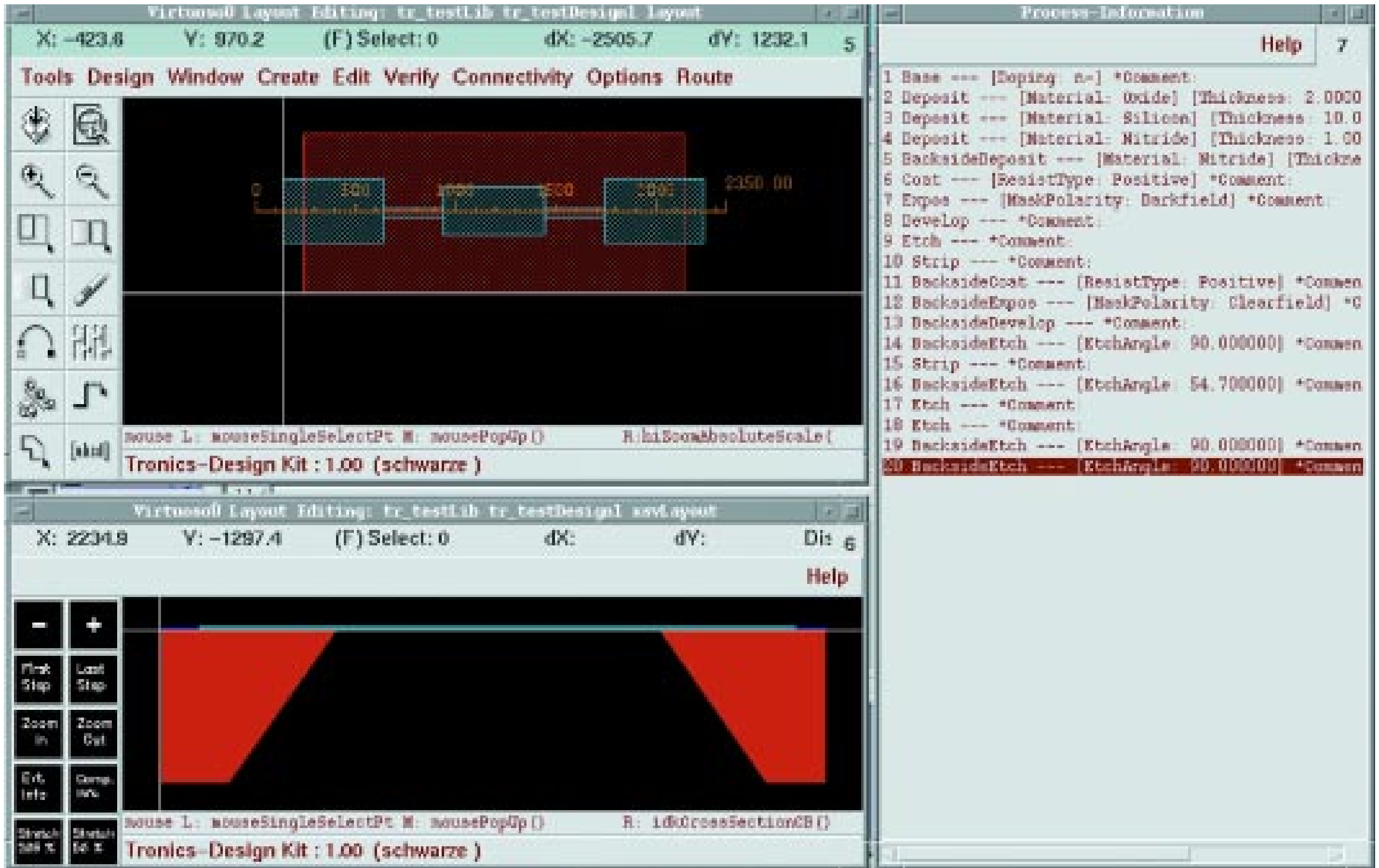


Figure 1:
Graphical user interface (GUI) of the cross-section viewer integrated in the realized design-kit.

Design-Kit for Microsystem Designers

Modern design of ICs is established since two decades in a way that designers use design-kits, distributed by the IC-fab of choice, to realize the electronics. The design-kit is a software add on written for one of the IC-design software packages, that includes specific data of the technologies the IC-fab offers. In the beginning there were only the technology file with the names of the layers, the design rules for the DRC and the parameters of the models. Nowadays design-kits are more complex, often the complete enviroment of the IC-design software is adapted and includes design examples, all kinds of documentations (.html or .pdf), tutorials for beginners, parameterized cells, and a set of verification tools.

With the first MST-fabs the idea to provide such a tool available for MST-designers is covered to accelerate the design and lower the hurdles for first-time users. The development of such a design-kit is part of the European project MEMSOI2 (IST-2001-33443) for the MST-fab Tronic's in France for their optical SOI technology.

The tool is fully integrated within the design environment of CADENCE, and includes a variaty of special add ons which accelerate the designflow from idea to final maskdesign. The design-kit simplifies a couple of design steps with a more intuitive graphical user interface based on the specific technological process. A cross-section viewer allows a general insight into the process to check the functionality of the particular device.

A number of parameterized layout cells (p-cell) like bars, massive and perforated blocks, round plates are available to create the design in an extremely flexible way. In a further step those special p-cells will include additional information that allows an easy-to-use interaction between the design environment and the mechanical FEM-simulator (ANSYS). Based on the process related material properties (youngs modulus, density, ...) and the geometrical data of the mask layout a software-interface has been realized which allows users to perform a stress and modal analysis with ANSYS, by simply click on a single button.

Due to the fact that the design-kit is directly integrated within the CADENCE environment by using its own programming language SKILL, the entire size of the software package is minimized to a couple of 100 kBytes only. Professional licensing and user-friendly installation is included, too.

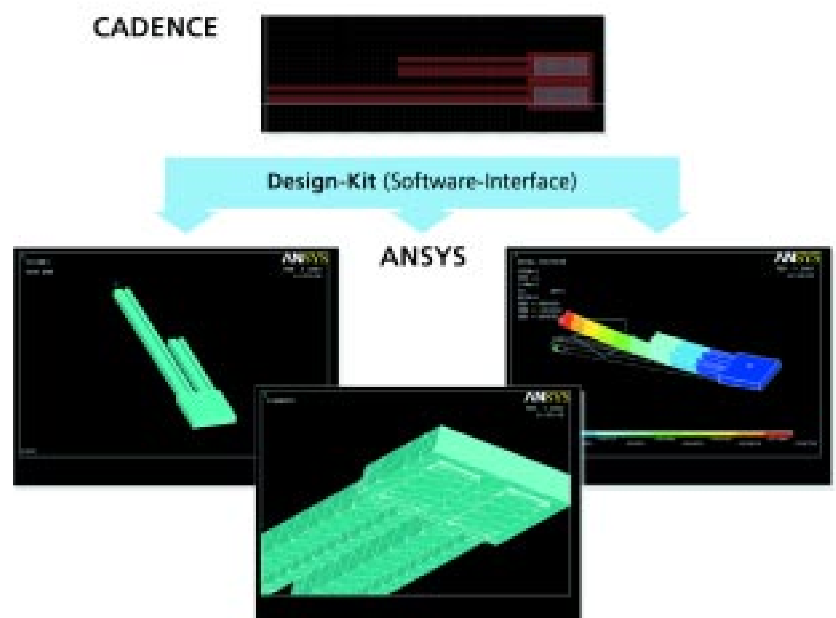


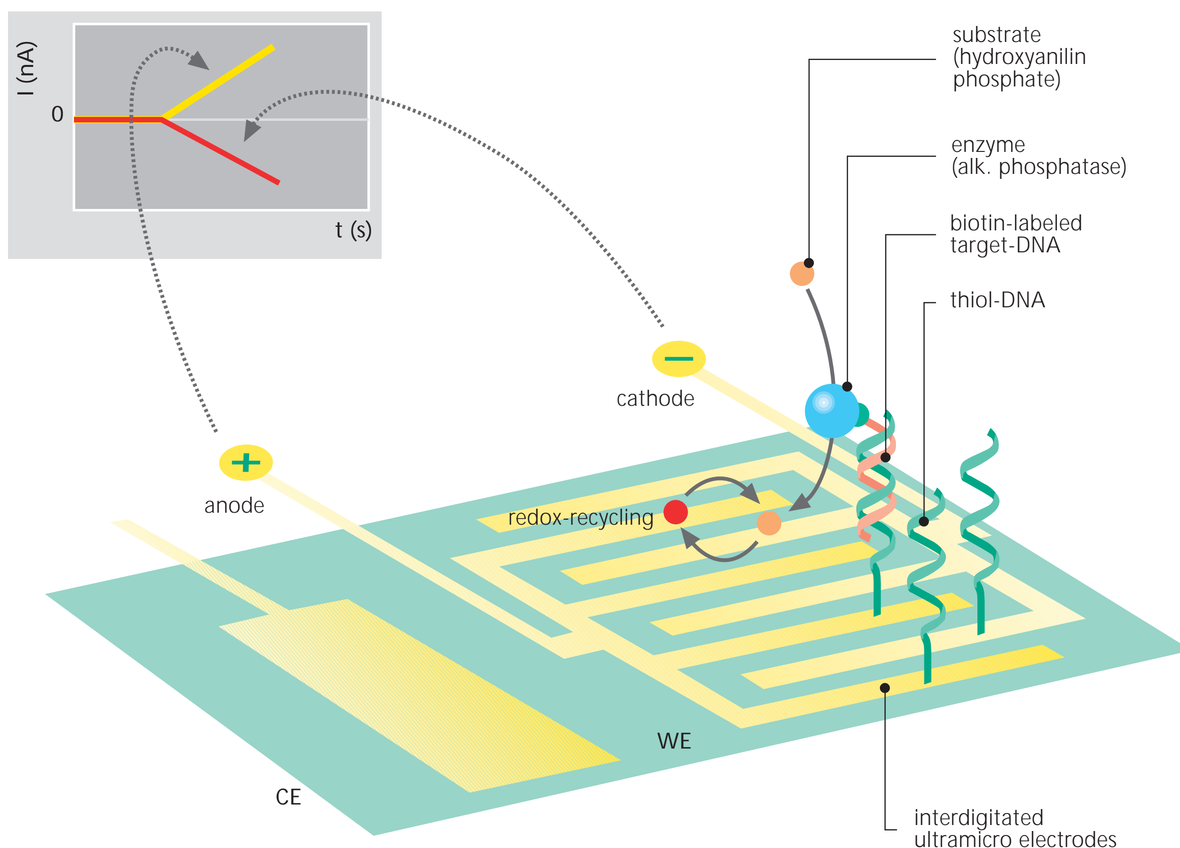
Figure 2:
Layout data from Cadence can simply be imported into Ansys in order to run FEM analyses.

Electrical Manipulation of DNA Molecules

Electrical biochips, developed at ISIT, offer several advantages regarding the realization of biochemical analytics systems. One favourable point is that it is possible to completely omit optical components. The biochips are made from silicon in an established semiconductor process in mass production and provide the basis for the cost effective production of robust biosensors.

Ultramicro electrodes present on the chips are used primarily for the electrochemical detection of biomolecules by enzyme enhanced redox recycling (figure 1). For this purpose capture molecules are applied to and anchored on the chip in a position specific manner. This is made possible by the use of precision robotics and optimized surface chemistry. Biomolecules are chosen which enable the binding of molecules for detection with high specificity. Mechanism present in nature, e.g. in the immune system, are used for the specific recognition of these target biomolecules. In case of DNA detection such molecules can consist of short oligonucleotide strands of complementary sequence. In case of protein detection suitable antibody molecules are employed. The target molecule containing sample is applied to the chip and the molecules are specifically bound by the capture molecules. In the following an enzyme is additionally attached to the complex bound target molecule. The enzyme now converts a substrate and produces a substance (hydroxyanilin) which can be

Figure 1:
Schematic depiction of the electrochemical detection on electrical biochips. The graphic shows the enzyme labeling of biomolecules captured on the chip, e.g. DNA.
The enzyme produces p-aminphenol for the redox recycling and generates an electrical current signal.



detected in a highly sensitive electrochemical reaction. The signal consist of an electrical current detectable by specialized electronics and directly suitable for computer compatible signal analysis and evaluation. Here the interdigitated structure of the embedded gold electrodes on the chip is a requirement for the sensitive detection.

Beside the electrochemical detection principle the presence of electrodes on the silicon chips enable additional new possibilities to actively control the detection of biomolecules. These possibilities are based on the fact that some of the detected biomolecules are charged particles. DNA molecules as well as proteins exhibit a surface charge due to their composition and structure. This charge can be used to manipulate the molecules by applied electrical fields. DNA is negatively charged and directed electrical fields move the molecules toward the chip surface. This procedure increases the local concentration of DNA and therefore reduces the time needed for specific binding (hybridization) and enhances the sensitivity in a given time frame. Vice versa a controlled repulsion can be effective for enhancing the specificity (stringency) of the binding reaction. Alternating electrical fields are used to prevent the generation of electrical double layers (figure 2). Both methods of attraction and repulsion allow to speed up the sensitive detection of biomolecules with electrical biochips and make it more specific as it would be possible with other passive biosensor systems.

The outlined technology was developed in the scope of the BMBF joint project SIBANAT. The project won the "Jack Raper Award for Outstanding Technology Directions Paper" in 2003.

Two preset potentials are applied alternating between the interdigital electrodes and the frequency of switching the potentials is being varied. The alternating field enables the effective attraction of fluorescence labeled DNA toward the electrodes.

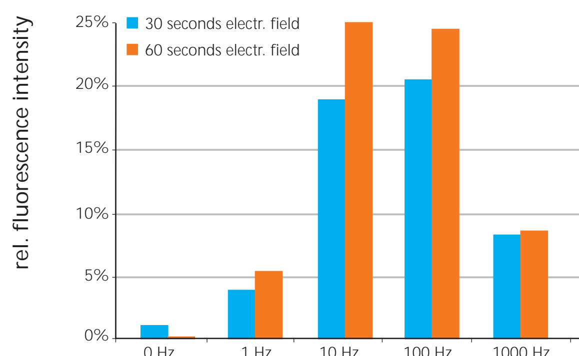


Figure 2:
Fluorescence detection of manipulation of DNA by applying alternating electrical fields. Two preset potentials are applied alternating between the interdigital electrodes and the frequency of switching the potentials is being varied. The alternating field enables the effective attraction of fluorescence labeled DNA toward the electrodes.

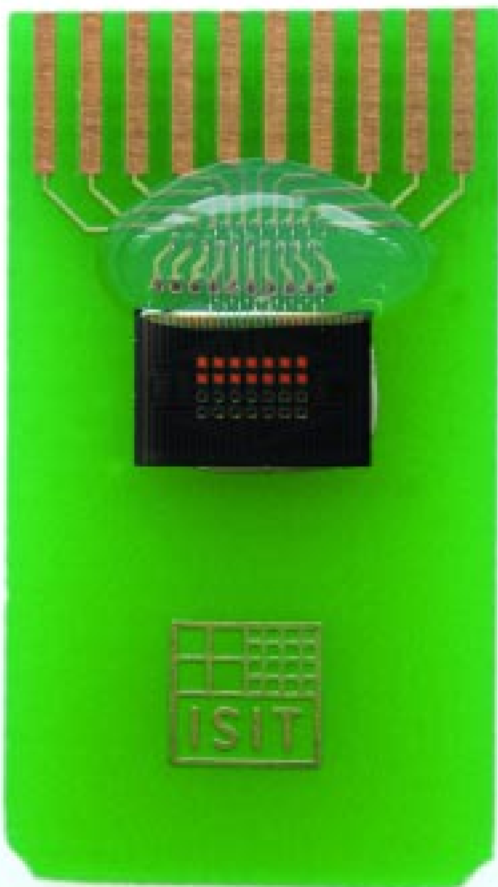
Representative Results of Work: Biotechnical Microsystems

Portable Monitoring Systems for Protein Detection

ISIT continous to develop the electrical biochip technology platform for different applications in biotechnology, medicine and the food industry. The available eBiochip devices are suitable to specific DNA- and RNA-identification as well as to the protein identification. Proteins have to be detected directly with high sensitive immunological methods because even smallest amounts of bioweapon toxins are lethal for humans.

Due to the principle and functionality of the eBiochip it is possible not only to realize devices for specific identification of molecular species but also to develop devices for monitoring air and water for contamination (alarm function). Here a combination with magnetic bead technology is used.

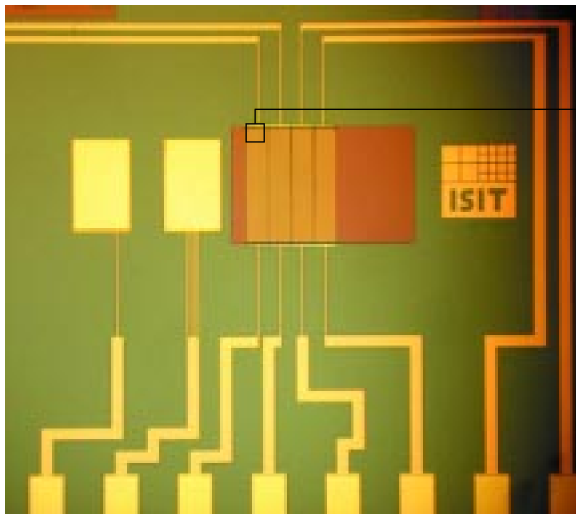
Figure 1:
Mounted electrical biochip.



The heart of the device is the electrical biochip. It is produced in silicon semiconductor technology at ISIT and exhibits embedded interdigitated micro electrode arrays made in gold, which are shaped like fingers of two hands entangled into each other (figure 2).

For the specific detection of proteins a common method called ELISA (Enzyme Linked Immunosorbent Assay is applied. Performing this measurement, biological capture molecules called antibodies are fixed to microscopically small paramagnetic plastic beads.

Then those antibody-loaded beads are transported in aqueous dispersion to the eBiochip device and collected with the help of a controllable magnet on the chip surface. If target molecules are present in a sample, which is subsequently brought in contact with the beads, they will bind to the specific antibodies. The following electrochemical detection is based on the redox-



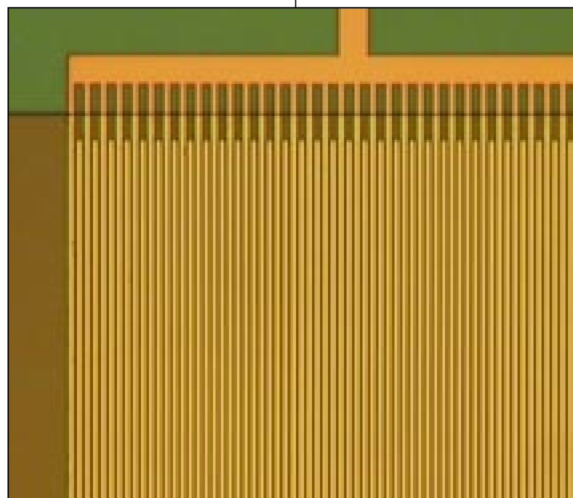
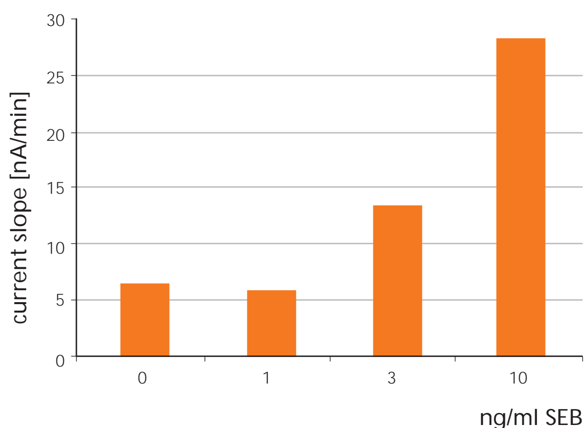


Figure 2:
Details of interdigitated embedded electrodes of 0,7 µm width.

recycling of hydroxyanilin, which is produced by a label enzyme, which is only bound if a target-capture complex was formed. After the removal of the magnet and the flushing of used beads the biochips can be used for new rounds of detection cycles with fresh antibody-loaded beads. This procedure enables a semi-continuous identification and monitoring (alarm function) of toxins using a chip for more than two weeks.
Due to the high sensitivity of the detection principle the eBiochip device was able to reach detection limits in the femtomolar range.
A concentration of 0,5 - 10 ng/ml of several bioweapon toxins e.g. staphylococcus enterotoxin type B (SEB), botolinum toxin type A has been detected as can be seen below.

Figure 3:
Sensitivity range of electrical monitoring of SEB.



Representative Results of Work: Module Integration

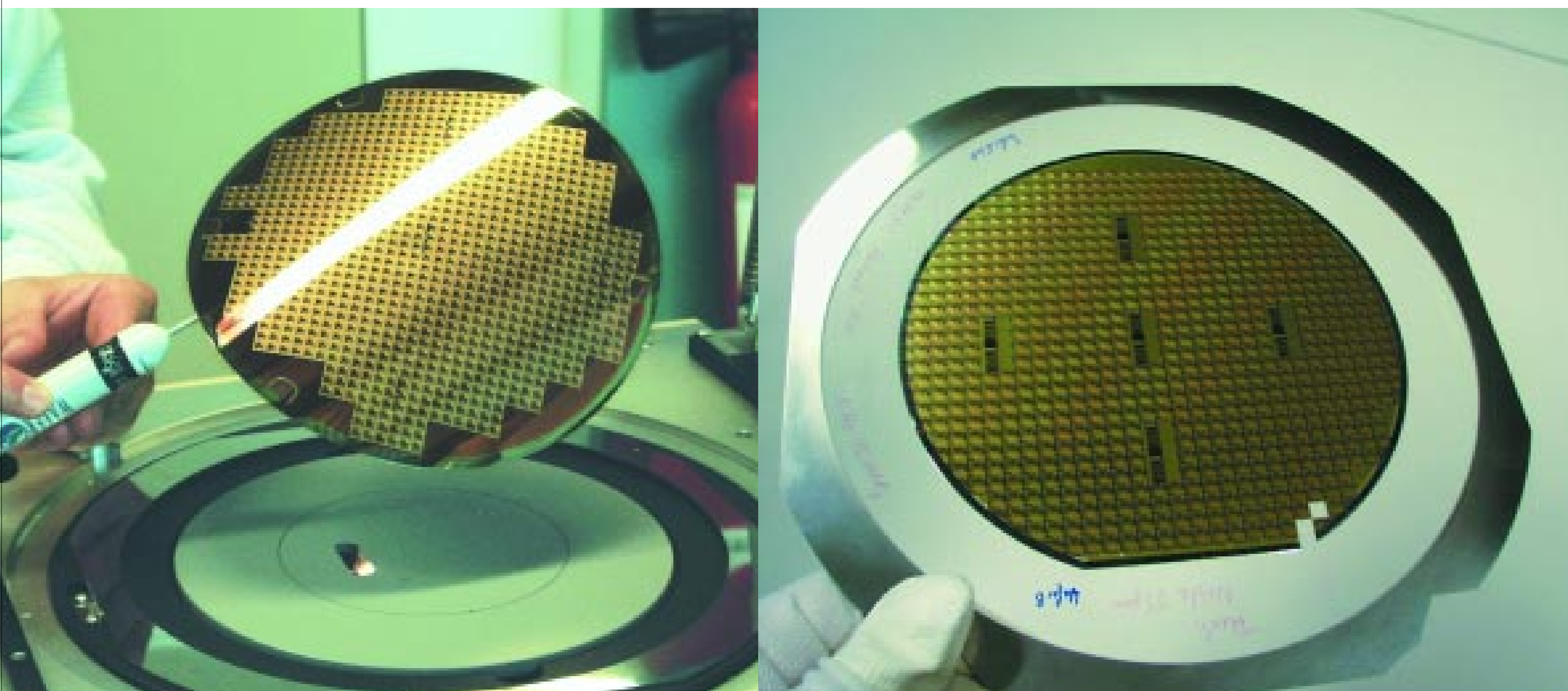
Low-Profile and Flexible Electronic Assemblies Using Ultra-Thin Silicon

Today there is a strong trend towards thin and flexible packages which is driven by different industrial applications e.g. smart cards and electronic labels. Furthermore, several technical approaches for ultra-thin chip stacking leading to 3D assemblies are followed, see table 1.
The motivation to use ultra-thin silicon is low-profile assemblies, flexible (bendable) assemblies and the enhancement of device performance e.g. in power electronics. In the European IST Project FLEX-SI ("Ultra-thin packaging solutions using thin silicon", IST-99-10205) the eight partners Philips Semiconductors (A), W.S.I. (F), Datacon (A), Nokia (FIN), Oticon (DK), PAV CARD (D), Helsinki University of Technology (FIN) and Fraunhofer ISIT (D) were working together on an industrial approach of low-profile packaging with ultra-thin flexible Si chips with a thickness < 50 µm. The basic approach of the FLEX-SI Project is to adapt and optimise existing industrial processes and equipment for the use of ultra-thin silicon instead of introducing totally different processes which are not compatible to the present infrastructure. With this approach, the FLEX-SI Project has provided a complete flow of industrial processes for ultra-thin silicon packaging from the initial end-user wafers to functional systems with low-profile modules.

Main results have been achieved in the following areas:

- wafer thinning to 50 µm rest thickness with complete de-stressing,
- electrical testing of ultra-thin wafers under static bending stress,
- handling and shipping of ultra-thin wafers,
- ultra-thin chip stacking for chip-on-chip applications,
- low-profile flip chip with pre-applied no-flow underfill,
- integrated module board (IMB) technique with ultra-thin chips,
- functional demonstrators working in their system environment.

Figure 1:
Handling of ultra-thin wafer: wafer bow (left), film-frame carrier (right).



Handling concept for of ultra-thin wafers

Based on the experience gained in the FLEX-SI Project is the use of flexible carrier based handling recommended. Here, standard film frame carriers with selected UV adhesive tapes with reduced residual adhesion can be used. Figure 1 shows the bow of a 50 µm ultra-thin wafer without support and an ultra-thin wafer mounted on tape. To minimize handling of bare ultra-thin wafers, the wafers should be mounted on the film frame carrier directly after ultra-thinning at the thinning site. This can be done by an automated handler to avoid any hands-on steps. We recommend that the dicing of the ultra-thin wafers is also perfomed at the thinning site as there are several advantages:

- know-how and experience in dicing of ultra-thin wafers but also in inspection of the dicing quality is available
- qualified UV exposure directly after the dicing
- robust shipping and handling (low stress on chip level)
- defined interface for automated equipment
- defined quality gate

Two important limitations of this concept should be mentioned:

- If a further processing of ultra-thin wafers is necessary, e.g. implantation and backside metallization in power electronics, a rigid carrier concept is beneficial.
- Following the FLEX-SI handling concept, especially when the ultra-thin wafers are diced at the thinning site, the user cannot perform electrical testing on wafer level after the thinning. Special testing equipment for diced wafers on film frame carrier is available, but does not provide the performance of standard wafer tester (e.g. speed, backside contact).

Applications	Technologies
• RF ID systems (smart cards, labels, tags) • Portable systems (telecom, video, ...) • Computer (memory modules) • Mechatronics, MEMS, sensors • Power electronics	• Flip chip on flex • Isoplanar interconnection • Chip embedding (chip-in-board) • Chip stacking and ´folded´ stacks • Vertical integration • Chip-on-bent surface • Power modules

Table 1:
Technology drivers for ultra-thin silicon.

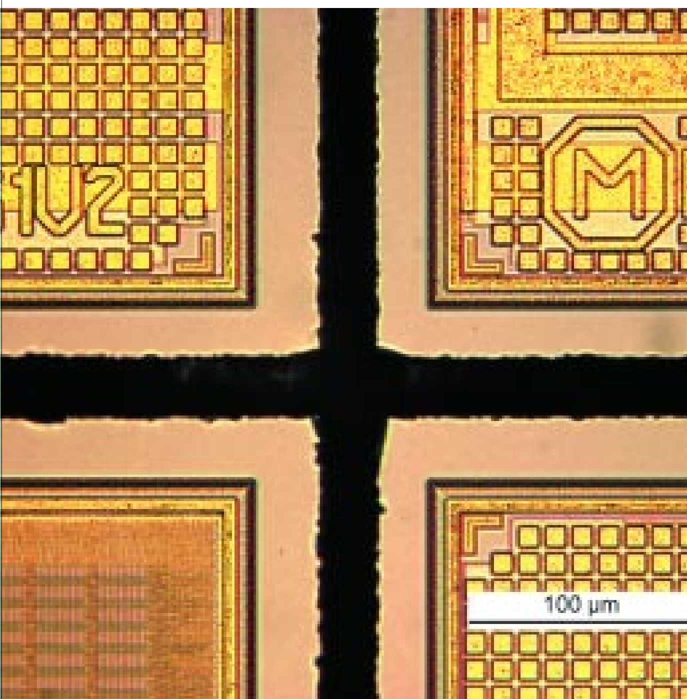


Figure 2:
8" wafer with 50 µm thickness (Philips Mifare®) after dicing in ISIT.

Representative Results of Work: Module Integration

Ultra-thin wafer dicing

The classical dicing process with a saw is able to process ultra-thin wafers down to a wafer thickness of 30 µm as has been demonstrated with very good yield (figure 2). The yield concerning process step is the mounting of the wafer on dicing tape, where uniaxial tension in the tape during mounting has to be avoided.

Ultra-thin chip stacking

Apart from low-profile flexible flip chip assemblies, ultra-thin chip stacking in chip-on-chip technology for system-in-package is another industrial application of the FLEX-SI project. For the chip-on-chip assembly with ultra-thin dice the die bonding is the crucial step and here especially the die ejection process, see figure 3 and 4.

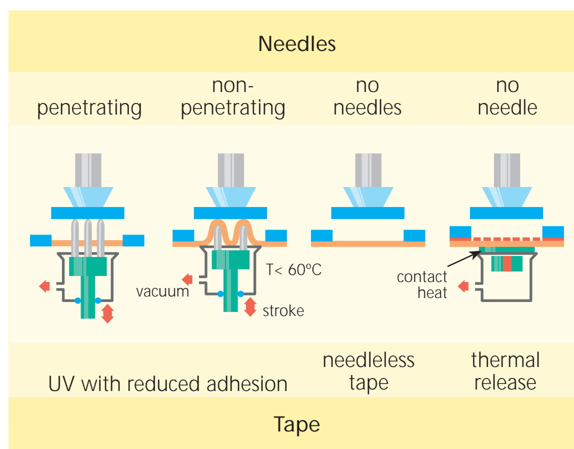


Figure 3:
Alternative methods for die ejection from tape.

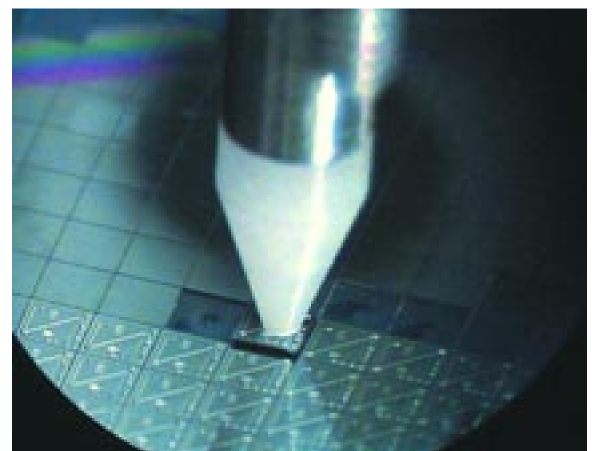


Figure 4:
Die eject process and ultra-thin die ejection.

The use of optimized UV-tape for low release adhesion is strongly recommended. The dicing defects introduced into the chip edges can be tolerated in an optimized die eject and assembly process, which limits the chip bending. For full flexible electronic assemblies, where an assembled large device will also become exposed to tensile and compressive stresses, a defect free chip edge is a must. Rounded chip edges and corners are beneficial. These demands can become covered with combined processes only:

- dicing and wet etching: chip surface protected by resin, special wet etch spin station
- dicing before grinding and plasma backside etching: high temperature tape required

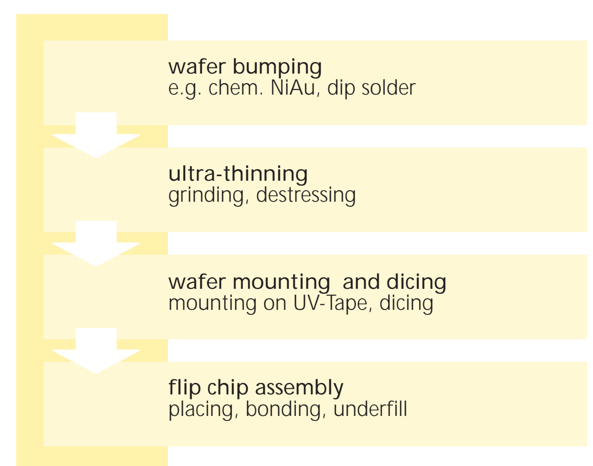


Figure 5:
Process flow of flip chip technology using ultra-thin ICs.

Figure 8:
Flip chip die bonder for ultra-thin silicon (Datacon 2200 apm).

Flip chip with ultra-thin ICs

The small-gap flip chip assembly of ultra-thin dice with low-profile bumps on thin and flexible substrates is enabling thin and flexible multi chip modules. To achieve a reliable flexible module the chips should be placed in the neutral layer of the bending.

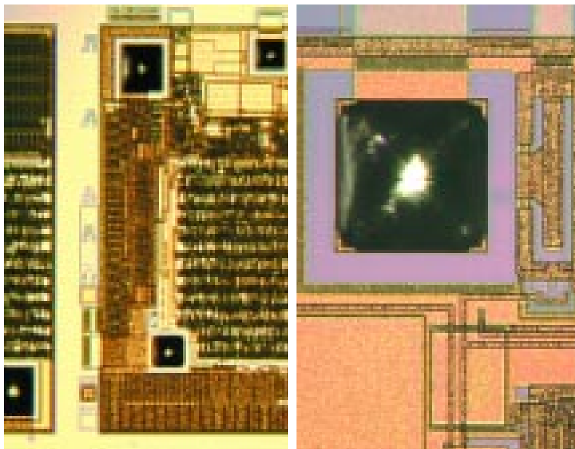


Figure 6:
Low profile solder bumping using solder dip transfer.

For the flip chip assembly with ultra-thin chips the FLEX-SI project followed the approach of wafer bumping before thinning (figure 5). The main reason for this decision is that there is no industrial process for the bumping of ultra-thin wafers.
As a consequence, the wafer thinning process has to be performed with bumped wafers.

The following challenges in the flip chip assembly of ultra-thin chips especially for solder flip chip have been met:

- no flux dip possible due to flat bumps
- capillary flow underfill after reflow difficult
- tool contamination due to underfill squeeze out likely
- die can float after placement or during reflow
- commercial available solder masks too thick for pad definition
- warped dice dependent on IC technology

Low-profile flip chip assemblies have been realized with ultra-thin Si chips using a solder flip chip technology. As low-profile bumps electroless NiAu/solder bumps were used where the flat solder cap is applied by a dip solder transfer process (figure 6). Attention has to be paid to the substrates as standard solder mask designs do not work. Pre-applied no-flow fluxing underfill is preferable compared to standard capillary flow underfill because of the small underfilling gap.

Flip chip die bonder for ultra-thin silicon

In the next step, the flip chip die bonder for ultra-thin silicon has been evaluated in an equipment assessment project (FLIBUSI, IST-2001-32315) under close to production conditions.
The overall objective of the FLIBUSI project is to evaluate, improve and assess the Datacon flip chip die bonder for use with ultra-thin chips (~50 µm), including the evaluation of the die ejection process with different tapes and the flip chip placing process (figure 7 and 8).
Its effectiveness for high speed flip chip bonding of ultra-thin chips for smart label production applications has been assessed. In a second

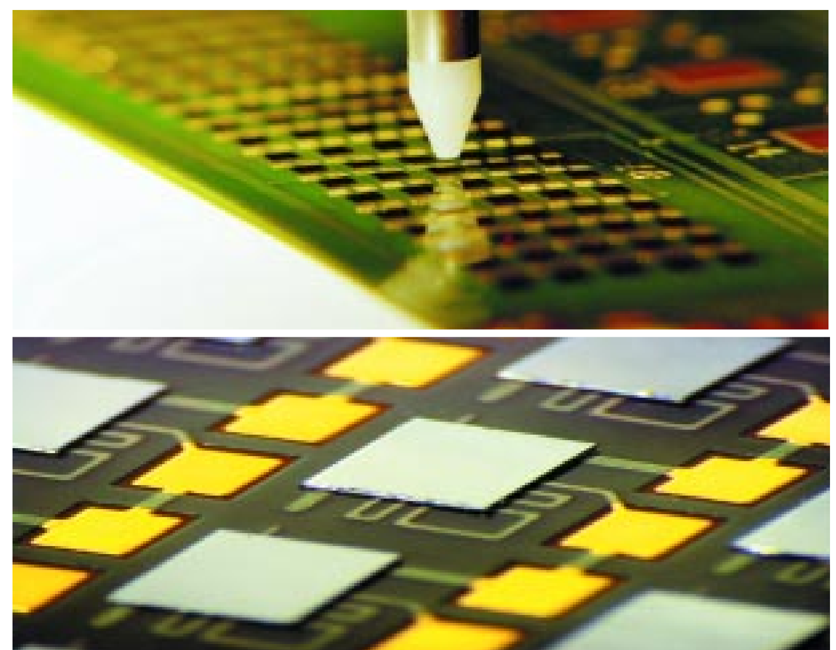


Figure 7:
Automatic flip chip on flex assembly with ultra-thin test chips (50 µm).

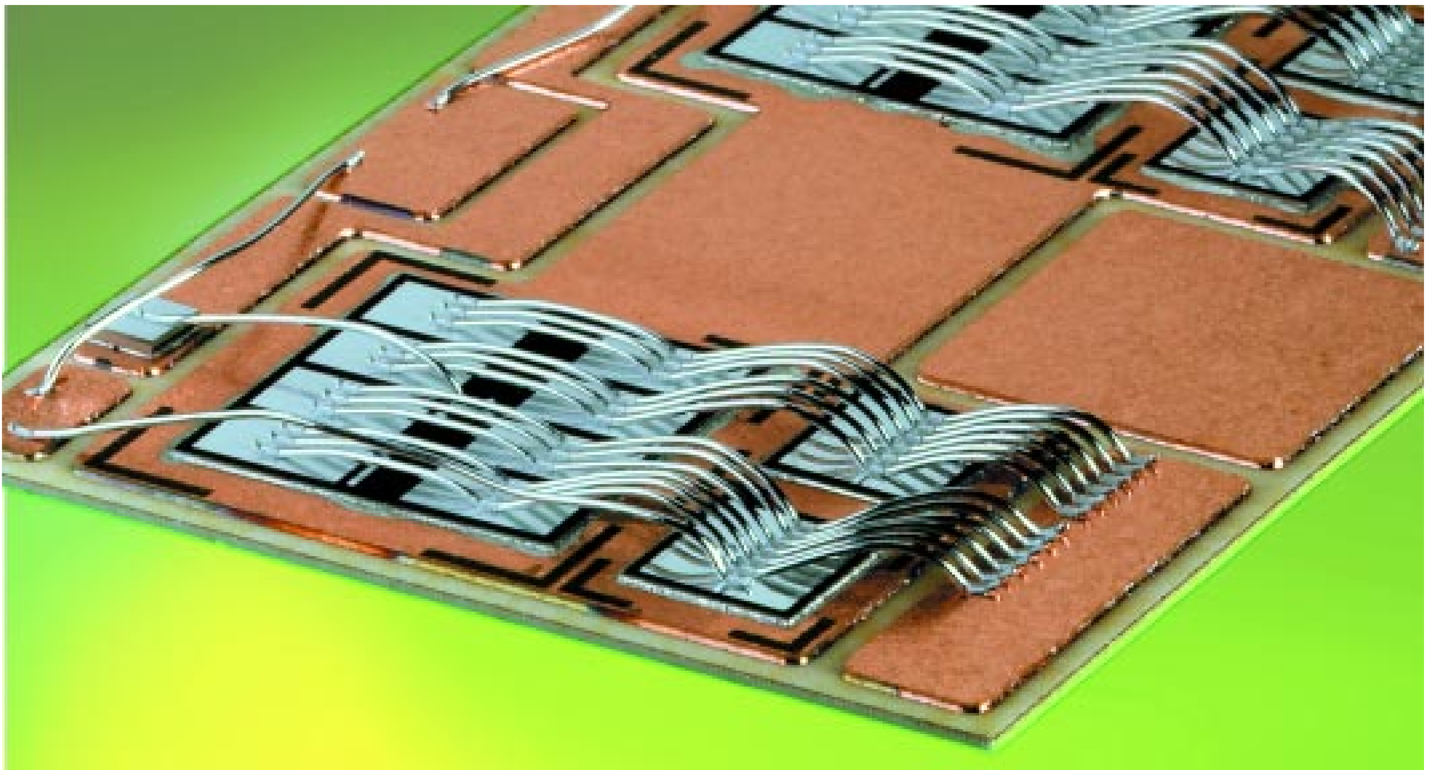


Figure 9:
DBC substrate with ultra-thin chips.

application, a solder die bond with ultra-thin chips for power modules is investigated. Figure 9 shows the direct bonded copper (DBC) substrate assembled with ultra-thin power semiconductors after large wire bonding. The performance of the equipment has been evaluated under close to production conditions and assessed in terms of process quality, yield, MTBF, MTTR, uptime, throughput and Cost of Ownership. As main result of the FLIBUSI project, it can be stated that ultra-thin die assembly technology is ready for production offering high speed processes (6000 uph for flip chip), high placement accuracy (< 10 µm/3 **σ**) and high yield (> 99 %), figure 10. The availability of automate equipment which is able to work with ultra-thin wafers resp. chips is a key requirement for the wide industrial use of thinned silicon in different applications including identification systems, power electronics, mobile telecommunication, computers, consumer electronics and medical technology. The main goal of the assessment project therefore is to enable enhanced use and performance of ultra-thin silicon by providing automated industrial equipment for chip and flip chip placement on substrates.

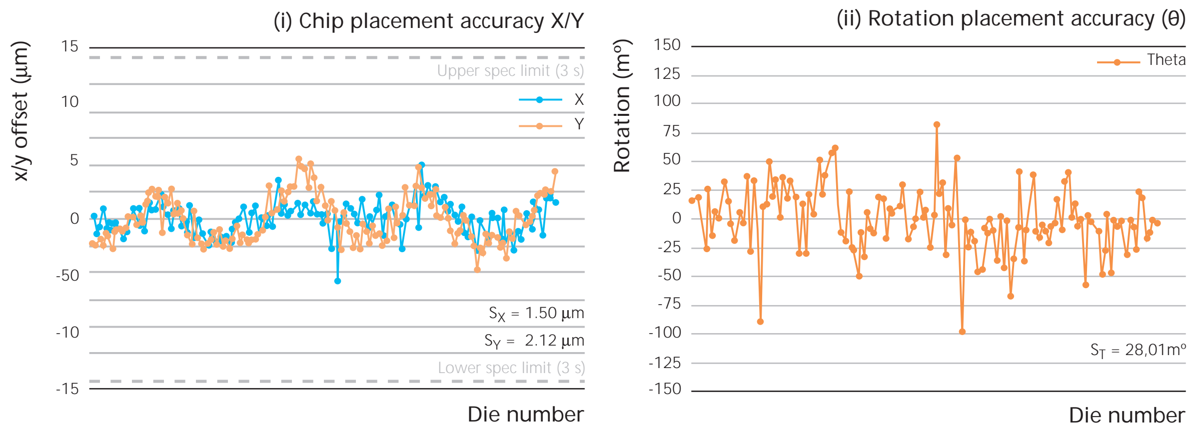


Figure 10:
Placement accuracy of flip chip die bonder with ultra-thin chips.

Representative Results of Work: Module Integration

Business Opportunities for Advanced Packaging in Europe

Together with three Partners (IZET Innovations-zentrum Itzehoe, Germany, MTA Marketing & Technologies Avancees, France and PP Provence Promotion, France) ISIT developes a business study about European packaging activities. This study is part of the project "Federating a Packaging and Interconnection Transeuropean Industrial Activity, PATRIA" supported by the European Commission (IST-2001-38482).

Vision

The global aim of PATRIA is to help pave the way for the resurgence of industrial scale advanced packaging and interconnection services in Europe targeting very advanced technologies, in closeness to European semiconductor manufacturers, smart card industry and MEMS facilities.

Aims

The aim of this study is to develop and to validate a plan for business opportunities in industrial scale advanced packaging and interconnection services in Europe, targeting very advanced technologies, in closeness to the European semiconductor manufacturers, smart card industry and MEMS facilities and situated within a consumer market of soon 500 million people with the expected EU expansion toward Eastern Europe.

PATRIA validates this work, representing a dynamic springboard to regain packaging business and industrial activity, today lost to Asian vendors, through the consolidation of a plan for business opportunities, building on emerging operations, attracting and federating industrial users, entrepreneurs and investors. PATRIA implements a model of federation of the existing operations and incubation of sub-critical initiatives, stemming from the existing research, commercial, industrial, political and governmental resources, in order to allow to reach the critical mass of what is considered as a capital intensive and competitive business.

Business Initiative Group "BIG"

A Business Initiative Group (BIG) has been set up consisting of a "who is who" in the field, which is to convene on a number of occasions to allow high level decision makers to interact, discuss, and network toward realising new initiatives for Europe in advanced packaging and interconnection. Any organisation with hands on business in packaging, interconnection and assembly can join. The BIG group will be operated in two phases:

1. devising a realistic strategy based on the European position and capabilities in terms of technology, market needs, available resources and funding;
2. implementing this strategy.

The BIG group brings together a core of persons holding strategy and management positions within the European research, manufacture and financial and communities. Involved in the packaging, interconnection and assembly processes, primarily as users, or as innovative suppliers too, they contribute in two ways:

- feed the study by their experience, vision of the markets and technologies
- hopefully become active players by implementing part of the plan for business released within PATRIA, along with other BIG members or by contracting alliances and partnerships with other organisations.

That's the PATRIA ultimate objective: synergize the wills of BIG members into new business.

PATRIA´s choice of Advanced Packaging & Interconnection technologies for semiconductors, smart cards and MEMS

Single chip IC packaging	miniaturised SMT packages (Chip-Scale-Package, CSP) incl. • wafer bumping for flip chip assembly • flip chip in package, • wafer-level CSP with balling focus: wafer-level chip size package (WL-CSP)
Hybrid integrated multi chip packaging	multi chip module (MCM) / system in package (SIP): • MCM/SIP for ICs with discrete or integrated passives • MCM/SIP for MEMS with ICs, passives • multi chip smart card module

Representative Results of Work: Module Integration

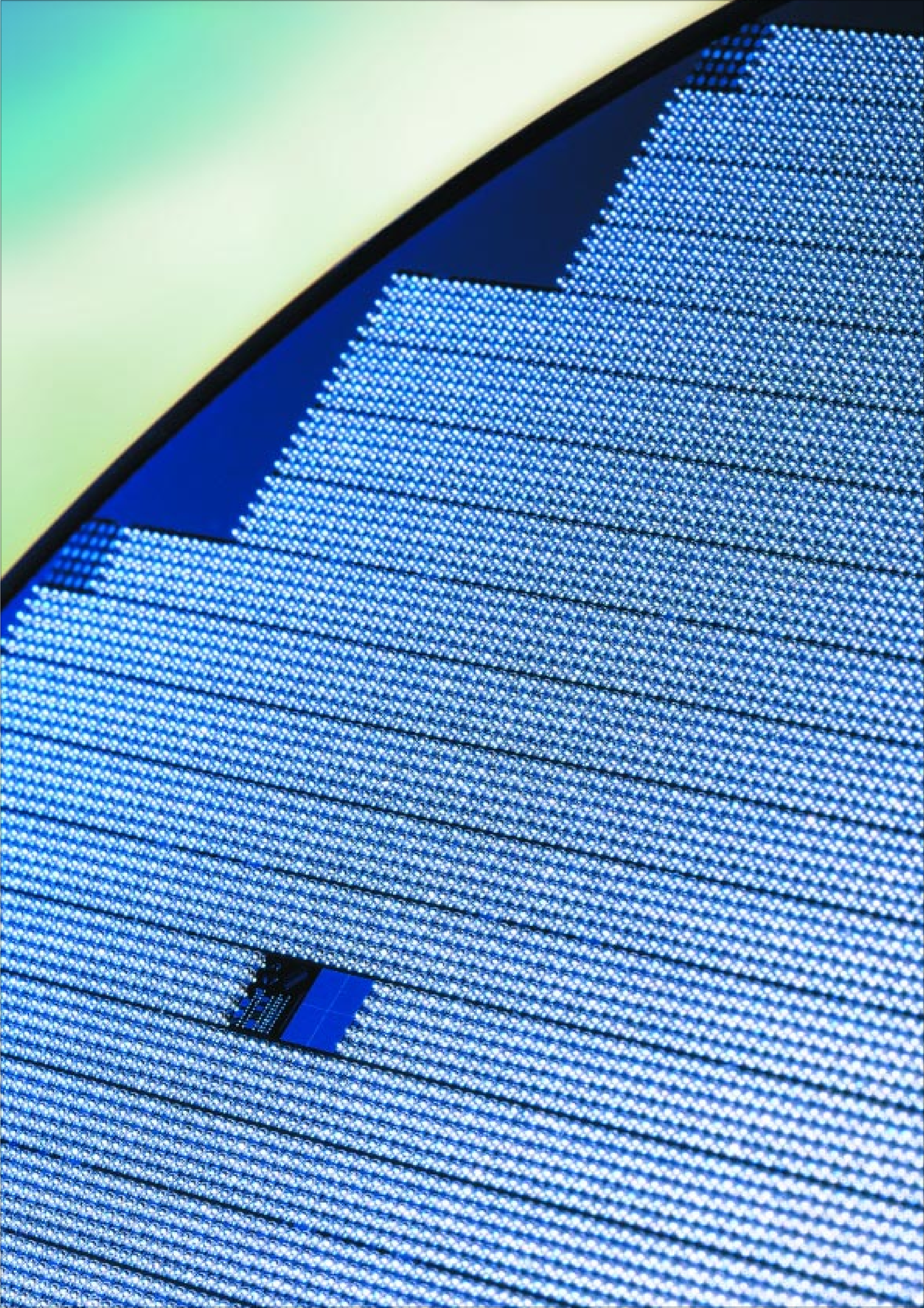
Project Results

The continuous technical progress and price decrease of silicon integrated circuits, smart cards and MEMS, in the direction of advanced system integration approaches, is accompanying the pervasion of consumer, computer and telecom products. Less known and visible is the considerable pressure that the IC technical progress - in term of physical volume, number of inputs and outputs, power dissipation, operating speed - puts on the techniques and industrial operations of packaging, interconnecting and assembling these ICs into cost-effective, small and affordable sub-assemblies. PATRIA addresses this specific need, delivering a practical action plan for solid and sustainable industrial supply of advanced packaging and interconnection solutions for the European industry in Europe federating the important stakeholders in this area.

The important issues are:

- Packaging and interconnection is becoming more and more a crucial part of components and system industries
  (e.g. key to Bluetooth modules efficiency, cost reduction & system business viability)
- System on a Chip issues can be (are) many times approached by system in a package solutions (e.g. Pentium, to quote only a famous one)
- Advanced packaging is difficult to outsource to distant and low engineering suppliers
- The viability of an European business model for advanced packaging solutions
  (BGA, CSP, ...) has been demonstrated by Atlantis or Pac Tech
- This is usually considered as a very capital intensive environment with rather low margins
- Interest in advanced packaging is combined with semiconductor industry cycles (of business and also of enthusiasm) and high industrial mobility (Moore's law, new fabs, global scenarios, ...)

Customer specific chip-size-packages with solder balls and BCB passivation before dicing.



Hearing-Aids with Rechargeable Power Supply (HARPOS)

The number of people depending on hearing-aids is steadily growing due to the increasing number of (a) elderly people in our society and (b) younger people suffering from hardness of hearing due to strong noise exposure by modern entertainment tools and events. Conventional hearing-aids are powered typically by primary cells that have to be exchanged at least once a week. Improvement in the ease of use of hearing-aids is achieved by using rechargeable batteries. Another important aspect is that hearing-aids are stigmatized to a certain degree. Therefore the number of totally implantable hearing-aids is growing. Fraunhofer-ISIT has started in the beginning of 2002 a EU-funded project with the Danish manufacturer of external hearing-aids Oticon and an Austrian manufacturer of cochlear implants Med-El. The University of Linkoeping is also involved in the project.

The challenge in this project is to adapt the lithium polymer technology developed by ISIT to the needs in hearing-aids applications. Basis of this technology is that all components of the battery are made from foils allowing for individually shaped batteries (figure 1). ISIT is supported in this project by the Bullith Batteries AG, a start-up company located at Munich and licencee of the ISIT battery technology. The development activity in this project has to adress to safety, reliability, energy density, lifetime and an appropriate housing technology for the very small battery cells required in hearing-aids. The batteries are realized in the so-called " bi-cell" geometry shown in figure 2.

The basic battery data elaborated from this set-up are as follows:

POLYMER BATTERY SYSTEM	
Anode	$Li_4Ti_5O_{12}$/Polymer
Cathode	$LiCoO_2$/Polymer
Separator	$Li_{1.3}Al_{0.3}Ti_{1.7}(PO_4)_3$/Polymer
Voltage	2,3 V

RESULTS	
Fading ($2mAh/cm^2$)	< 10 % / 2000 cycles at C-rate (37 °C)
DC-impedance (at 100 mHz)	< 5 Ω
Irr. capacity loss (37 °C)	< 7 % / year
Deep discharge (short)	tolerance 45 h at minimum
Self discharge	< 4 % / month

The system with lithiumtitanate as anode material has been selected for both applications for the external as well as for the implantable system due to its robustness even though it has a smaller specific capacity than the standard lithium rechargeable battery with graphite as anode material. An outstanding result is the cycle stability of the titanate system shown in figure 2. But also the low self discharge rate (reversible and irresversible) and the stability with respect to deep discharge are remarkable.

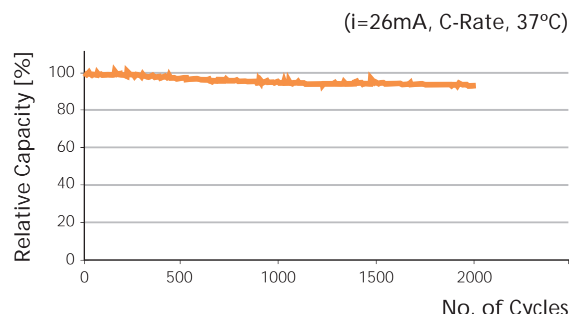


Figure 3:
Cycling of lithium polymer cells with lithiumtitanate as anode material. Charging and discharging were carried out at C-rate at 37°C. After more than 2000 cycles the capacity loss is below 10 %.

Cross section

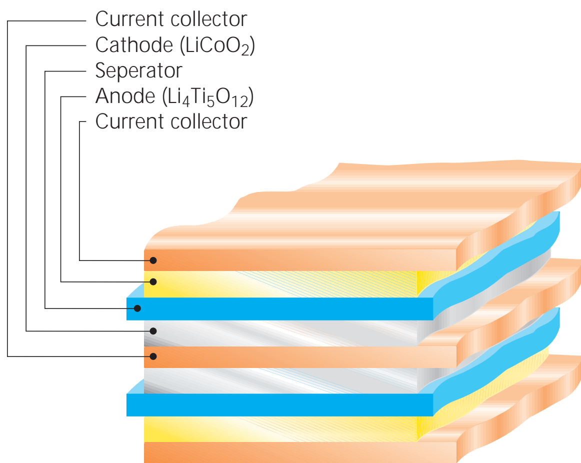


Figure 2:
Set-up of
lithium polymer cells.

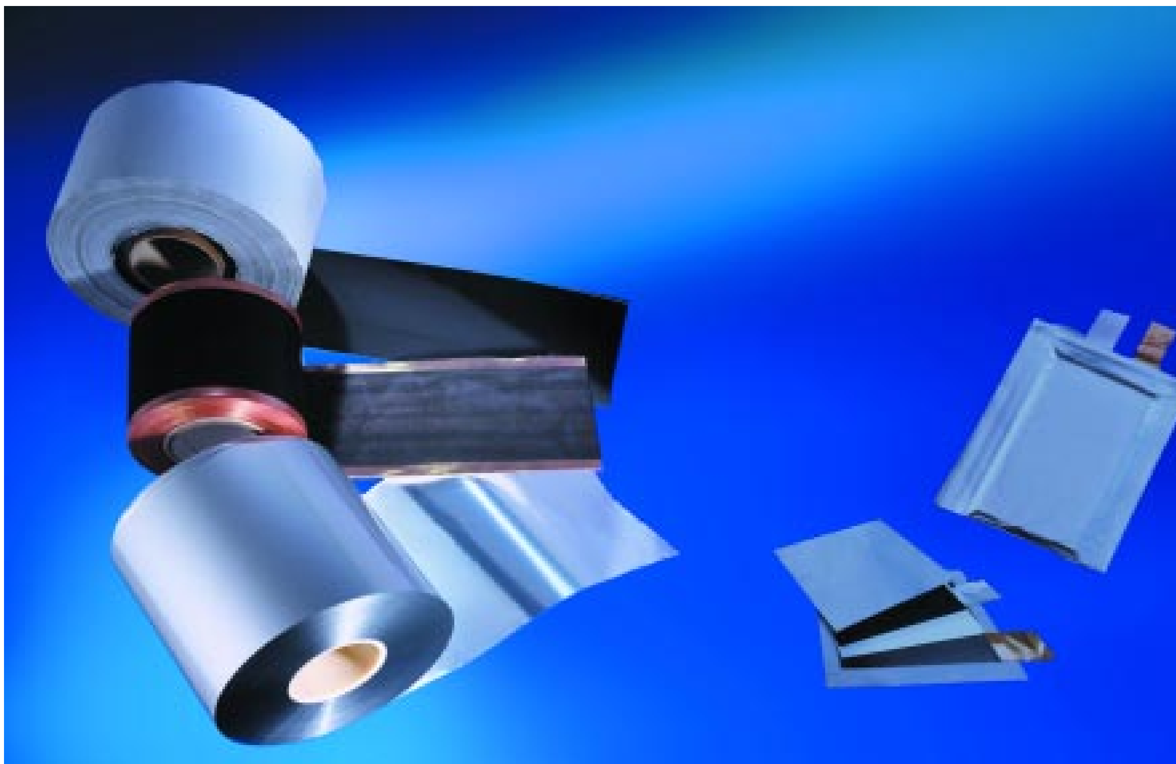


Figure 1:
Foils for electrodes, current collectors and the housing are the basic materials for the production of Lithium polymer rechargeable batteries.

Important Names, Data, Events
Annual Report 2002

Important Names, Data, Events

Lecturing Assignments at Universities

H. Bernt:
Halbleitertechnologie I und II, Technische Fakultät der Christian-Albrechts-Universität, Kiel

A. Heuberger:
Lehrstuhl für Halbleitertechnologie, Christian-Albrechts-Universität, Kiel

Memberships in Coordination Boards and Committees

T. Ahrens:
Coordinator of AOI-Anwenderkreis (Automated Optical Inspection)

T. Ahrens:
Member of DVS Fachausschuss Löten

T. Ahrens:
Member of DVS Fachausschuss Mikroverbindungstechnik

T. Ahrens:
Member of Hamburger Lötzirkel

W. H. Brünger:
Member of Steering Committee: Electron, Ion and Photon Beams and Nanofabrication, EIPBN, USA

W. H. Brünger:
Member of VDI Fachausschuss: Maskentechnik, VDI, Düsseldorf

W. H. Brünger:
Section Head: Micro and Nano Engineering, MNE 02, Grenoble

J. Eichholz:
Member of MEMSTAND Workshop International Steering Committee

T. Harder:
Member of European Network ¨Adhesives in Electronics¨

A. Heuberger:
Advisory Editor of International Journal of Semiconductor Manufacturing Technology; Microelectronic Engineering

A. Heuberger:
Member of NEXUS Board

A. Heuberger:
Member of NEXUS Excecutive Board

A. Heuberger:
Member of NEXUS Academic Working Group

A. Heuberger:
2. Chairman of an International Conference on Micro Electro, Opto, Mechanic Systems and Components

R. Hintsche:
National Delegate of COST Nanoscience & Technology Advisory Group (NanoSTAG)

K. Pape:
Member of VDI Fachausschuß Assembly Test, VDI, Frankfurt

K. Pape:
Member of BVS, Bonn

K. Pape:
Member of FED

H. C. Petzold:
Member of NEXUS Executive Board

H. C. Petzold:
Co-editor of mst news

M. Reiter:
Member of Gf Korr " Arbeitskreis Korrosionsschutz in der Elektronik"

M. Reiter:
Member of " Arbeitskreis Lotpasten"

M. Reiter:
Member of " Arbeitskreis Bleifreie Verbindungstechnik in der Elektronik„

M. Reiter:
Member of " Industrie-Arbeitskreis Know-How-Transfer mikrotechnischer Produktion"

G. Zwicker:
Head of Fachgruppe Planarisierung/ Fachausschuss Verfahren / Fachbereich Halbleitertechnologie und -fertigung der GMM des VDE/VDI

Cooperation with Institutes and Universities

Institut für fluidtechnische Antriebe und Steuerungen, RWTH, Aachen

Institut für Werkstoffe der Elektrotechnik, RWTH, Aachen

Aalborg University, Aalborg, Denmark

Hahn-Meitner-Institut, Berlin

Technische Universität Berlin

Technische Universität Braunschweig Fachbereich Elektrotechnik, Institut für Elektrophysik

Technical University of Budapest, Department of Electronic Technology, Budapest, Ungarn

Cambridge University, UK

Rutherford Appleton Laboratories, Didicot, UK

Technische Universität Dresden, Institut für Halbleiter- und Mikrosystemtechnik

University of Gdansk, Polen

Karl-Franzens University, Graz, Österreich

Ernst-Moritz-Arndt-Universität (EMAU), Greifswald

CEA Leti, Grenoble, France

Max-Planck-Institut für Mikrostrukturphysik, Halle

Universitätskrankenhaus Eppendorf, Hamburg

Universität Hamburg, Abteilung für Biochemie und Molekularbiologie

Fachhochschule Westküste, Heide

University of Technology, Helsinki

Institut für Fügetechnik und Werkstoffprüfung (IFW), Jena

Universität Karlsruhe

Christian-Albrechts-Universität, Technische Fakultät, Kiel

Fachhochschule Kiel

IEMN-ISEN, Lille, France

University of Linkoeping, Sweden

City University, London, UK

University of Southern California, Los Angeles, USA

Université catholique de Louvain, Louvain-la-Neuve, Belgium

Fachhochschule Lübeck

CNRS-Université Claude Benard, Lyon, France

Universität, Madrid, Spanien

Technische Universität München

Universität der Bundeswehr, München

SINTEF, Oslo, Norway

Universität Oulu, Finland

Rutherford Appleton Laboratory Oxford, United Kingdom

Universtity of Pavia, Italy

University of Perugia, Italy

Royal Institute of Technology (KTH), Stockholm, Sweden

VDI/VDE-Technologenzentrum Informationstechnik, Teltow

Fachhochschule Wedel

Technische Universität Wien, Austria

Trade Fairs and Exhibitions

Hannover Messe 2002.
MP-CC Micro Plastic – Competence Center,
April 15 – April 20, 2002,
Hannover

Analytica 2002.
Instrumental Analysis, Laboraty Technology and Bio Technologies. 18th International Trade Fair and Analytica Conference,
April 23 – April 26, 2002,
München

PCIM 2002.
International Exhibition and Conference for Power Conversation and Intelligent Motion,
May 14 – May 15, 2002,
Nürnberg

SMT/ES&S/Hybrid 2002.
System Integration in Micro Electronics, Exhibition and Conference,
June 18 – June 20, 2002
Nürnberg

Optatec 2002.
International Trade Fair for Optics and Optoelectronics – Application and Technology,
June 18 – June 21, 2002,
Frankfurt

Electronica 2002.
20th international Trade Fair for Components and Assemblies in Electronics,
November 12 – November 15, 2002,
München

Miscellaneous Events

Der Lötprozess in der Fertigung elektronischer Baugruppen
Seminar. March 18 – March 2, 2002,
ISIT Itzehoe

8. CMP Users Meeting
Forum der Technik, April 19, 2002,
Munich

SMT-Rework-Praktikum
Seminar. April 24 – April 26, 2002,
ISIT Itzehoe

Manuelles Löten von SMT-Bauelementen
Seminar. April 24 – April 26, 2002,
ISIT Itzehoe

Official event on the occasion of the opening of the new factory building for Solid Energy GmbH and Condias GmbH right next to the Fraunhofer ISIT
June 24, 2002, Itzehoe

ISIT-, Vishay-Presentation at Tag der beruflichen Bildung
organized by Berufliche Schule des Kreises Steinburg. July 2, 2002,
Itzehoe

ISIT-, Vishay-Presentation at Tag der Ausbildung
organized by ÜAZ Itzehoe.
September 15, 2002, Itzehoe

Mobiles-Rework-Praktikum
Seminar. September 25 –
September 26, 2002, ISIT Itzehoe

Workshop on Ultra-thin Si Packaging
Seminar. September 25 –
September 26, 2002, ISIT Itzehoe

Der Lötprozess in der Fertigung elektronischer Baugruppen
Seminar. October 7 – October 9,
2002, ISIT Itzehoe, 2002,

9. CMP Nutzertreffen
3M – Eurpoean Technical Center,
October 25, 2002, Neuss

Offical event at MuK Lübeck on the occasion of awarding the Solid Energy GmbH with the Schmidt-Römhild Technology Award
November 7, 2002, MuK Lübeck

SMT-Rework-Praktikum
Seminar. November 20 – November 22, 2002, ISIT Itzehoe

Manuelles Löten von SMT-Bauelementen
Seminar. November 20 – November 22, 2002, ISIT Itzehoe

Scientific Publications

Journal Papers and Contributions to Conference

R. Brandes, F. Klaessig, T. Knothe, W. Lortz, F. Menzel, T. Shibasaki, A. Philipossian, G. Zwicker:
New Particles for the CMP Application by Changing the Powder Morphology of Fumed Silica. Planarization & CMP Technical Meeting 2002, Japan Society of Precision Engineering, San Francisco, July 24, 2002

W. H. Brünger, C. Dzionk, R. Berger, H. Grimm, A. Dietzel, F. Letzkus, R. Springer:
Evaluation of Ion Projection using Heavy Ions suitable for Resistless Patterning of Thin Magnetic Films. Microelectron. Eng., 61-62, p. 295-300, 2002

W. H. Brünger, J. Eichholz, H. Hanssen, D. Friedrich:
Fabrication and Electrical Characteristics of Carbon Nanotube-based Microcathodes for Use in a Parallel Electron-Beam Lithography System. American Vacuum Society, B 21(2), March – April 2003

A. Dietzel, R. Berger, H. Grimm, C. Schug, W. H. Brünger, C. Dzionk, F. Letzkus, R. Springer, H. Löschner, E. Platzgummer, G. Stengl, S. Anders, Z. Z. Bandic, C. T. Rettner, B. D. Terris, H. Eichhorn, M. Böhm, D. Adam:
Resistless Patterning of Magnetic Storage Media using Ion Projection Structuring. Mat. Res. Soc. Proc., 705, p. 279-289, 2002

A. Dietzel, R. Berger, H. Grimm, W. H. Brünger, C. Dzionk, F. Letzkus, R. Springer, H. Löschner, E. Platzgummer, G. Stengl, Z. Z. Bandic, B. D. Terris:
Ion projection direct Structuring for Patterning of Magnetic media. IEEE Trans. Magn., 38, p. 1952-1954, 2002

R. Dudde, G. Piechotta, R. Hintsche:
Microsystems based Glucose Sensor for continuous Monitoring of Blood Glucose Levels. MST News, April, 2002

T. Harder:
Low-Profile and Flexible Electronic Assemblies Using Ultra-Thin Silicon – the European FLEX-SI Project. International Conference on Advanced Packaging and Systems ICAPS, Reno (NV), March 10 – March 13, 2002

T. Harder, W. Reinert:
Low-Profile and Flexible Electronic Assemblies Using Ultra-Thin Silicon – the European FLEX-SI Project. IMAPS/Kluwer book, Foldable Flex and Thinned Silicon Multichip Packaging. (Ed J. Balde), 2002

H. Löschner, G. Stengl, H. Buschbeck, A. Chalupka, G. Lammer, E. Platzgummer, H. Vonach, P. W. H. de Jager, R. Käsmaier, A. Ehrmann, S. Hirscher, A. Wolter, A. Dietzel, R. Berger, H. Grimm, B. D. Terris, W. H. Brünger, D. Adam, M. Böhm, H. Eichhorn, R. Springer, J. Butschke, F. Letzkus, P. Ruchhöft, J. C. Wolfe:
Large-Field Ion-Optics for Projection and Proximity Printing and for Mask-less Lithography (ML2). Proc. SPIE-Int. Soc. Opt. Eng., 4688, p. 595-606, 2002

K. Oelsen, R. Eisele, M. H. Poech, D. Thumfart, C. Auradnik:
Reliability of Power Modules for Mobile Applications. PCIM Europe, October, 2002

M. H. Poech:
Schädigungsmechanismen in Lötverbindungen bei erhöhter Temperatur. VTE, 14/1, p. 12, Düsseldorf, 2002

Talks and Poster Presentations

T. Ahrens, A. Karilainen, D. Prochota, M. H. Poech:
Phasenwachstum und Scherfestigkeit von Lötstellen. Seminar: Elektronische Baugruppen – Aufbau- und Verbindungstechnik, DVS/GMM Tagung, Fellbach, February 6 – February 7, 2002

T. Ahrens:
Lötqualität. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, March 18 and October 7, 2002

T. Ahrens:
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T. Ahrens:
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T. Ahrens:
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T. Ahrens, H. Schimanski:
Rework-Stationen für komplexe SMT-Baugruppen. Seminar: Mobiles-Rework-Praktikum, ISIT, Itzehoe, September 25, 2002

T. Ahrens, H. Schimanski:
Qualitätsbewertung der Lötverbindungen. Seminar: Mobiles-Rework-Praktikum, ISIT, Itzehoe, September 26, 2002

T. Ahrens:
Bleifrei Wellenlöten. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, October 9, 2002

Scientific Publications

Doctoral Theses

P. Merz:
Herstellung mikrostrukturierter Oberflächen in Glas und Polymer durch replikative Verfahrens-technologien.
Christian-Albrechts-Universität Kiel, Technische Fakultät, November, 2002

Diploma Theses

J. Pontow:
Prozessintegrierte Reparatur von miniaturisierten SMD-Bauteilen mit bleifreiem Lot.
Fachhochschule Wedel, August, 2002

D. Süsselbeck:
Entwurf, Simulation und Charak-terisierung elektromagnetisch angetriebener MEMS-Scanner.
Fachhochschule Münster, October, 2002

Patents

T. Ahrens, S. Puls:
Aufschmelzeinrichtung für Röntgeninspektionsanlage
DE 10225899.6

F. Bonfati, H. Futscher, G. Neumann:
Mit einem Stanzmuster versehende Folien und Folienverbünde, insbesondere für die Fertigung von elektrochemischen Bauelementen auf Folienbasis
DE 10238354.5

W. Brünger:
Verfahren zur Herstellung von Nanostrukturen auf nichtplanaren Oberflächen
DE 10223223.7

J. Eichholz:
Vorrichtung zur Steuerung eines Elektronenstromes
DE 10241433.5

J. Eichholz, J. Quenzer, P. Staudt:
Verfahren zur Herstellung einer digitalen Gatterschaltung mit her-abgesetztem Querstrom
DE 19819867

J. Eichholz:
Verfahren und Schaltungsvor-ichtung zur Ansteuerung einer Mehrzahl von Schaltungen
DE 10030752

T. Lisec, P. Merz:
Sensorchip für einen Differenz-drucksensor mir beidseitigem Überlastungsschutz
DE 10249238.7

T. Lisec:
Anordnung beweglicher Pipettenspitzen zum Pipettieren auf unebenen Oberflächen
DE 10135963.2

M. März, H. Ryssel, K.-H. Pettinger, A. Heuberger:
Energiespeicher mit einstellbarer konstanter Ausgangsspannung
DE 10138515.3

G. Neumann, H. Futscher:
Verfahren zur Herstellung von beschichteten Streckmetallen und Verwendung solcher Metalle als Stromableiter in elektrochemischen Bauelementen
DE 10257186.4

H. J. Quenzer, A. V. Schulz, B. Wagner, P. Merz:
Herstellung von segmentierten Silizium-Glas-Verbund-Substraten, insbesondere zur elektrischen HF-Durchkontaktierung auf Waferebene
DE 10118529.4-33

H. J. Quenzer, W. Reinert:
UV-Strahlformungsblende mit Gebrauchsspuren
DE 10134893.2

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Verbessertes Verfahren zur Herstellung von dicken Glas-schichten für das anodische Bonden
DE 10208782.2

B. Wagner:
Verfahren zur Strukturierung eines aus glasartigem Material bestehenden Flächensubstrats
DE 10118529C1

R. Wilm, W. Reinert:
Chipkarte
DE 19641406.7-53

G. Zwicker, M. Fryda, T. Matthée:
Neues Verfahren zum Ätzen von Fotoresist
DE 10219688.5

General View on Projects

Overview of Projects

- Erzeugung dreidimensionaler Mikrostrukturen, MIKROSTRUK
- Prozesse/ Verfahren für die Herstellung ultradünner Trench-IGBTs auf sub-100 µm Silizium-Substraten
- Entwicklung einer UBM/BCB Technologie für wafer level packaging
- Optimierung des Stressverhaltens galvanisch erzeugter Ni-Fe-Schichten
- Fabrication of Si-Microstructures based on SOI-wafers
- Prozessentwicklung und Unterstützung bei der Produktion von Philips-Wafern
- Weiterentwicklung und Herstellungskonzept für ultradünne PowerMOS Transistoren und IGBTs
- Halbleiterbauelemente hoher Leistung
- Entwicklung von Super-Junction-Strukturen für Hochvolt-Power MOS-Anwendungen
- Prozessierung von Wafern mittels Silizium-Trockenätzen zur Erzeugung spezieller Si-Strukturen
- Fabrication of Capacitor Structures
- Herstellung von Nonostrukturen in Siliziumnitrid
- Optische Reflexionsgitter auf Tantalpentoxid
- Einsatz der Ionen-Projektions-Lithographie im Fertigungsprozess für die kontaktlose Strukturierung planarer magnetischer Speichermedien
- Ausgasverhalten von e-beam-Lacken
- Arrays of Microguns for Parallel e-beam Nanolithography, NANOLITH
- Entwicklung von Post-CMP-Reinigungsprozessen für die Fertigung von zukünftigen integrierten Schaltkreisen in der Si-Technologie
- Evaluierung von Slurries zum chemisch-mechanischen Polieren von SiO_2
- Planarisierung von Glaswafern
- Prozessentwicklung für die Herstellung von terrasierten Silizium-Strukturen
- Maskenentwurf für „Integrated Discretes"
- Designkit für Tronic´s
- Untersuchung an mikromechanischen Drehraten-Sensoren
- Entwicklung eines mikromechanischen Luftmassensensors
- Entwicklung eines in Siliziumtechnologie hergestellten pneumatischen 3/2-Wege-Mikroventils
- European Access to Manufacturing Service for MEMS on SOI Micromachining Technologies
- Herstellung und Replikation von großflächigen 3D-Nano- und Mikrostrukturen, NanoFab
- Entwicklung von kapazitiven HF-Schaltern
- Entwicklung und Herstellung von Flowsensoren
- Musterfertigung von Blendenkarten mit Soft-Blenden
- Fertigung eines Spiegelarrays mit elektrischem Anschluss und Beurteilung der Mikrospiegeltechnologie
- Entwicklung eines 4x 4 Arrays von Zweiachsen-Mikrospiegeln
- Fabrication, Assembly and Testing of a Miniature Two-Axis Laser Scanner and a High Voltage Amplifier
- Micromachined Electromechanical Devices for Integrated Wireless Communication Transceivers, MELODICT
- Herstellung von Nanolichtquellen zur hochauflösenden Inspektion von biologischen Proben
- Kostengünstige Herstellung von Mikrosystemen: Verbundtechnik von Kunststoff und Silizium (MP-CC)
- Entwicklung eines hochdruckfesten Drucksensors
- Herstellung mikrooptischer Linsenarrays aus Glas
- Herstellung mikrooptischer Linserarrays in Polycarbonat
- Electric DNA Chips for Bioprocess Control
- Integriertes mikrobiologisches Sensorsystem zur Abwasseranalyse
- Silizium-Chipsystem für die biochemische Analysentechnik: Technologische Plattform und Systemintegration Teilvorhaben: Messverhalten und biochemische Assays
- Silizium-Chipsystem für die biochemische Analysentechnik: Technologische Plattform und Systemintegration, Teilvorhaben: Testchips und Testverhalten
- Entwicklung von Ultramikroelektrodenarrays und Integration in ein automatisiertes fluidisches Analysesystem
- Advanced Insulin Infusion Using a Control Loop ADICOL
- Nanoskalige elektrische Messverfahren für portable Analysesyteme niedermolekularer Verbindungen
- Aufbau einer technologischen Plattform zur Erregerdiagnostik mit Elektrischen Biochips (BMBF)
- Online Programmierung komplexer Biosysteme in rekonfigurierbarer bioelektronischer Hardware BMBF-Verbundprojekt BioPro
- Manufacturing Cluster, EUROPRACTICE AMICUS
- Customer Support and Design Centre for Physical Measurement Systems, EUROPRACTICE CCMeSys
- Microactuator Competence Centre, EUROPRACTICE IV CCMicro
- Laserlöten von Silizium-Pyrex mittels Glaslot zur Kapselung von Mikrosensoren
- Mikrosystemtechnik 2000+, µ-Encoder mit zentrischer optischer Abtastung
- Bonden mit Cu-Draht in der Leistungselektronik
- Flip-Chip-Technologie mit gedünnten Siliziumchips für intelligente Etiketten (Smart-Label)
- Chipkartenbestückung mit Grautonblenden
- Ultra-Thin Packaging Solutions using Thin Silicon
- Thematic Network " Adhesives in Electronics"
- Flip Chip Die Bonder for Ultra-Thin Silicon
- Alternatives Löten von Mikrobausteinen
- Untersuchung zur Unterfüllung von Bauteilen mit flächig verteilten Lötanschlüssen in der Oberflächenmontagetechnik, CSP Underfill
- Long-term stability of vacuum-encapsulated MEMS devices using eutectic wafer bonding, VABOND
- Federating a Packaging and Interconnection Transeuropean Industrial Activity, PATRIA
- Stressarme Montage von Sensoren und Mikrooptik – Komponenten mittels Mikroklebtechnik
- Entwicklung eines marktfähigen Micro-Drehgebers zur absoluten Winkelcodierung nach dem Prinzip der optischen Abtastung, Centro, BMBF
- Evaluation of packaging concepts for the gyro-sensor, Gyrosil, BMBF
- Fertigung von Testwafern zur Justierung von Bestückungsanlagen
- Bleifreies Wellenlöten, EUREKA
- Herstellung porenarmer Weichlötverbindungen
- Reflow und Wellenlöten mit bleifreien Loten
- Zuverlässigkeit mikrotechnischer Lötverbindungen
- Die elektronische Baugruppe der Zukunft
- Stressoptimierte Montage und Gehäusetechnik für mikromechanisch hergestellte Silizium-Drehratensensoren
- Festkörper-Lithiumakkumulatoren
- Entwicklung von hochzyklenfesten Li – Festkörper – Polymerakkumulatoren mit einstellbarer, konstanter Ausgangsspannung
- Hearing – aids with rechargeable power supply, HARPOS

Contact

Please contact us for further information.
We would be glad to answer your questions.

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