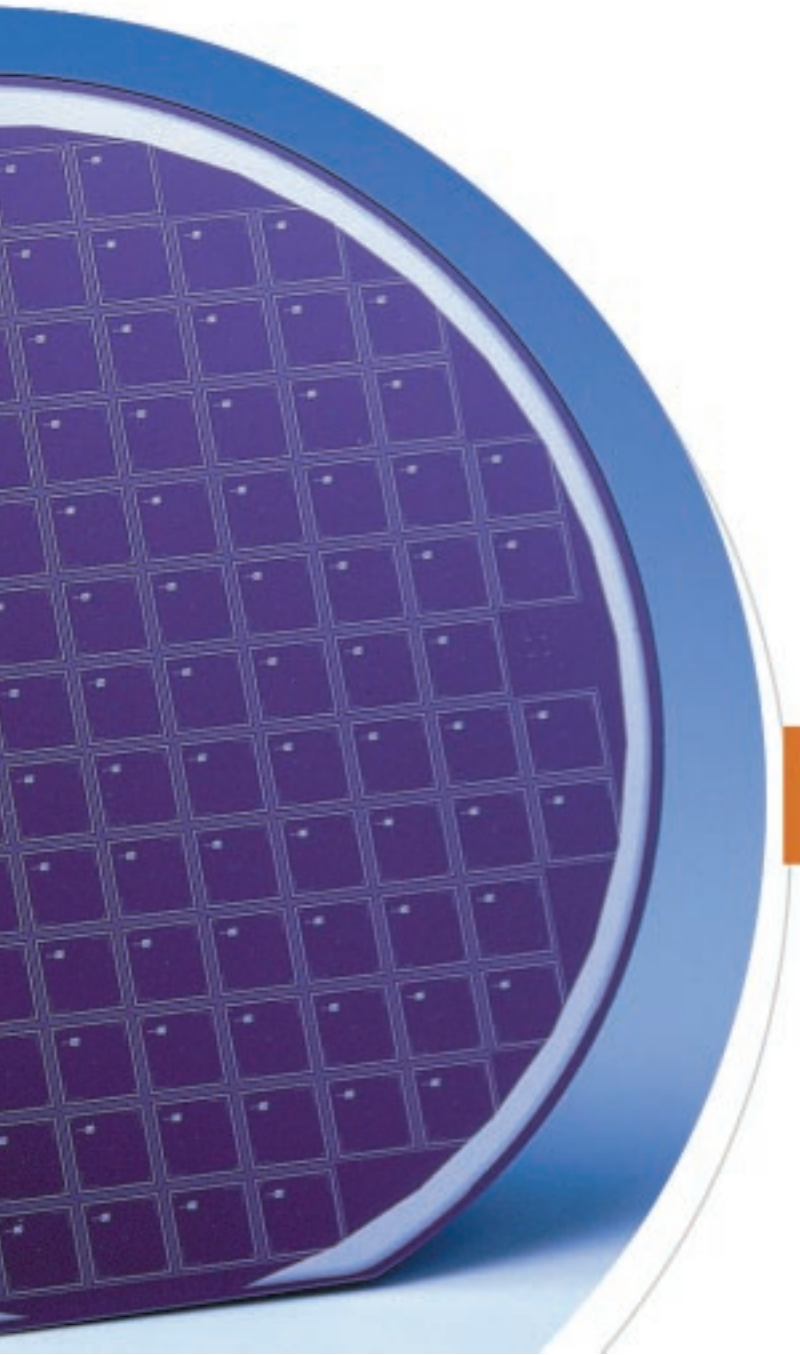
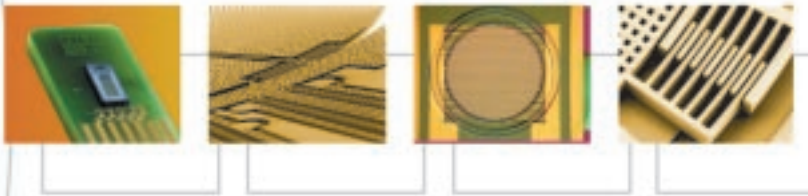
ISIT

Fraunhofer Institut Siliziumtechnologie



Achievements and Results
Annual Report 2003



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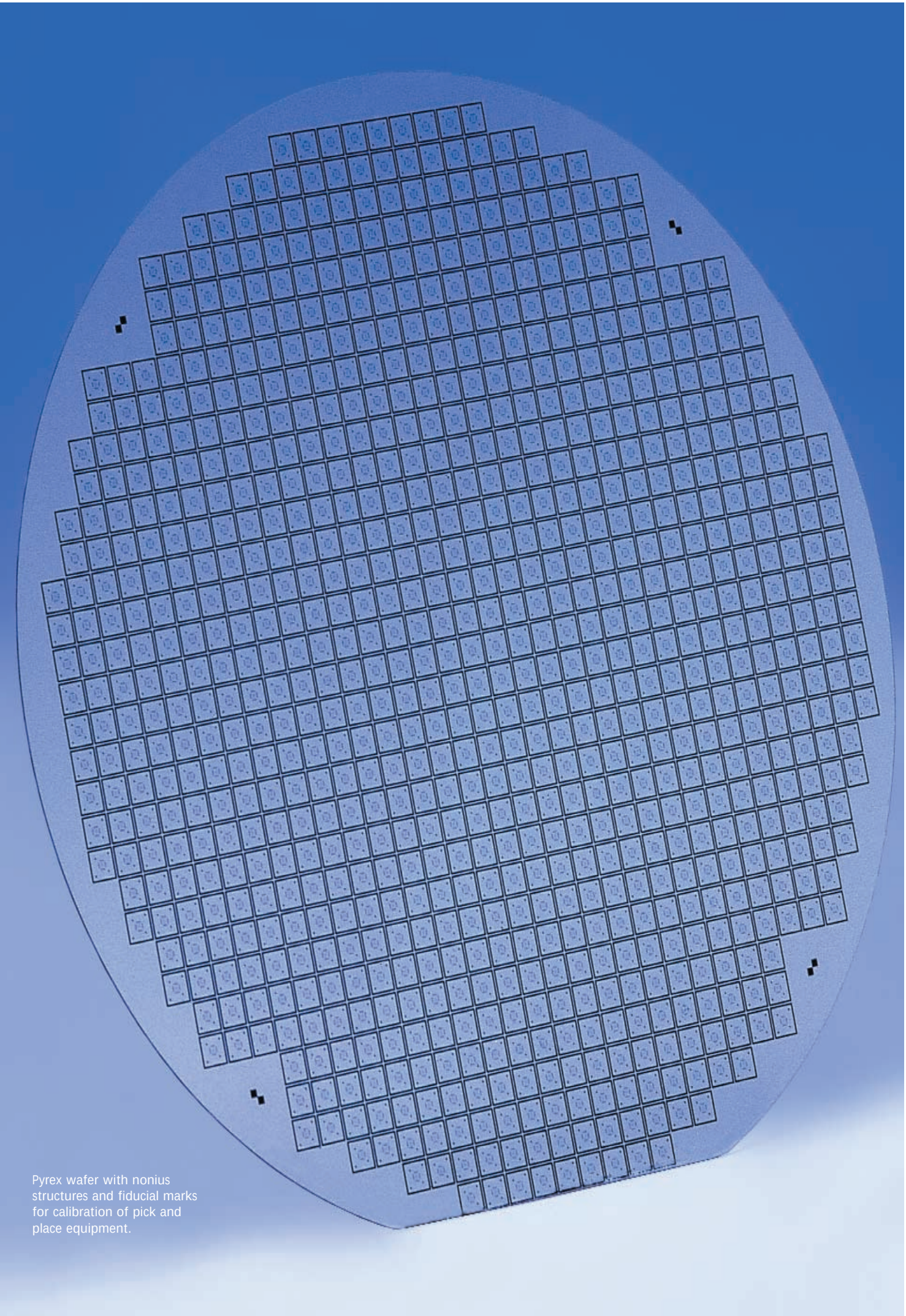


Pyrex wafer with nonius structures and fiducial marks for calibration of pick and place equipment.

Preface

In 2003, major milestones were achieved for the development of Itzehoe as a high-tech location. Altogether nearly 600 jobs have now been created at all the institutions set up there.

The outstanding event of the year was without doubt the opening of the development and administration building of Silicon Manufacturing Itzehoe SMI GmbH directly next to the Institute. The company was formed with the participation of the Philips Group and cooperates closely with the ISIT. SMI intends to establish itself as a microsystems (MEMS) development partner and supplier, with the aim of bringing product ideas to the market quickly at competitive prices. The product range is varied: It extends from telecommunications and automotive technology to bioengineering and health care sector. SMI benefits from the experience available at Philips in semiconductor production and the technological know-how available at the ISIT. At the end of 2003, SMI had more than 20 permanent employees.

In the past year, ISIT and SMI completed a major cooperation project involving the assembly and packaging of highly integrated microelectronic and micromechanical components. This wafer level packaging (WLP) is regarded as the assembly technology of the future, because the resultant packages are very small, not bigger than the silicon chip itself (chip-size packages). This process is favored by more and more chip manufacturers around the world. SMI and ISIT have set up Europe's first and only industrial packaging line for WLP.

The chip-size packaging project is the first cooperation between ISIT and SMI. The aim is to extend the cooperation with SMI into the entire field of microsystems engineering and to also expand it significantly in terms of quantity. ISIT is already the biggest independent MST foundry in Germany and can offer the entire chain of services from system development, design, simulation and prototyping to production. Production is, however, limited to 50,000 wafers per year and the current production line is designed for 6" wafers. With the support of ISIT, SMI will install a further clean room at the location for the production of microsystems on 8" wafers.

ISIT's main cooperation partner on site, Vishay Semiconductor Itzehoe GmbH, has also decided to invest about 10 million dollars in order to expand its production facilities here. This underlines the importance of the Itzehoe location for Vishay as an international group. An epitaxy center is to be built to supply the Vishay Group with epi wafers. Important production steps will be brought to Itzehoe which up to now have been carried out at the American parent company. These facilities will enable Vishay Itzehoe to modify its products more quickly and therefore to respond more flexibly to the market. What's more, Vishay intends to expand its equipment to include plasma and metallization equipment for new generations of densely integrated power components. ISIT and its customers will also benefit from this equipment update.

The development of the location over recent years would not have been possible without the involvement of the regional government, and I would

ISIT-cooperation partners in Itzehoe: IZET Innovationszentrum (left), Solid Energy GmbH and Condias GmbH (above), Silicon Manufacturing Itzehoe SMI GmbH (right), Vishay Semiconductor Itzehoe GmbH and Fraunhofer ISIT (bottom).

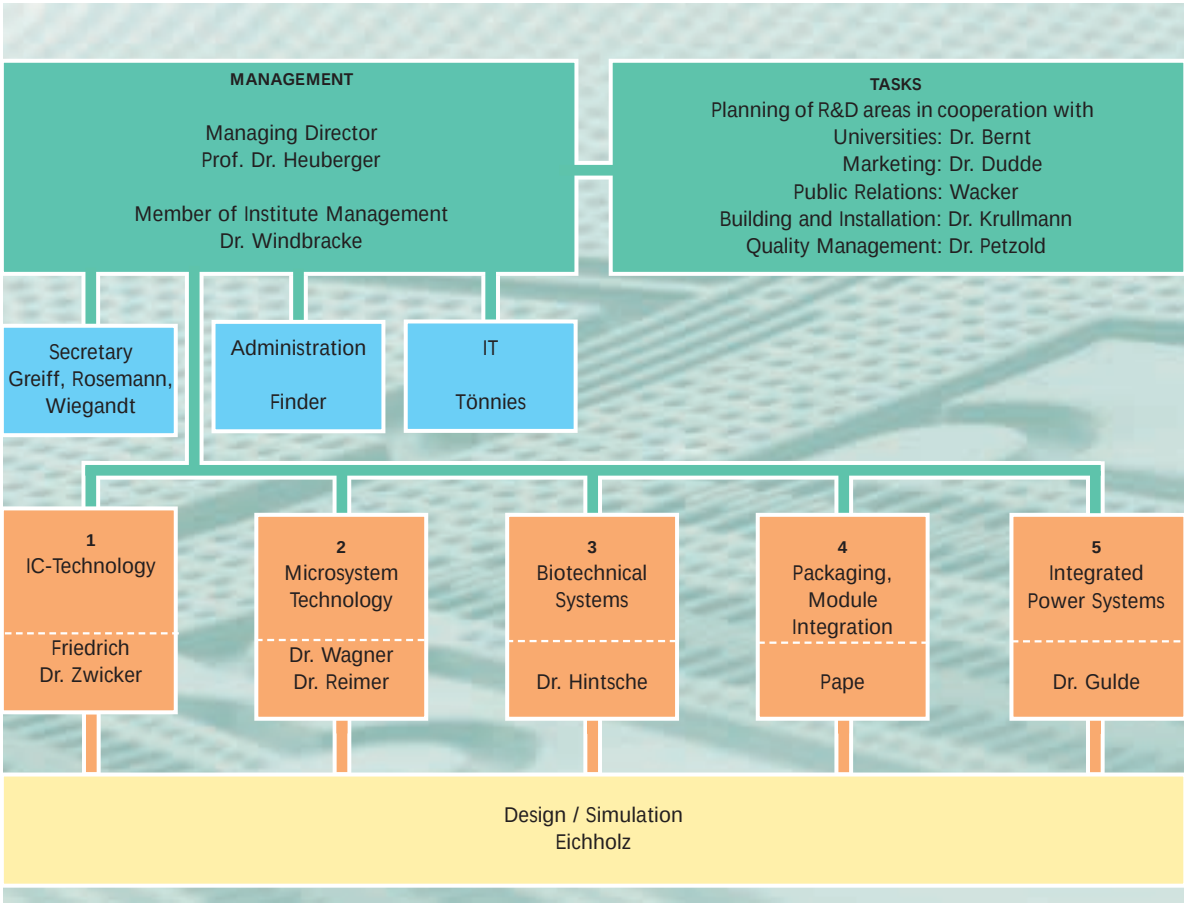
SMI office building.

like to express my thanks for this once again at this point. With the support of the Schleswig-Holstein government, ISIT is, for example, currently developing a microsystems processing sequence for the monolithic integration of piezoceramics with silicon. The object of the project is to provide new, more powerful and faster-acting force-generating mechanisms for the use in microsystems, with a view to reduce production costs. The system allows to manufacture inkjet printer heads for solid inks or rapid-action microvalves capable of generating the high closing forces required, for example, in automotive applications.

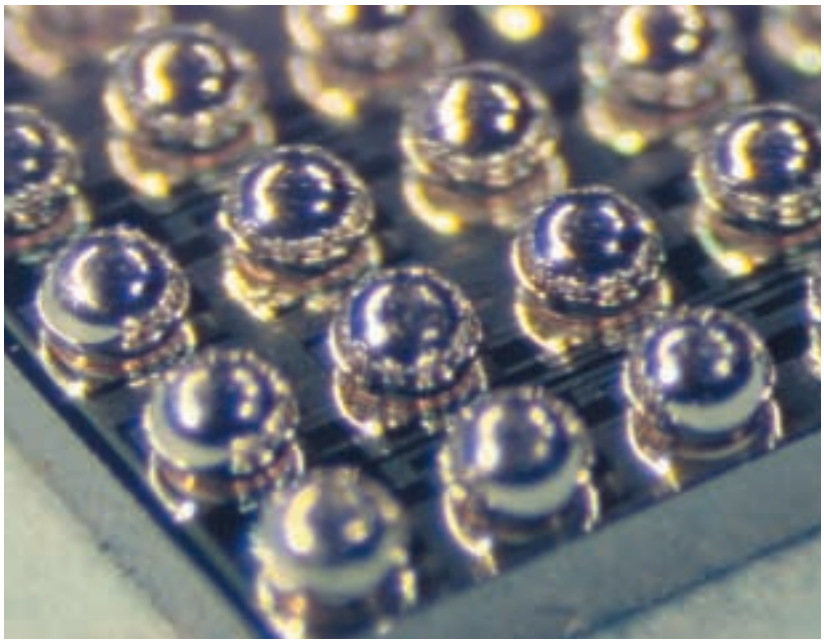
Apart from the distinctly innovation-friendly climate that exists in the area, a major reason why companies choose to locate to Itzehoe is the proximity of the town to various universities of applied sciences providing a reliable source of highly qualified engineers and skilled workers.

To satisfy the demand for skills in microsystems and semiconductor technology, as required for the development of the high-tech location, ISIT has for a long time been cooperating closely with schools and universities in the region. Three years ago, with support from the Institute, the local vocational college in Itzehoe established an apprenticeship scheme leading to a new official diploma in microtechnology. Itzehoe is now the center for training in microsystems and semiconductor technology for all of northern Germany. The first young qualified microtechnologists completed their apprenticeship last summer, and have all found a good starting point for their career in and around Itzehoe. The universities of applied sciences, too, are interested in cooperation with ISIT. Collaboration with the Fachhochschule Westküste in Heide, for example, was intensified last year and is currently being formalized in a cooperation agreement.

ISIT Organigram



Chip Size Package ready for placement.

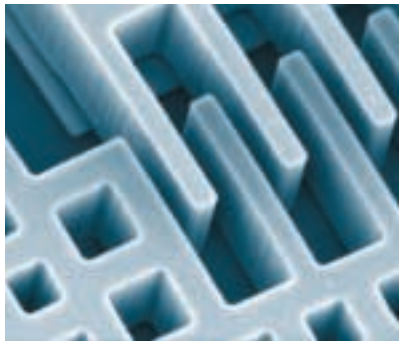


With its concept for developing closer links between research and procuction industry, Fraunhofer ISIT is leading the way towards the paradigm shift in the focus of technological research in Germany needed to face the challenges of the future. The greatest problem facing German research is not that there is any lack of ideas and findings, but that the results of research and development work are not transferred quickly enough into practical application. In future, the research community must take this matter into its own hands and demonstrate ways in which the results of its R&D can be transferred to industrial applications.

A key government instrument for promoting this paradigm shift is the support given to projects conducted jointly between research establishments and industry. From the perspective of the national economy, the promotion of project-based joint industrial research is extremely important for several reasons. Innovative projects extending over a period of more than two years are rarely undertaken without external funding, because the competitive market forces major industrial firms and small business alike to plan within a short-term horizon. Without financial support, high-risk interdisciplinary projects would not be tackled either. What's more, this form of project funding has an European dimension. Only in areas where projects are supported at national level is an adequate level of return funding received from the EU, and without project support German industry is excluded from major European collaborative research programs (e.g. Eureka, Medea, Eurimus).

Unfortunately, the funding of joint projects between science and industry in Germany is in a deep structural crisis. Through its long-term commitments to basic research, the government has lost its scope for action and, in order to balance the budget, regularly cuts back on joint research work with industry whenever money is limited. Project funding is therefore subject to considerable fluctuations and difficult to plan in advance. At present the situation is particularly critical. Apart from a few exceptions, no new projects were approved in 2003. This entails direct consequences for ISIT.

Surface micromachined polysilicon structures for inertial sensing.

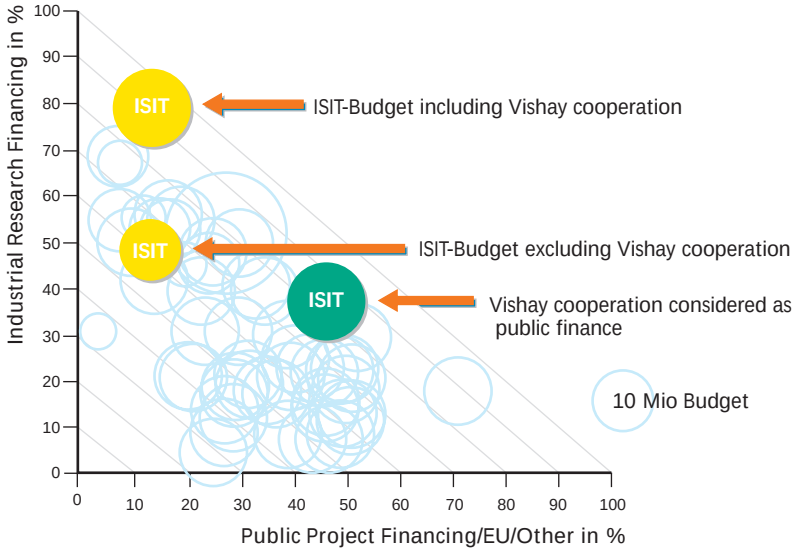


Due to the budgetary constrains the German research ministry has withdrawn the originally planned funding for four major projects in the last year. Fortunately, over the past few years, ISIT has made up for the shortfall in project funding by engaging in additional industrial projects. As a result, ISIT finances approx. 85 % of its needs from industrial projects, and even if all the payment flows connected with the research contract with Vishay are excluded, ISIT still earns close on 50 % of its income from industry. This situation is reflected in the chart illustrated below. It is to be hoped that the financial situation of the German research ministry changes soon, because in industry-related R&D, too, high-risk long-term projects can only be carried out with the aid of funding.

Quality roadmap for the qualification of ISIT as a supplier for the automotive industry.

ISIT accomplished the necessary paradigm shift some years ago with its combination of contract-based development and production of new microsystems and microelectronic products in the same technology line. In silicon technology in particular, the traditional demarcation between research and development on the one hand and production on the other has no longer functions. Product development in an R&D context followed by transfer to a manufacturer is too expensive, too time-consuming and in many cases not even possible owing to the incompatibility of the technologies involved. The industrial customer needs a product at a competitive price and not the half-finished result of an R&D project. Experience at ISIT shows that development work conducted in conjunction with a production line is more efficient and economical, and that it facilitates a smooth transfer into the production environment.

Overview of Source of Financing among all Fraunhofer Institutes in 2003.



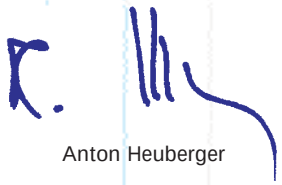
From the business perspective, 2003 was a difficult year for the Institute, but it also had many positive aspects. The situation was difficult in economic terms for two reasons. Firstly, the Institute is affected by cutbacks in government project funding as already described, and although institutional funding for the Fraunhofer-Gesellschaft was increased slightly overall, this is of little help. Secondly, the Institute was only able to obtain EU project funding to a much lesser extent than in previous years. The main reason for this decrease is the transition from the fifth to the sixth EU Framework Programme. Nevertheless, ISIT can report major successes

from its work: The expansion of cooperation with SMI in the area of chip-sized packages has already been mentioned. Work on the development of electronic biochips also yielded pleasing results last year. For instance, fully automated analysis systems developed at ISIT for detecting warfare agents were successfully tested by the German armed forces.

Particular mention should be given to sensor-based microsystems, especially those incorporating inertial sensors, as they hold considerable importance for automotive applications. Germany is the unrivaled leader in the field of the automotive industry, and this facilitates the domestic marketing of microsystems. According to an analysis made by the German Electrical and Electronic Manufacturers' Association (ZVEI), Germany is the biggest market for micro-mechanical sensors, with more than 80 % of these components being developed and produced for the automotive industry. Germany holds almost 50 % of the world market in this product sector. Over the next few years there will be a distinct increase in the amount of electronically controlled equipment installed in automobiles and so considerable growth in microelectronic and microsystems technology for use in the car industry can be expected. Double-digit growth rates are forecasted for this sector.

To ensure that the Institute is equipped for this market and can meet the requirements of its industrial customers, microengineered components are developed, tested and produced at ISIT on the basis of a quality management system. This system has been built up over the past two years and in 2003 was certified under ISO 9001:2000. In addition, with a view to present and future production and development activities for the automotive industry, rapid preparations are being made for certification under TS 16949.

In conclusion, I express my thanks to the employees of ISIT for the work they have performed. Their commitment, performance and motivation were the key elements behind the success achieved by the Institute in a financially difficult year. I am particularly pleased with the results of a staff survey conducted in September throughout the Fraunhofer-Gesellschaft, which showed that the majority of staff is satisfied with ISIT as an employer and that the Institute has fulfilled their needs and expectations. Nearly 61% of the Institute's staff stated that they would stand by their decision to work for ISIT. That is one of the best ratings among all the Fraunhofer Institutes. For me, this result is an incentive to ensure that this continues to be the case.



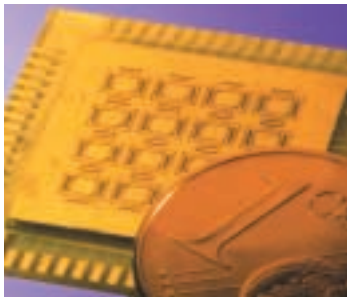
Anton Heuberger

Brief Portrait

Fraunhofer ISIT
Research and Production at one Location

The Fraunhofer-Institut für Siliziumtechnologie (ISIT) develops and manufactures components in microelectronics and microsystems technology, from the design phase – including system simulation – to prototyping and fabrication of samples, up to series production. Though components such as valves and deflection mirrors manufactured by Fraunhofer ISIT often measure just a fraction of a millimeter in size, their range of applicability is anything but small: the devices are implemented in areas as diverse as medicine, environmental and traffic engineering, communication systems, automotive industry, and mechanical engineering. Working under contract, ISIT develops these types of components in accordance with customer requirements, also creating the application-specific integrated circuits (ASICs) needed for the operation of sensors and actuators. Included in this service is the integration into the overall microsystem using miniaturized assembly and interconnection technology.

Device development and production at ISIT is ISO 9001 certified.



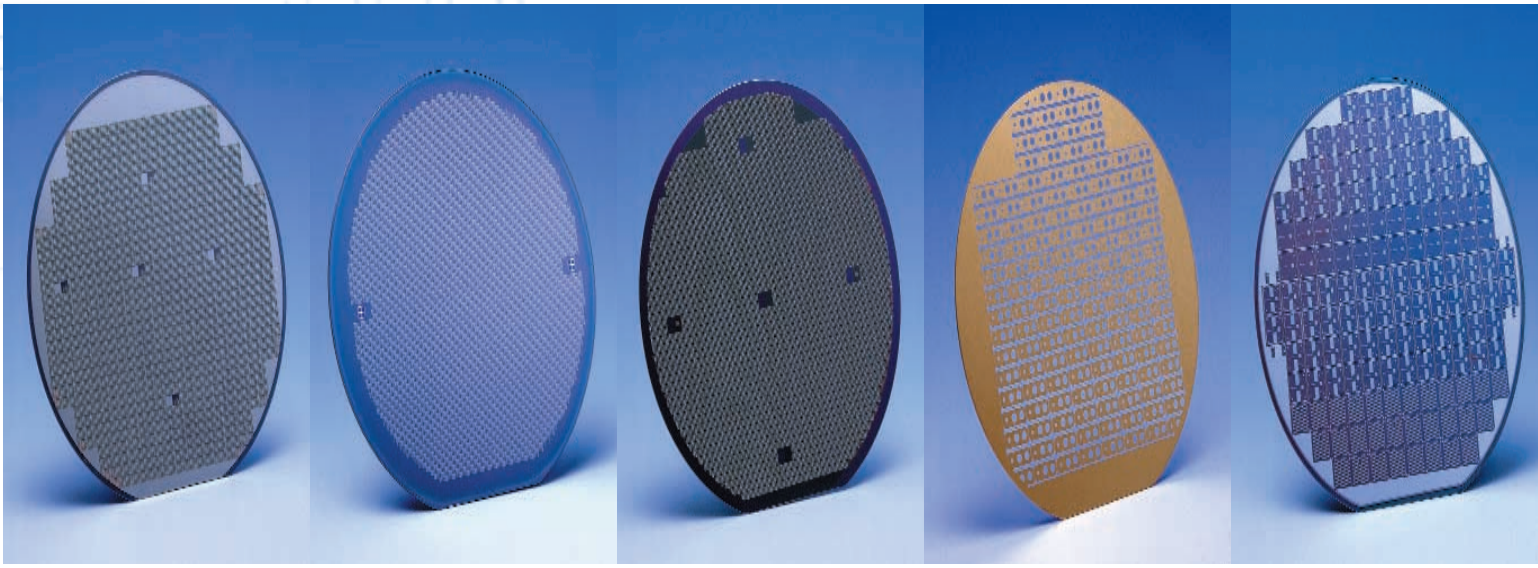
4 x 4 micromirror array of 2D-scanners.

Together with Vishay Semiconductor Itzehoe GmbH, the institute operates a professional semiconductor production line which is up-to-date in all required quality certifications. The line is used not only for producing microelectronic components (PowerMOS) and microsystems, but also for R&D projects aimed at developing new components and technological processes. An ISO-9001-certified quality management system serves as the basis for the development, qualification and production of micro-engineered components.

Other groups at ISIT carry out work on assembly and packaging techniques for microsystems and sensors, analyze the quality and reliability of electronic components, and develop advanced power-supply components for electronic systems.

The institute employs a staff of around 150.

Different test wafers for process evaluation.



Main Fields of Activity

Microsystems Technology (MEMS) and IC Design

The work performed at the institute focuses predominantly on microsystems technology, an area which ISIT pioneered in Germany. For over 20 years ISIT scientists have been working on the development of micromechanical sensors and actuators, micro-optic and fluidic components, and components for radio-frequency applications (RF-MEMS). Their work in this area also includes integrating these components with microelectronics to create novel systems. A multitude of components and systems have originated at ISIT.

The current emphasis in the area of sensor technology is on inertial sensor technology (motion, inclination, acceleration, angular rate, IMU) and pressure, temperature and flow sensors (particularly gas flow), all with integrated electronics (ASICs). The development of customized integration concepts, ranging from simple, cost-effective assembly in a common package to complete monolithic integration, represents the core of ISIT's offerings in this area. One integration technique that customers may find particularly valuable is the ability to mount a microsystem on the surface of a fully processed ASIC wafer using a low-temperature process such as electroplating.

Among the key fluidic components created at ISIT are pneumatic valves, bi-stable fluid valves, sensor-controlled automatic microdosing devices, and micropumps, all of which can also be employed in Lab-on-Chip systems.

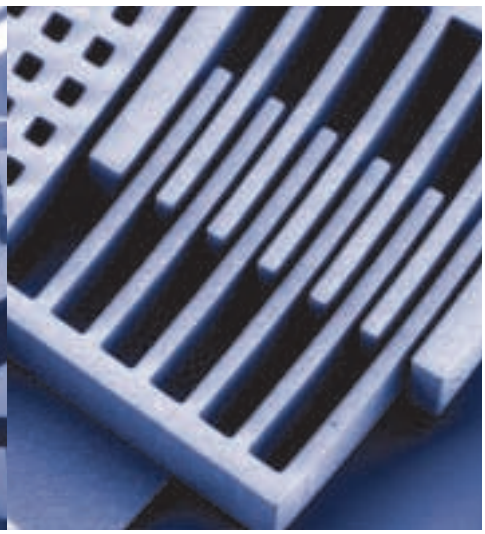
ISIT also develops optical microsystems, primarily for optical communication and instrumentation. Examples include micromirrors for laser displays, laser scanners and digital light modulators, and passive optical elements such as refractive and diffractive lenses, prisms, or aperture systems.

Radio-frequency microsystems developed at ISIT, designed primarily for use in wireless communication devices, include microrelays, highfrequency switches and tunable capacitors.

Systems that utilize actuators need to be able to generate the forces necessary for the device to interact with its environment. In order to meet the special requirements of microscopically small

MEMS devices under RF testing.

3D electrodes for high efficiency electrostatic actuation.



Electrostatic comb drive.

Resonant Silicon scanner (left).

Mounted air flow sensor (right).

systems, ISIT implements electrostatic, thermal and – more recently – piezoelectric power.

The ISIT approach enables the institute to offer its customers all of these components as prototypes and also to manufacture them in series according to the customer's specific needs, utilizing the institute's in-house semiconductor production line wherever possible. The services provided also include application-specific microsystem packaging at the wafer level, using advanced wafer bonding methods.

Should a customer's requirements fall outside the scope of the institute's technological capabilities, ISIT can utilize an European network to gain access to other manufacturers and processes, like production lines at Bosch, SensoNor, HL Planar, ST and Tronic's. ISIT organizes the production as a foundry service for interested customers. And with the settlement of SMI GmbH in Itzehoe, the institute has gained a key partner for producing microsystems and related components as a foundry service under customer contract.

One of the prerequisites for developing original microsystems and microelectronic components is a highly capable circuit design group. The staff at ISIT are specialists in the design of analog/digital circuits, which enable the electronic analysis of signals from silicon sensors. The circuit designers at ISIT also devise micromechanical and micro optic elements and test their functionality in advance using FEM simulation. To carry out these assignments, the team has modified commercial design tools to meet the specialized challenges of microsystems technology.

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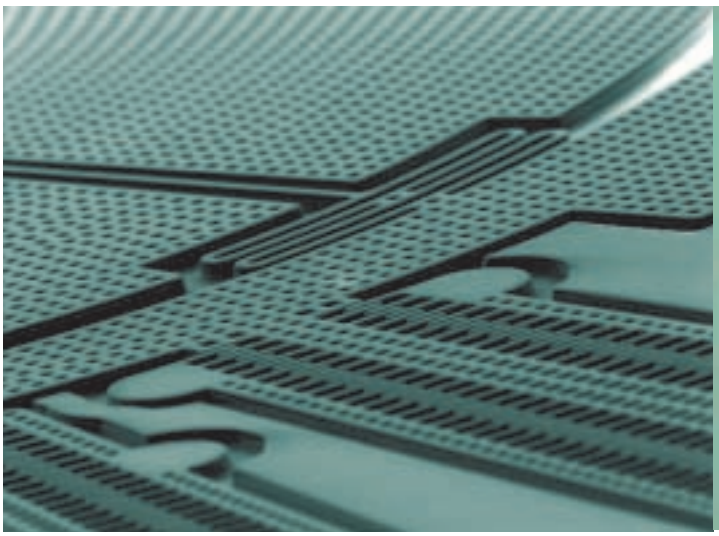
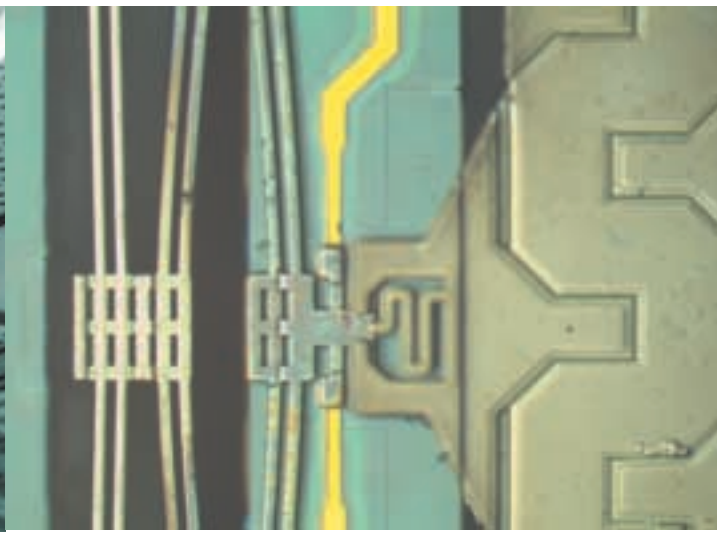


Inertial microsensor structure.



Bistable thermomechanical micro relay.

IC Technology and Power Electronics

The power electronics and integrated circuits group develops and manufactures active integrated circuits as well as discrete passive components. Among the active components the main concern lies on power devices such as smart power chips, IGBTs, bi-directional components, PowerMOS circuits and diodes. Thereby ISIT primarily uses Vishay's customized, individual production sequences. Additional support for work in this area is provided by an array of modified tools for simulation, design and testing. The ISIT also benefits from years of experience in the design and construction of CMOS circuits.

The passive components developed and fabricated at ISIT are primarily chip capacitors, precision resistors and inductors. Materials development and the integration of new materials and alloys into existing manufacturing processes play an important role in the development process.

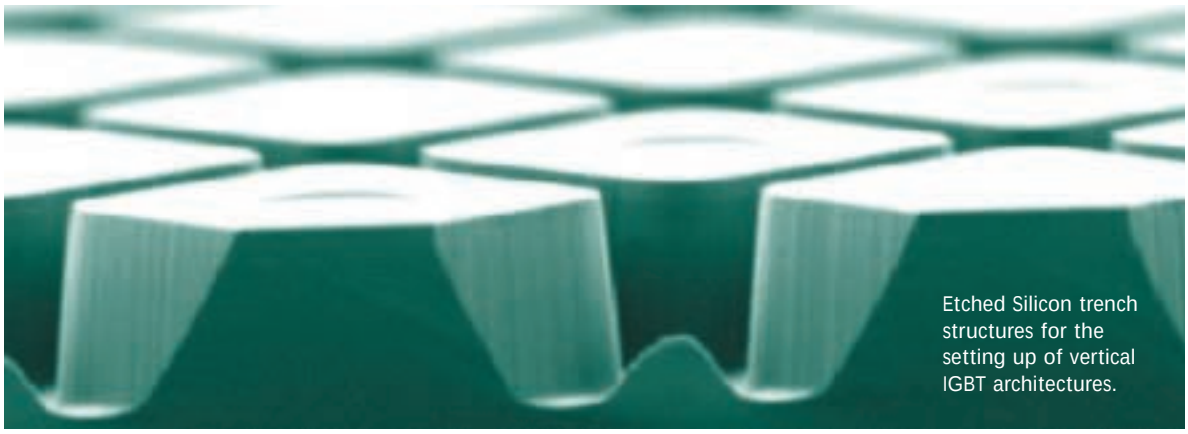
ISIT develops individual processes, process modules and complete process flows for diverse applications. The institute also offers customer-specific silicon components processing in small to medium-sized batches on the basis of a qualified semiconductor process technology.

To support the development of new semiconductor production techniques, production equipment of particular interest is selected for testing and optimization by the ISIT staff. This practice provides the institute with specialized expertise in challenges related to etching, deposition, lithography, and planarization methods. Planarization using chemical-mechanical polishing (CMP) in particular is a key technology for manufacturing advanced integrated circuits and microsystems.

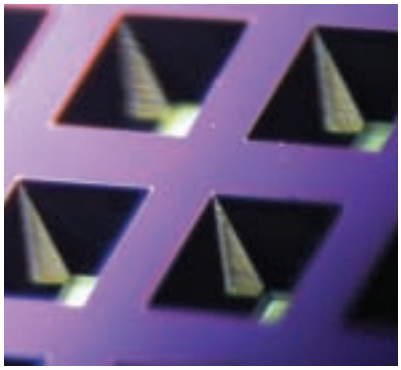
The intensive work done by ISIT in this area is supported by a corresponding infrastructure: The institute's CMP application lab is equipped with CMP cluster tools, single- and double-sided polishers and post-CMP cleaning equipment for wafers with 100 to 300 mm in diameter.
The CMP group at ISIT works in close relationship to Peter Wolters Surface Technologies GmbH since many years, as well as other semiconductor fabrication equipment manufacturers, producers of consumables, CMP users and chip and wafer manufacturers.

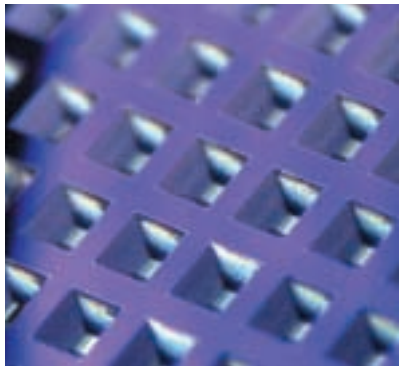
The group's work encompasses the following areas:

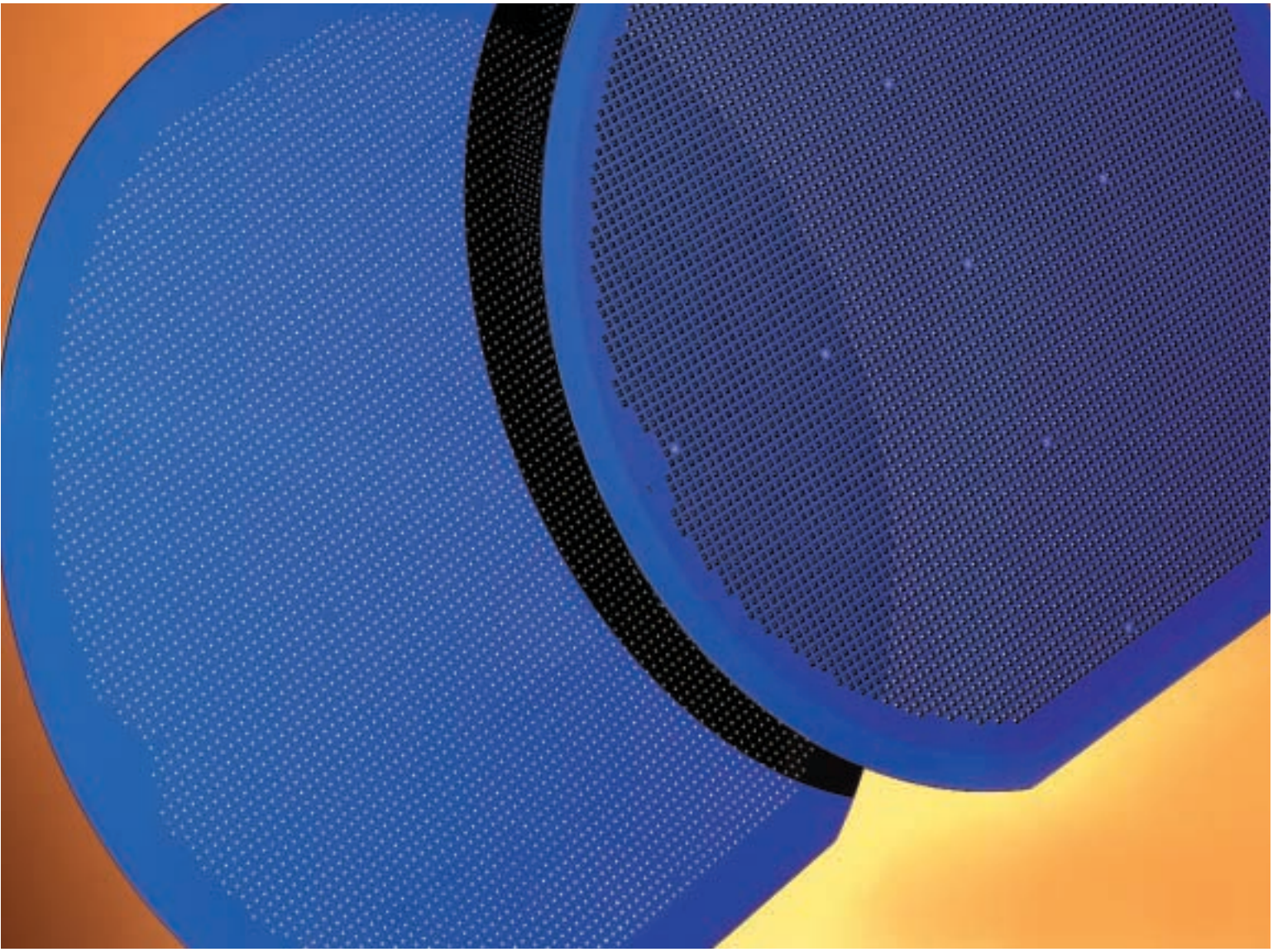
- Testing of CMP systems and CMP cleaning equipment
- Development of CMP processes for
  - Dielectrics (SiO_2, TEOS, BPSG, low-k, etc.)
  - Metals (W, Cu, Ni, etc.)
  - Silicon (wafers, poly-Si)
- Testing of slurries and pads for CMP
- Post-CMP cleaning
- CMP-related metrology
- Implementation of customer-specific polishing processes for ICs and microsystems



Etched Silicon trench structures for the setting up of vertical IGBT architectures.







Carrier substrate for an ultra thin wafer handling concept (top: details).

Chip production in the ISIT cleanroom.

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Biotechnical Microsystems

ISIT is worldwide leading in electrical biochip technology, and is holding around 20 patents in the area. In contrast to the functionality of optical biochips, redox molecules can be directly detected by the underlying circuit on the surface of ISIT's electrical biochips through a biochemical reaction. Employing new ultramicroelectrodes enables the construction of powerful sensor arrays and the use of ultra-sensitive, ultra-selective measurement techniques, such as "redox recycling". In combination with microfluidic components and integrated electronics, these electrical biochips represent the fastest and most cost-effective basis for mobile analysis systems, which can be used to detect and identify DNA, proteins like biowarfare agents and haptens like antibiotics for example.

For this kind of biochips multi-channel analysis devices are developed, which can detect a variety of analytes simultaneously. These types of biochips might be implemented in future "lab-on-chip" systems. In the field of bioanalysis, ISIT works closely with the Itzehoe-based company eBiochip Systems GmbH, an ISIT spin-off, to facilitate the marketing with these new technologies.

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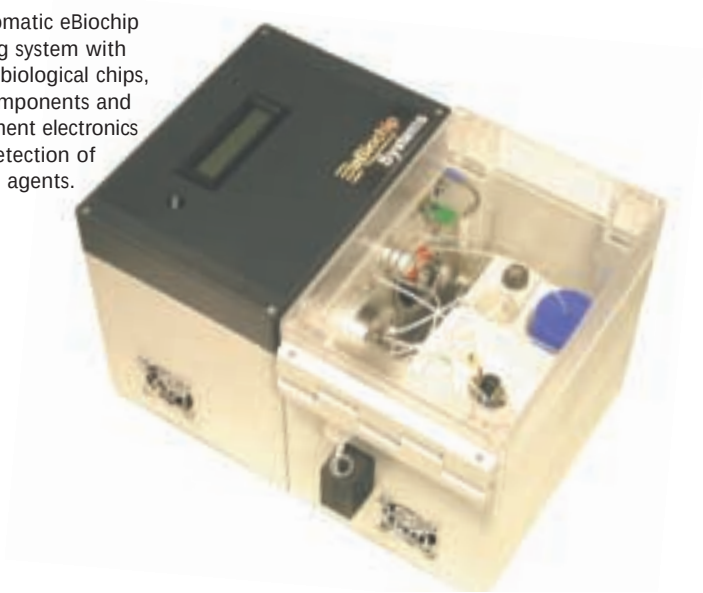
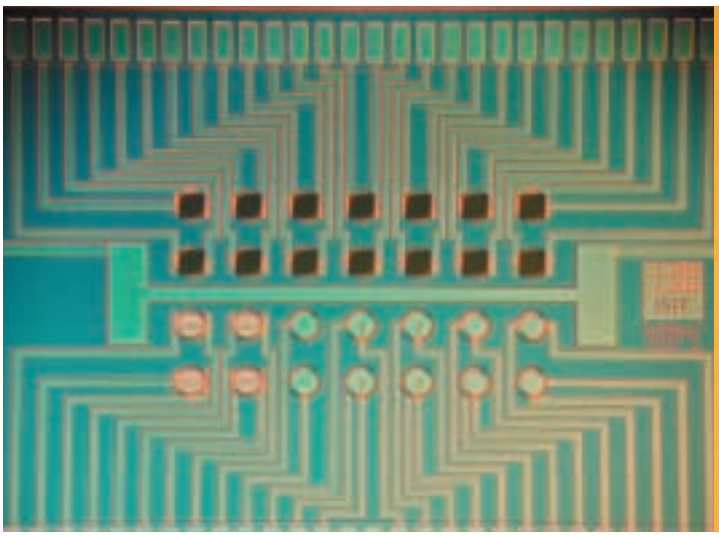
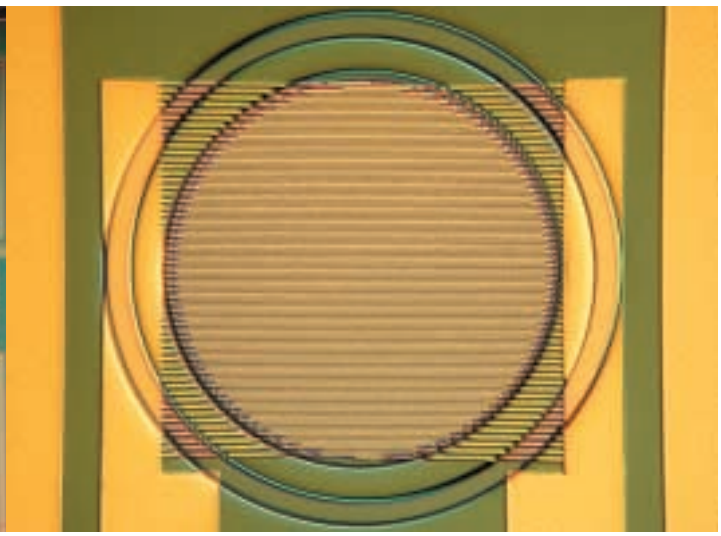


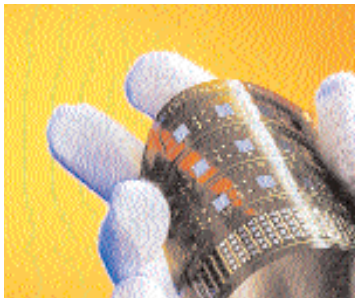
Fully automatic eBiochip measuring system with electrical biological chips, fluidic components and measurement electronics for the detection of biological agents.

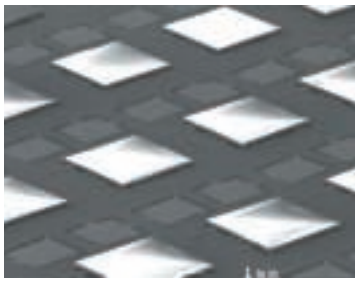
Electrical Silicon biochip.





Detail of an electrical biochip with ultramicroelectrodes. The Gold electrodes are adjusted to each other in the nanometer range.





Thin Silicon chips (50 µm) on flexible substrate. With such test boards modern pick and place equipment can be evaluated and optimized. Overview (top) and detail (bottom).

Packaging Technology for Microelectronics and Microsystems

The assembly and interconnection technology group offers customers a broad range of services, including precision assembly of microstructured components and development and qualification of customer-specific packaging. Work in this area includes hermeticity and material compatibility tests for assemblies that have to work in aggressive environmental conditions, e.g., analysis of microsystem packages intended for in vivo use in medical technology.

Another focal area is miniaturization of chip and sensor assemblies and packages, which includes direct assembly of bare silicon chips. The institute possesses capabilities in all of the essential technical stages for chip-on-board (COB) technology, from designing the circuit boards to qualified COB assemblies. The bare ICs and microsensors are mounted using the Chip & Wire or Flip-Chip techniques.

The group also develops processes for assembling and packaging chips and sensors/actuators while still on the wafer. Due to the increasing global trend among chip manufacturers to implement this special packaging process, Wafer Level Packaging (WLP) – now considered the assembly technique of the future – has become a central focus of the group's work. WLP technology can also be applied for packaging sensors under vacuum, such as angular rate or acceleration sensors. ISIT is active in this area not only as a technology developer, but also as a manufacturer of assemblies for its customers using the available Chip-Size-Packaging production line.

The group also develops ultra-thin electronic assemblies, which involves mounting flexible silicon chips as thin as 50 µm on flexible substrates.

These techniques will ultimately lead to further miniaturization in existing systems, such as laptops, hand held PCs or mobile phones, but will also enable the development of new products like intelligent flexible product labels or smart clothes.

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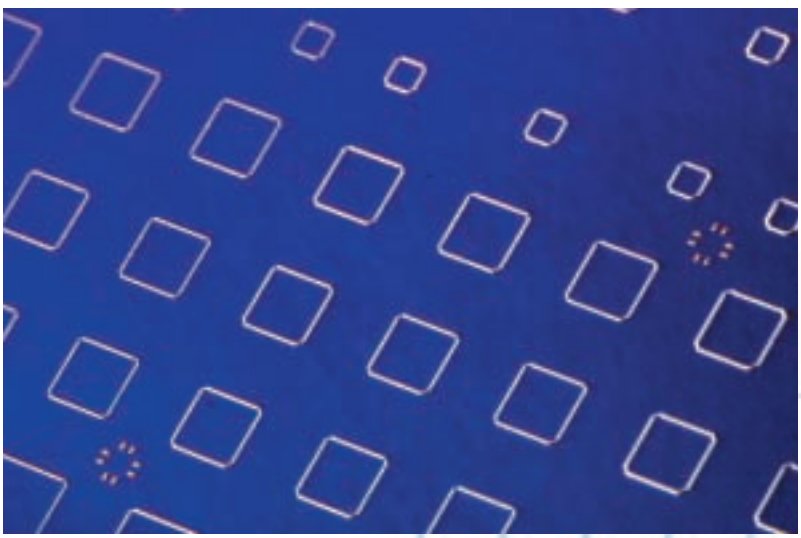


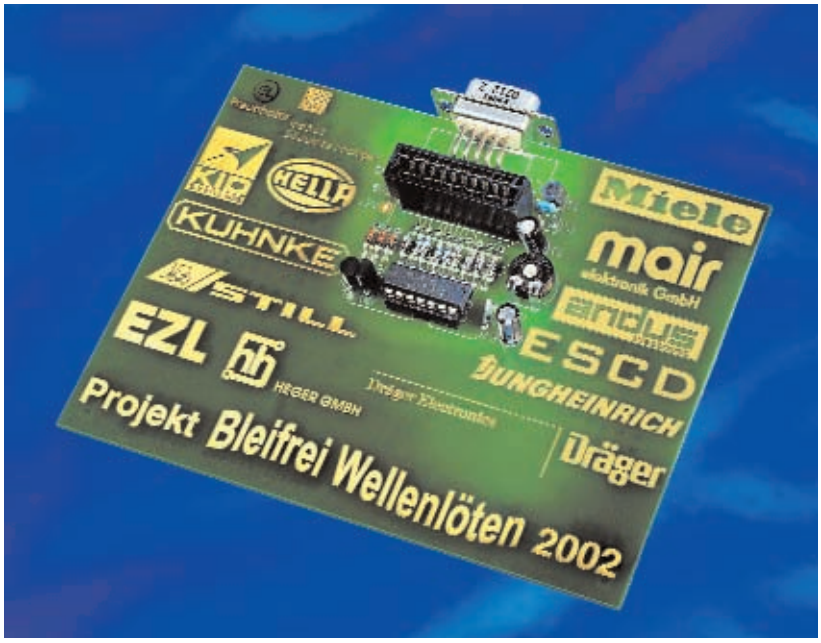
Diffferent solder frames on test cap wafer for MEMS encapsulation (right: details).

Quality and Reliability of Electronic Assemblies

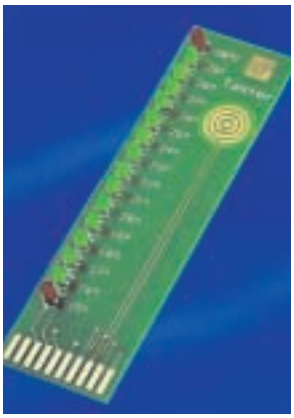
Quality evaluation – in particular for the soldering work done in pre-production, pilot and main series lots – represents a continuous challenge for ISIT, for example whenever new technologies such as lead-free soldering are introduced, when increased error rates are discovered, or if the institute desires to achieve competitive advantages through continual product improvement. To reveal potential weak points, ISIT employs both destructive and non-destructive analysis methods, such as x-ray irradiation. Working from a requirements matrix, ISIT scientists also evaluate long-term behavior of lead-free and lead-containing assemblies alike. They then formulate prognoses on the basis of model calculations, environmental and time-lapse load tests, and failure analysis.

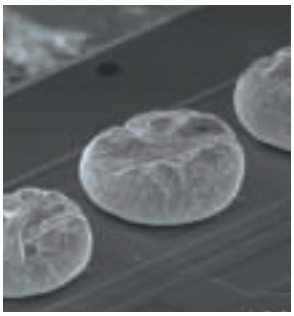
In anticipation of a conversion to lead-free electronics manufacturing, Fraunhofer ISIT is undertaking design, material selection and process modification projects. To effect a further optimization of manufacturing processes, the institute applies process models and produces samples on industry-compatible equipment. The group also addresses issues related to thermal management and reliability for customer-specific power modules.

In addition to these technological activities, the group regularly holds training sessions, including multi-day classes, at the institute or at company site.



Demonstration board showing lead free through hole wafe soldered components.
(top: base; right: display)





Deformed solder balls due to thinning and cleaning of wafers.

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Lithium polymer rechargeable battery: low weight, scalable, powerful, flexible in design.

The growing use of a wide array of mobile electronic devices is generating an increased demand for rechargeable batteries that are lighter, yet provide increased power density. Along with an exceptional power capacity, consumers expect long battery lifetime, increased safety and a higher degree of environmental compatibility. A new Lithium rechargeable battery design developed by ISIT over the last few years – for which the institute has submitted a patent application – is capable of meeting these demands. This new concept, which features solid-state electrolytes, affords the same high power density typical of Lithium-ion rechargeables, but because the materials used in the new battery are inert, it does not need the complicated hermetic packaging technology required with conventional Lithium-ion batteries, which contain liquid electrolytes. The battery needs only a metallized plastic foil packaging to make it air- and moisture-tight, resulting in a lower overall weight for the finished product.

The base material for ISIT's Lithium battery production process is a foil material. This allows batteries to be made in a much greater variety of shapes and sizes, thus significantly diversifying the range of possible applications.

ISIT offers the following services in this area: development, fabrication and small series production of customer-specific battery formats (ranging in size from microsystems to laptops) in a broad range of available ampere-hour ratings, with various forms of housings and materials (e.g. plastic or Titanium). Following the preparation of samples, ISIT supports the customer in the transition to series production. The institute also provides application-specific material selection of various compounds for cathodes (e.g. Lithium Cobaltite, Lithium Iron Phosphate) and anodes (Graphite, Lithium Titanate, etc.) to ensure optimal conformity to the application requirements (e.g., power density, cycle stability, capacity, product life cycle, self-discharge rate.) ISIT has built an initial production line for an industrial-scale production process. The institute's spin-off company Solid Energy GmbH was founded and set up near the ISIT facility to manufacture the batteries.

Upper: Sample product from battery pilot production.

Down: Customized batteries (5.5 x 16 x 100 mm³) with safety electronics for new penphones (electronic reading pen with scanner camera, GSM module and bluetooth module).

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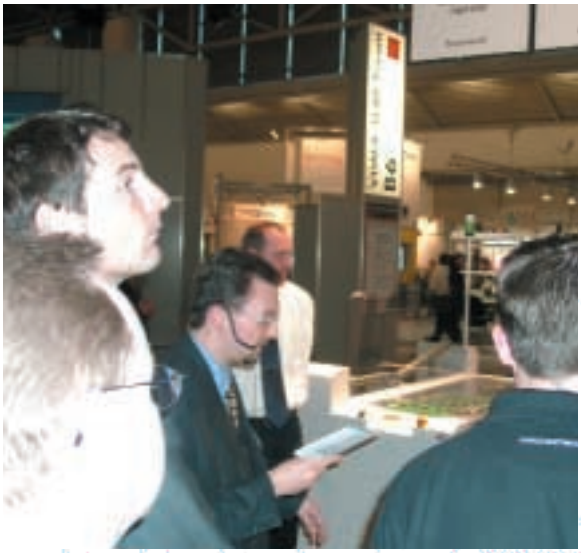
Facilities and Equipment

In terms of both space and technical capabilities, the facilities at Fraunhofer ISIT provide an ideal environment for research & development work as well as production. In addition to its 150 mm silicon technology line and 2500 m^2 of clean-room space, the institute has a further 450 m^2 of clean-room area (class 100) for specific microsystems engineering processes, including: wet-etching processes, high-rate plasma etching, deposition of non-IC-compatible materials, lithography with thick resist layers, gray-scale lithography, electroplating, microshaping and wafer bonding. Further 200 m^2 clean-room (class 10-100) is equipped for chemical-mechanical polishing (CMP) and post-CMP cleaning. ISIT also offers a diverse selection of labs (1500 m^2) that are utilized by working groups for the development of chemical, biological and thermal processes, electrical and mechanical component characterization, and for assembly and interconnection technology. A spin-off arising from the work in assembly and interconnection technology – a CSP (Chip-Size Packaging) production line with an annual capacity of 100,000 wafers – was built in the ISIT clean rooms in collaboration with SMI GmbH (Silicon Manufacturing Itzehoe).
The line is jointly operated by ISIT and SMI.
The ISIT facility also operates a pilot production line for Lithium-polymer rechargeable batteries with power capacities of up to several ampere-hours.

ISIT cleanroom in the diffusion furnace area.



Spectrum of Services

The institute makes its range of services available to companies representing a wide variety of branches, including medical technology, communication systems, automotive industry, and industrial electronics, just to name a few. After industrial customers specify necessary requirements of the components and systems, ISIT engineers work closely with them to design, simulate and produce the components, systems and manufacturing processes. In this context, ISIT follows the technology platform concept, which entails defining standard process flows that can be used to manufacture a large group of components simply by varying certain design parameters. Applying this modular technology concept is the optimal way to ensure that ISIT continues to offer competitive prices to its customers.

ISIT services have attractive implications for small- and medium-sized enterprises, which can take advantage of the institute's facilities and expertise in realizing technological innovations up to products.

ISIT presentation at Sensor 03, Nuremberg (top).

ISIT at Productronica 03, Munich (above and right).

Demonstration of ultra thin flip chip assembly on industrial scale for smart labels.

Customers

ISIT cooperates with companies of different sectors and sizes. In the following some companies are presented as a reference:

ABB, Heidelberg

Advanced Electronics Energy, Hong Kong, China

Alcatel Kirk, Ballerup, Denmark

Alcatel Vacuum Technology, Annecy, France

Alcatel, Stuttgart

Amperex Technology Ltd. ATL, Hong Kong, China

Andus GmbH, Berlin

Applied Photonics, Hamburg

Atotech Deutschland GmbH, Berlin

Basler Vision Technologies, Ahrensburg

Beiersdorf AG, Hamburg

Beru Electronics GmbH, Bretten

Biotronik GmbH, Berlin

Borg Instruments, Remchingen

Bosch, Reutlingen

Bullith Batteries AG, München

Bundesanstalt für Materialforschung und –prüfung, Berlin

Card Guard, Rehovat, Israel

Cavendish Kinetics B. V., LA´s-Hertogenbosch, Netherland

CITIC Guoan, Mengguli Power Sources, Beijing, China

Condias GmbH, Itzehoe

Corning Frequency Control GmbH & Co. KG, Neckarbischofsheim

Daimler Benz Aerospace, Bremen

DancoTech A/S, Ballerup, Denmark

Danfoss Lighting Controls, Nordborg, Denmark

Danfoss Drives, Graasten, Denmark

Danfoss Silicon Power GmbH, Schleswig

Datacon, Radfeld/Tirol, Austria

Degussa AG, Hanau

Diabem, Barcelona, Spanien

Diehl Avionik, Überlingen

Disetronic Medical Systems AG, Burgdorf, Switzerland

Drägerwerk AG, Lübeck

Dräger Electronics GmbH, Lübeck

EADS, Ulm

eBiochip Systems GmbH, Itzehoe

Edan Technology, Taipeh, Taiwan

Elmos Semiconductor AG, Dortmund

Epcos AG, München

Eppendorf-Netheler-Hinz GmbH, Hamburg

ESCD, Brunsbüttel

ESW-EXTEL Systems GmbH, Wedel

EVGroup, Schärding, Austria

EZL, Limburg

Flextronics International, Althofen, Austria

FOS Messtechnik GmbH, Schacht-Audorf

Fresnel Optics, Apolda

Fuba GmbH, Gittelde

GALAB Products, Geesthacht

GKSS, Geesthacht

HannStar Color, Taipeh, Taiwan

Heidelberger Druckmaschinen, Kiel

Heidenhain, Traunreut

HL Planartechnik GmbH, Dortmund

H. C. Starck, Leverkusen

Hella KG, Lippstadt

IBM- Speichersysteme GmbH, Mainz

IC-Haus GmbH, Bodenheim

ICT, München

IDB Technologies, North Somerset, UK

IMS, Wien, Austria

Incoatec, Geesthacht

Infineon Technologies GmbH, München

ISiltec GmbH, Erlangen

Jiangmen J. J. J. Battery Co., Jiangmen, China

JLS Designs, Somerset, UK

Jungheinrich AG, Norderstedt

Kapsch, Wien, Austria

Kember Associates, Bristol, United Kingdom

KID Systeme, Buxtehude

Kolbenschmidt Pierburg AG, Neuss

Kugler GmbH, Salem

Kuhnke GmbH, Malente

K & W Asia, Hong Kong, China

LEICA Microsystems, Jena

Litef, Freiburg

Mair Elektronik GmbH, Neufahrn

MED – EL, Innsbruck, Austria

Miele & Cie., Gütersloh

Motorola GmbH, Flensburg

mrt – Micro-Resist-Technology, Berlin

m-u-t GmbH, Wedel

Nanophotonics AG, Mainz

Nokia Research Center, Nokia Group, Helsinki, Finland

November AG, Erlangen

Novo Nordisk A/S (NOVO), Bagsvaerd, Denmark

NU-Tech GmbH, Neumünster

OK Media Disc Service GmbH & Co.KG, Nortorf

Orga Kartensysteme GmbH, Flintbeck

Oticon, A/S, Hellerup, Denmark

PAV Card GmbH, Lütjensee

Pohlmann & Partner GmbH, Quickborn

Perkin Elmer Optoelectronics, Wiesbaden

Philips Semiconductors, Gratkorn

Philips Semiconductors, Hamburg

Qinetiq, Malvern, UK

Qinetiq Ltd, Worcestershire, UK

Raytheon Anschütz GmbH, Kiel

Robert Bosch GmbH, Salzgitter

RongHua Group New Materials, Xi´an, China

SAES Getters S.p.A., Lainate/Milan, Italy

Scana Holography Company GmbH, Schenefeld

Scanbec Oy, Oulu, Finland

Scanbec GmbH, Halle

Schott, Landshut

Seibersdorf Research, Seibersdorf, Austria

SEF Roboter GmbH, Scharnebek

SensLab GmbH, Leipzig

SensoNor, Horten, Norway

Sentech Instruments GmbH, Berlin

Siemens AG, Zentrale Technik, Erlangen

Siemens AG, München

Siemens Mobile, München

Siemens VDO Automotive AG, Schwalbach

SMA Regelsysteme GmbH, Niestetal

SMI GmbH, Itzehoe

Smith Meter GmbH, Ellerbeck

Solid Energy GmbH, Itzehoe

ST Microelectronics, Mailand, Italy

Still GmbH, Hamburg

SÜSS Microtec AG, Garching

TCL Hyperpower Batteries, Huizhou, China

Technolas, München

Technovision GmbH, Feldkirchen

Telefonica, Madrid, Spanien

Tesa AG, Hamburg

Thales Avionics, Valence, France

Thales, Paris, France

Trioptics GmbH, Wedel

Tronic´s, Grenoble, France

VDMA Fachgemeinschaft Fluidtechnik, Frankfurt

Vishay, Holon, Israel

Vishay Semiconductor GmbH, Itzehoe

Wabco Fahrzeugbremsen, Hannover

Peter Wolters CMP Systeme GmbH, Rendsburg

Woowon Technology, Korea

YAGEO EUROPE GmbH, Elmshorn

Innovation Catalogue

ISIT offers its customers various products and services already developed for market introduction. The following table presents a summary of the essential products and services. Beyond that the utilisation of patents and licences is included in the service.

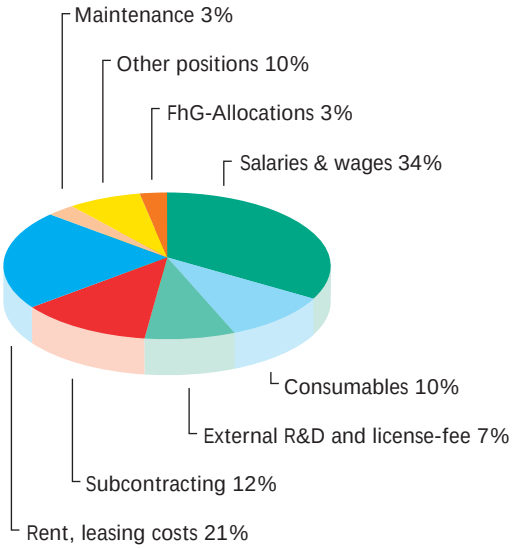
Product / Service	Market	Contact Person
Testing of semiconductor manufacturing equipment	Semiconductor equipment manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
Chemical-mechanical polishing (CMP), planarization	Semiconductor device manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
Wafer polishing, single and double side	Si substrates for device manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
IC processes CMOS, PowerMOS, IGBTs	Semiconductor industry IC-users	Detlef Friedrich + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Single processes and process module development	Semiconductor industry semiconductor equipment manufacturers	Detlef Friedrich + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Customer specific processing	Semiconductor industry semiconductor equipment manufacturers	Detlef Friedrich + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Microsystem Products	Electronic industry	Dr. Ralf Dudde + 49 (0) 4821/17-4212 ralf.dudde@isit.fraunhofer.de
Plasma source development	Semiconductor equipment manufacturers	Christoph Huth +49 (0) 4821/17-4628 christoph.huth@isit.fraunhofer.de
Plasma diagnostics	Semiconductor equipment manufacturers	Joachim Janes + 49 (0) 4821/17-4509 joachim.janes@isit.fraunhofer.de
Etching and deposition process control	Semiconductor industry	Joachim Janes joachim.janes@isit.fraunhofer.de
Ion projection, lithography open stencil mask technology and resist processes	Semiconductor industry	Dr. Wilhelm Brünger + 49 (0) 4821/17-4228 wilhelm.bruenger@isit.fraunhofer.de
E-beam circuit testing and e-beam induced deposition	Semiconductor industry	Dr. Wilhelm Brünger + 49 (0) 4821/17-4228 wilhelm.bruenger@isit.fraunhofer.de
Inertial sensors	Motorvehicle technology, navigation systems, measurements	Dr. Bernd Wagner + 49 (0) 4821/17-4223 bernd.wagner@isit.fraunhofer.de
Design for commercial MST processes	Micro sensors and actuators	Dr. Bernd Wagner + 49 (0) 4821/17-4223 bernd.wagner@isit.fraunhofer.de
Microvalves for gases and liquids	Analytic, medical technology measurement	Hans Joachim Quenzer + 49 (0) 4821/17-4524 hans-joachim.quenzer@isit.fraunhofer.de
Microoptical scanner	Biomedical technology, optical measurement industry, telecommunication	Ulrich Hofmann + 49 (0) 4821/17-4529 ulrich.hofmann@isit.fraunhofer.de
Microoptical components	Optical measurement,	Dr. Klaus Reimer + 49 (0) 4821/17-4506 klaus.reimer@isit.fraunhofer.de

Product / Service	Market	Contact Person
Mastering and replication of micro structures in plastic	Microoptics, microfluidics	Dr. Klaus Reimer + 49 (0) 4821/17-4506 klaus.reimer@isit.fraunhofer.de
Design and test of analogue and mixed-signal ASICs	Measurement, automatic control industry	Jörg Eichholz + 49 (0) 4821/17-4537 joerg.eichholz@isit.fraunhofer.de
Design Kits	MST foundries	Jörg Eichholz + 49 (0) 4821/17-4537 joerg.eichholz@isit.fraunhofer.de
RF-MEMS	Telecommunication	Dr. Bernd Wagner + 49 (0) 4821/17-4223 bernd.wagner@isit.fraunhofer.de
MST Design and behavioural modelling	Measurement, automatic control industry	Jörg Eichholz + 49 (0) 4821/17-4537 joerg.eichholz@isit.fraunhofer.de
Electrodeposition of microstructures	Surface micromachining	Martin Witt + 49 (0) 4821/17-4541 martin.witt@isit.fraunhofer.de
Digital micromirror devices	Communication technology	Dr. Klaus Reimer + 49 (0) 4821/17-4506 klaus.reimer@isit.fraunhofer.de
Electrical biochip technology (proteins, nucleic acids, haptens)	Biotechnology, related electronics medical diagnostics, environmental analysis, Si-Chipprocessing, packaging, chip loading	Dr. Rainer Hintsche + 49 (0) 4821/17-4221 rainer.hintsche@isit.fraunhofer.de
Secondary lithium batteries based on solid state ionic conductors	Mobile electronic equipment, medical applications, automotive, smart cards, labels, tags	Dr. Peter Gulde +49 (0) 4821/17-4606 peter.gulde@isit.fraunhofer.de
Battery test service, electrical parameters, climate impact, reliability, quality	Mobile electronic equipment medical applications, automotive, smart cards, labels, tags	Dr. Peter Gulde +49 (0) 4821/17-4606 peter.gulde@isit.fraunhofer.de
Quality and reliability of electronic assemblies (http://www.isit.fhg.de)	Microelectronic and power electronic industry	Karin Pape + 49 (0) 4821/17-4229 karin.pape@isit.fraunhofer.de
Material and damage analysis	Microelectronic and power electronic industry	Dr. Thomas Ahrens + 49 (0) 4821/17-4605 thomas.ahrens@isit.fraunhofer.de
Thermal measurement and simulation	Microelectronic and power electronic industry	Dr. M. H. Poech + 49 (0) 4821/17-4607 max.poech@isit.fraunhofer.de
Packaging for microsystems, sensors, multichip modules (http://www.isit.fhg.de)	Microelectronic, sensoric and medical industry	Karin Pape + 49 (0) 4821/17-4229 karin.pape@isit.fraunhofer.de
Wafer level and ultra thin Si packaging	Microelectronic, sensoric and medical industry	Wolfgang Reinert + 49 (0) 4821/17-4617 wolfgang.reinert@isit.fraunhofer.de
Direct chip attach using flip chip techniques	Microelectronic, sensoric and medical industry	Wolfgang Reinert + 49 (0) 4821/17-4617 wolfgang.reinert@isit.fraunhofer.de
Flow sensors	Automotive, fuel cells	Dr. Peter Lange +49 (0) 4821/17-4118 peter.lange@isit.fraunhofer.de

Representative Figures

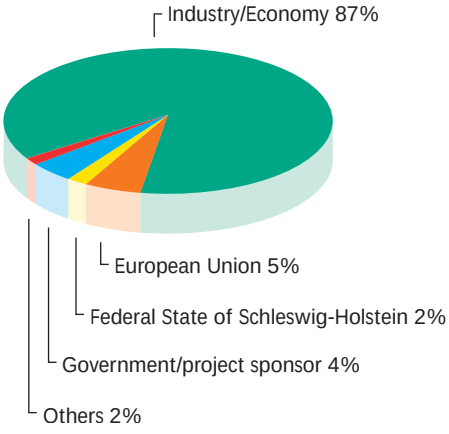
Expenditure

In 2003 the operating expenditure of Fraunhofer ISIT amounted to kEuro 18.296. Salaries and wages were kEuro 6.160 consumables and other costs were kEuro 12.137.



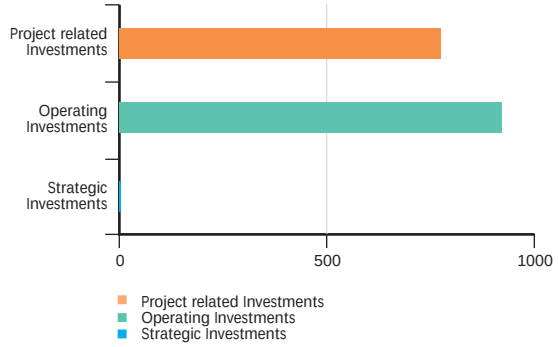
Income

The budget was financed by proceeds of projects of industry/industrial federations/small and medium sized companies amounting to kEuro 14.000 of government/project sponsors/federal states amounting to kEuro 1.216 and of European Union/others amounting to kEuro 831.



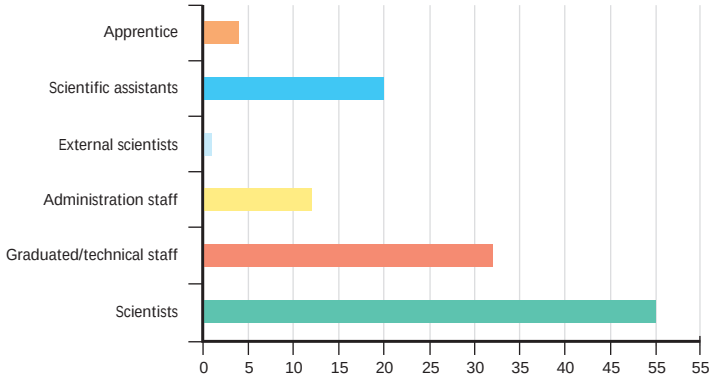
Capital Investment

In 2003 the institutional budget of capital investment was kEuro 1.699. The operating investment was kEuro 925 and project related investments were amounted to kEuro 775.



Staff Developement

In 2003, on annnual average the staff constisted of 94 employees. 50 were employed as scientific personnel, 32 as graduated/technical personnel and 12 worked within organisation and administration. 1 scientist, 20 scientific assistents and 4 apprentice supported the staff as external assistance.



The Fraunhofer-Gesellschaft

The Fraunhofer-Gesellschaft undertakes applied research of direct utility to private and public enterprise and of wide benefit to society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration. The organization also accepts commissions and funding from German federal ministries and government departments to participate in future oriented research projects with the aim of finding innovative solutions to issues concerning the industrial economy and society in general.

By developing technological innovations and novel systems solutions for their customers, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. Through their work, they aim to promote the successful economic development of our industrial society, with particular regard for social welfare and environmental compatibility. As an employer, the Fraunhofer-Gesellschaft offers a platform that enables its staff to develop the professional and personal skills that will allow them to take up positions of responsibility within their institute, in other scientific domains, in industry and in society.

At present, the Fraunhofer-Gesellschaft maintains roughly 80 research units, including 58 Fraunhofer Institutes, at over 40 different locations in Germany. A staff of 12,700, predominantly qualified scientists and engineers, work with an annual research budget of over 1 billion euros. Of this sum, more than € 900 million is generated through contract research. Roughly two thirds of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. The remaining one third is contributed by the German federal and Länder governments, as a means of enabling the institutes to pursue more fundamental research in areas that are likely to become relevant to industry and society in five or ten years' time.

Affiliated research centers and representative offices in Europe, the USA and Asia provide contact with the regions of greatest importance to future scientific progress and economic development.

The Fraunhofer-Gesellschaft was founded in 1949 and is a recognized non-profit organization. Its members include well-known companies and private patrons who help to shape the Fraunhofer-Gesellschaft's research policy and strategic development. The organization takes its name from Joseph von Fraunhofer (1787-1826), the illustrious Munich researcher, inventor and entrepreneur.

Locations of the Research Establishment

Representative Results of Work

Representative Results of Work
IC-Technology

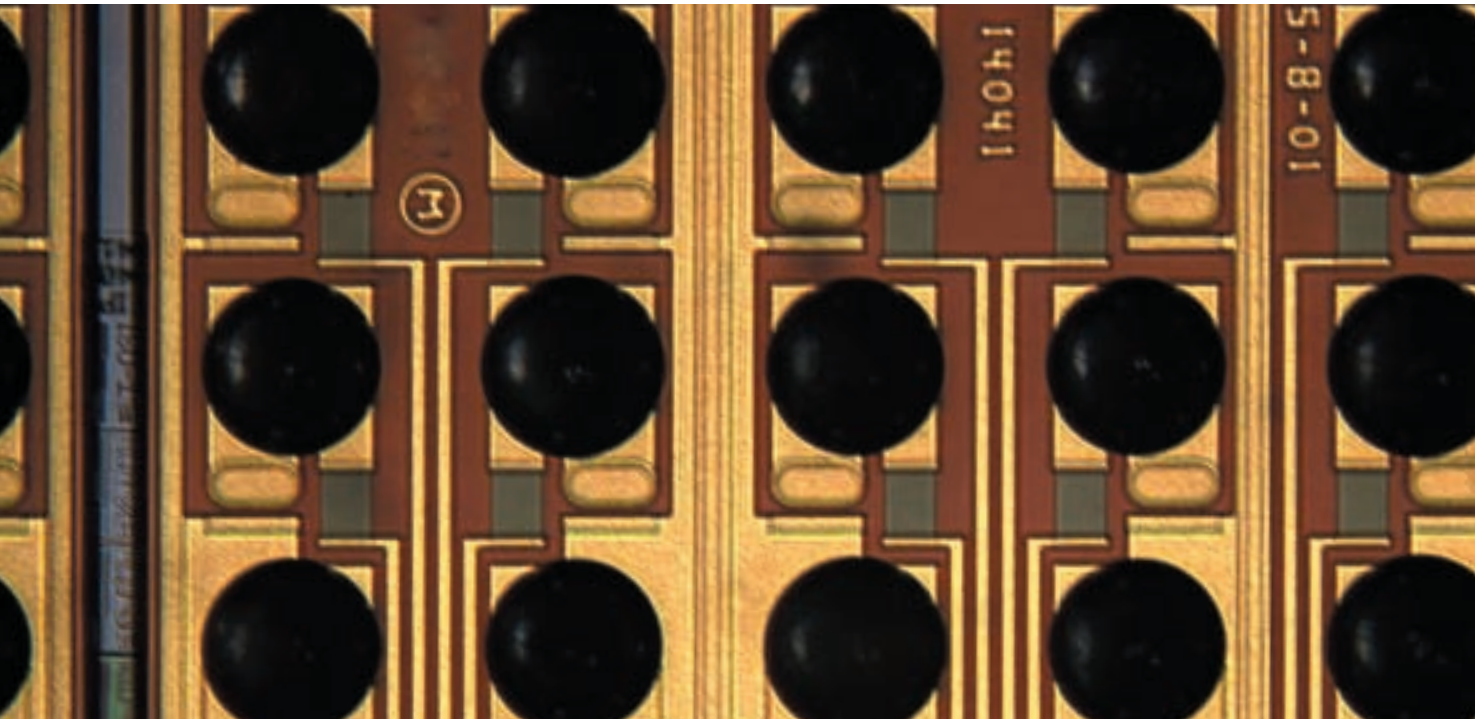
Wafer Level – Chip Size Packaging (WL-CSP)

With the beginning of the IC-Technology in the early 60‘s wirebonding was the predominant technique for chip interconnection used for the packaging of semiconductor devices. Over the decades this technique became the mainstream technology following most of the demands in interconnection density.

However, today leading edge ASICs and microprocessors have pin counts exceeding 2000. Their packaging requirements are currently covered by Flip-Chip technologies in ball grid array (BGA) packages, only.

Along with the need for increased pin counts for high interconnect densities, a growing interest was arising in the last years for increased packaging densities which can be fulfilled by WL-CSP approach. This need was especially driven by hand held and portable electronic devices, e.g. mobile phones, cameras, medical devices, laptops, etc.

It is the most important requirement that the CSP should have the same size as the die itself. This is illustrated in figure 1 showing a typical CSP with 25 solder balls for mobile phone application.



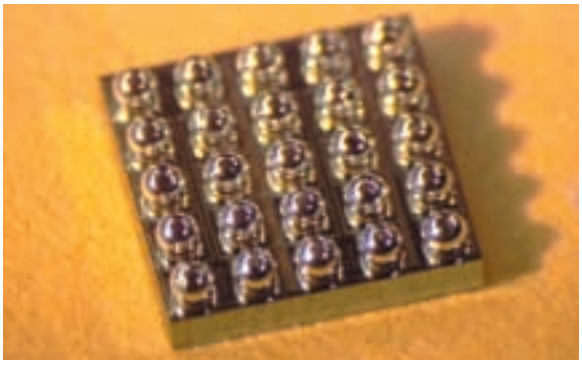


Figure 1:
Example for
a) WL-CSP with solder balls placed on a wafer.

b) CSP with 25 solder balls per chip (ball diameter 300 µm, pitch 500 µm). The CSP is equal to die size.

WL-CSP is a packaging technology on wafer level for the placement of solder balls on specially prepared pad openings in chip area arrays across the entire wafer.

The main features which makes WL-CSP attractive for increasing number of applications are:

- Cost competitive with low cost packaging technologies
- Smallest possible board space needed
- Compatible with exsisting SMT (Surface Mount Technology) assembly
- Reworkable in PCB (Printed Circuit Board) assembly
- Compatible with exsisting IC design and independent of die stepping and shrinks
- Reliability proven for application
- No moisture sensitivity by BCB passivation

The WL-CSP technology is based on an Under Bump Metallisation (UBM) on top of the chip passivation. UBM is consisting out of Al/NiV/Cu stak. NiV is needed as a diffusion barrier against Sn diffusion and Cu as a wetting layer to allow the solder ball to be connected to UBM after a reflow process. After structuring of the UBM a special passivation layer is deposited for definition of the openings for flux print and the ball placement. As shown in figure 2 the UBM layer can also be used as a redistribution layer for transformation of the chip perimeter leaded bonding pads into an area array of pads suitable for WL-CSP technology.

For a 6 inch wafer with a solder ball pitch of 500 µm the typical number of solder balls amounts to approx. 50 000 balls per wafer. The real geometries are illustrated in figure 3 showing a SEM cross section of a lead free solder ball after reflow. The intermetalic phase formation between solder ball and UBM can be clearly seen. There is no lateral encroachment of the solder observed by excellent sealing of the BCB passivation layer (Benzocyclobutene) along the periphery of the solder ball.

Since most of the standard packaging technologies have been gone to Far East assembly houses over the years, there is a lack of even advanced commercial packging activities in Europe, althought the market perspective is excellent. This was the reason that a collaboration between ISIT and SMI (Philips) was started in 2002 to build up a production for WL-CSP. By the end of 2003 production processes for lead content and lead free solder balls were qualified.

Since beginning of 2004 the production ramp up is in progress with an envisaged capacity of 100 000 wafers per year. At this time SMI-ISIT are offering the only commercial WL-CSP process for high volume production within Europe.

Figure 2:
Principle schematic of WL-CSP technology.

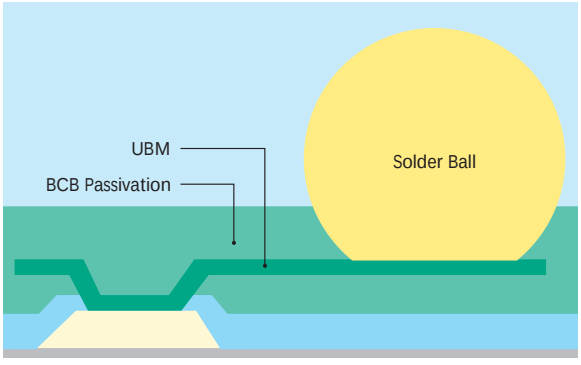
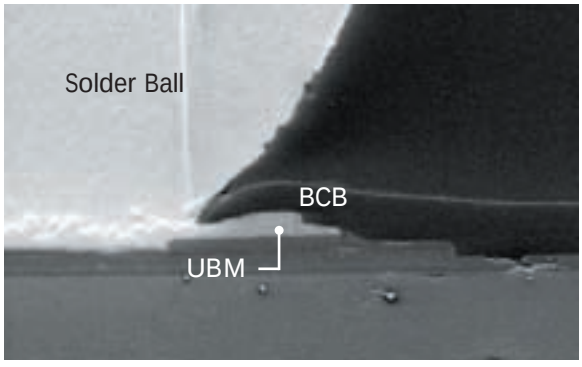


Figure 3:
SEM cross section of a lead free solder ball in a WL-CSP technology.



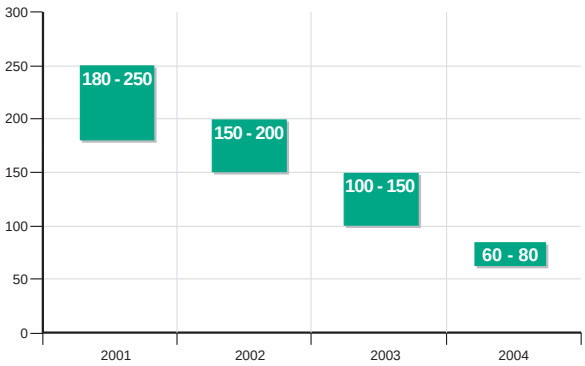
Representative Results of Work
IC-Technology

Ultra Thin Silicon Substrates for Power Devices

In contrast to lateral power devices used in BCD-MOS Smart Power ICs (combined Bipolar-CMOS-DMOS Technology) most of the discrete power transistors for medium and high power ranges are vertical devices. In this case the current flow is directed from the wafer front side to the back side. Here, the wafer substrate has important impact on the device performance in terms of thermal- and electrical resistance. Therefore, ultra thin wafer substrates are mandatory for the reduction of the conduction losses and improvement of the heat transfer. For this purpose the wafer thickness has been reduced over the years stepwise and will be further continued down to the physical limits. An illustration of the roadmap for wafer thinning of power devices is shown in figure 1.

Depending on the type of the device and the voltage range the optimal wafer thickness can vary, due to device physical considerations. For example, 600 V IGBTs which are used for power control in e.g. "white goods" the wafer thickness can be reduced down to 70 µm – 80 µm. An illustration of the geometrical dimensions for a 600 V Trench-IGBT is shown in figure 2. Ultra thin wafer technology is a pre-condition for high performance power devices in terms of low power loss and high temperature application.

Figure 1:
Roadmap for the wafer thickness of power devices.



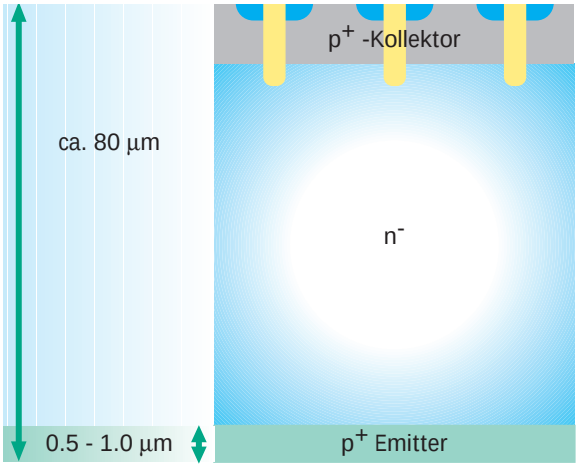


Figure 2:
Geometrical dimensions of a NPT-Trench-IGBT.

Within the entire processing chain for power device fabrication several process steps have to be carried out with thinned wafer. Suitable process and handling sequences are required. Therefore, the development of ultra thin wafer technology is primarily focused on special handling techniques for wafers with substrate thicknesses below 100 µm.

To realise the concept of thin wafer processing different attemps have been proven. For the decision of a suitable concept the following criterea have to be fulfilled: mechanical stability for wafer handling, chemical stability for standard etch and cleaning processes, capability for processing under vacuum and thermal stability up to approx. 150° C.

For this purpose, the ISIT concept is based on a supporting substrate technique, taking into account the above mentioned requirements suitable for all back side processes e.g. grinding, implantation and metallisation. After finishing the front side processes, the power device wafer is temporarily glued up side down on a supporting substrate by use of a double sided glueing tape in between. The principle of this technique is illustrated in figure 3. With this 3 fold stack (device wafer, tape, supporting substrate), the device wafer is grinded to the intended

thickness, which is actually 100 µm in our case. First results showed that standard substrates with a wafer edge profile according to the SEMI standard have very fragile edges after the thinning process. This is leading to edge micro cracks with a high propability of wafer breakage. To overcome this problem special asymmetrical edge profiles have been introduced. On that condition, the sharp wafer rim is avoided resulting in a mechanically more stable wafer edge.

Moreover, it is important to remark, that several back side processes are performed under vacuum e.g. emitter implantation and metallisation. Even smallest inclusions of air bubbles under the foil can lead to severe mechanical damage of the thin device wafer, due to the local pressure difference of 1 bar. To avoid air inclusions under the tape the optimisation of the taping and bonding process is of special importance.

First results have been obtained with the supporting substrate technique for back side processing of 600 V Trench-IGBTs. In this case, all back side processes were carried out with 100 µm thin IGBT wafers using this wafer carrier technique, except the final thermal anneal at 475° C. This annealing process was being done after tape release in a specially designed quarz carrier for furnace processing.

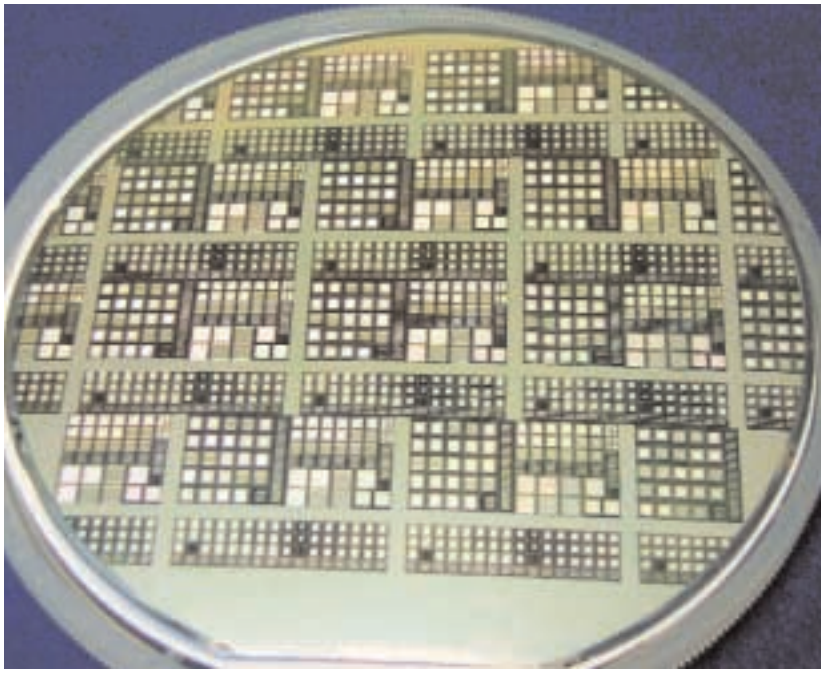
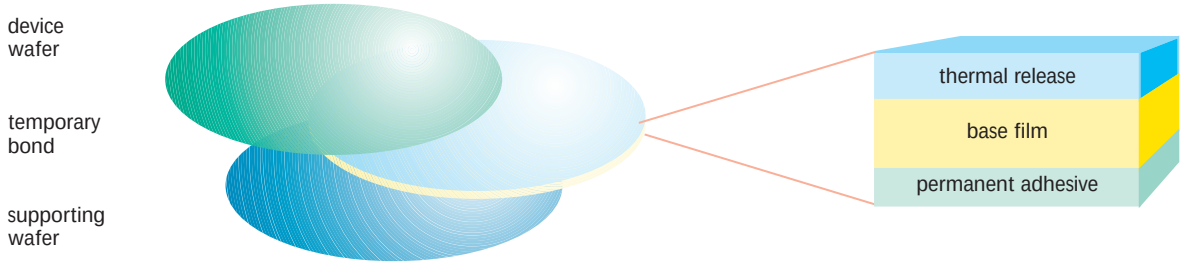


Figure 4:
Flexible 100 µm thin IGBT wafer.

The thin wafers were released from the tape and carrier substrate by hot plate heating at a temperature of 170° C for 30 sec. No residues from the tape have been observed on the wafer front side. The residual wafer bow was in the range of 500 µm. Nevertheless, the IGBT wafer shown in figure 4 was electrically characterised by wafer probing and subsequently mounted on a tape for dicing.

In terms of IGBT performance the saturation voltage V_{CEsat}, which is a measure for the conduction losses, is reduced by 40 % compared to IGBTs with a substrate thickness of 200 µm.

Figure 3:
Schematic of temporary bonding of two wafers with a double sided glueing tape in between.



Modification of Oxide-CMP Slurries for Future Demands

Due to ever decreasing pattern dimensions of advanced ICs and emerging demands in the planarisation of surfaces e.g. for the fabrication of MEMS devices, the polishing slurries for chemical-mechanical polishing (CMP) have to be adapted appropriately. Two kinds of slurries are presently employed in CMP processes for the planarization of inter-lever dielectrics:

- colloidal-silica based slurries, consisting of spherical abrasive particles, show comparatively lower polishing rates, but lead to very smooth surfaces
- fumed-silica based slurries, consisting of flake-like abrasive particles, which are agglomerates of smaller primary particles, show higher removal rates with the drawback of rougher surfaces

In order to achieve smoother surfaces with fumed-silica slurries, the abrasive particles have to be modified from the flake-like to a more spherical shape. In a series of experiments, dispersed AEROSIL® particles from Degussa, one of the market leaders in fumed-silica powders, have been treated in a wet-jet mill with extremely high shear energies.

The principle operation of a wet-jet mill is depicted in figure 1. Pressurised dispersed fumed silica (750 – 2500 bar) is divided into two flows and expands into a reaction chamber via two diamond nozzles. The two slurry jets are directed onto each other from opposite directions and collide. The basic idea is that the high shear forces strip protruding branches of the fumed-silica agglomerates and change the shape of the particles.

Subsequent polishing tests with the modified dispersions should reveal changes in the polishing behaviour in comparison to untreated slurries. Various AEROSIL® dispersions and a commercial fumed-silica product have been wet-jet milled with different shear forces and the obtained polishing results have been compared with untreated fumed-silica dispersions and additionally with a commercial colloidal-silica product.

The results can be summarised as follows:

- The typical behaviour of colloidal-silica slurries to show a strictly linear dependence of removal rate on the product of down force and platen speed (Preston's law) has not been observed even with very high milling energies. The typical sub-linear dependence of fumed-silica slurries did not alter.
- The mean removal rates of treated dispersions only slightly decreased, so that only minor modifications of the morphology of the particles can be assumed.
- The surface roughness results after CMP of R_a 0,15 nm for colloidal silica have not been achieved. All milling treatments left the typical roughness values for fumed silica of R_a 0,25 – 0,30 nm nearly unchanged.
- However, the post-CMP cleaning behaviour

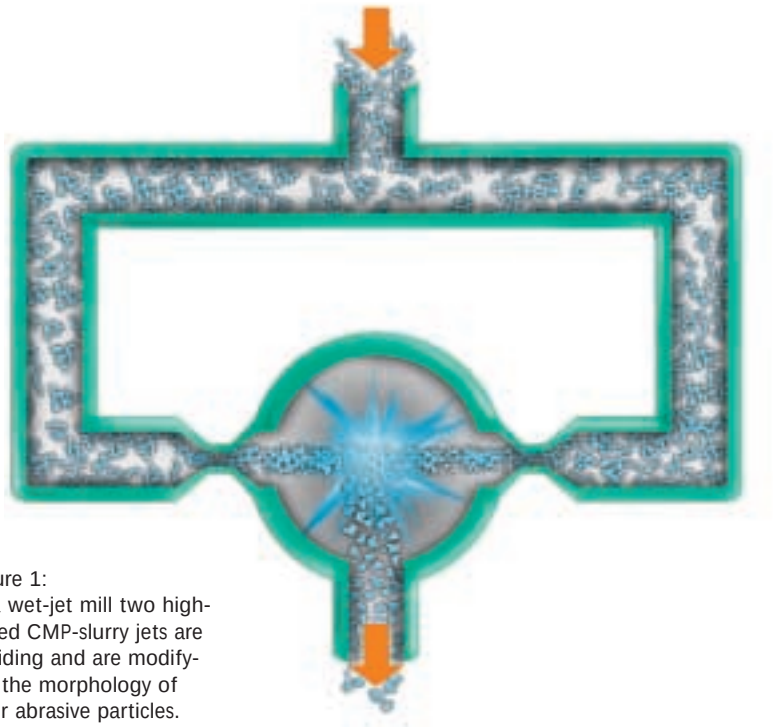


Figure 1:
In a wet-jet mill two high-speed CMP-slurry jets are colliding and are modifying the morphology of their abrasive particles.

of wafers polished with differently treated or untreated samples changed. It could be observed that the surface particle density left after cleaning increased dramatically with milling cycles and milling energies. Only untreated colloidal or fumed silica slurries showed small acceptable numbers.
This observation indicates a modification of the abrasives to either smaller agglomerates or to an increase in sticking points of the particles on the surface.

In order to get a better understanding of the wet-jet milling process, the project partner Degussa performed high shear rate viscosity measurements in a capillary viscometer with shear rates comparable to wet-jet milling. Some results are summarised in figure 2. For all dispersions the viscosity is nearly constant for shear rates below 100 000 s^{-1}. A typical colloidal silica shows a slow increase in viscosity above that shear-rate value, while fumed products (Fumed and AE90 R/S) showed a steep increase in viscosity above ~ 200 000 s^{-1}. This behaviour can be intensified by a wet-jet milling with a milling energy of 750 bar.

However, a treatment with even higher milling energies of 1500 or 2500 bar alters the viscosity behaviour and leads to results comparable with colloidal silica, but shifted to higher shear rates. From these results, it can be concluded that wet-jet milling is modifying fumed-silica slurries, but that the influence on the CMP process in the investigated polishing parameter range seems to be negligible.

What are the consequences of these findings?

All experiments have been performed on blanket wafers. Under an assumption of a slurry film thickness of 10 µm and a relative speed of 1 m/s between pad and wafer, the typical shear rate amounts to 100 000 s^{-1}. This is below the shear rates where the viscosity changes drastically and might explain, why the removal behaviour of the slurries has not changed.

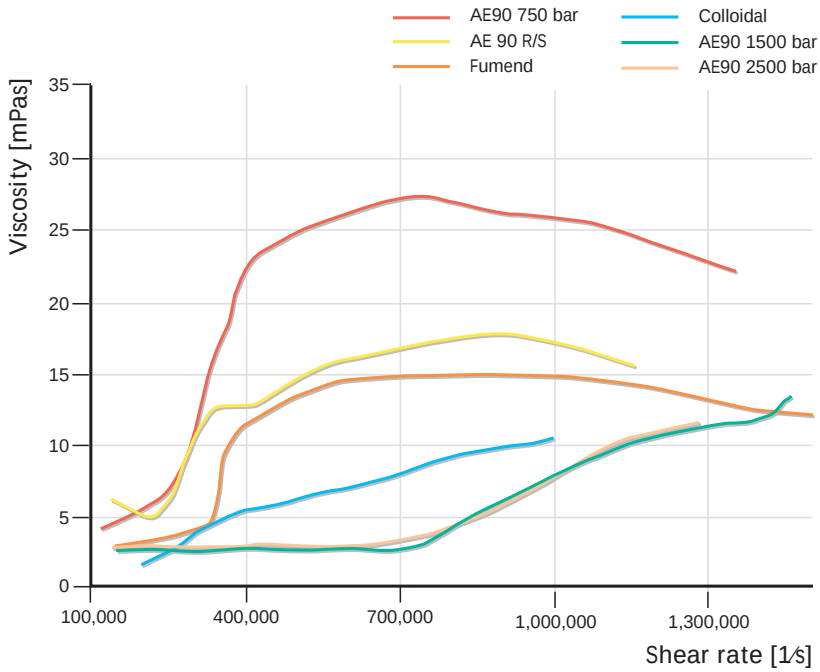


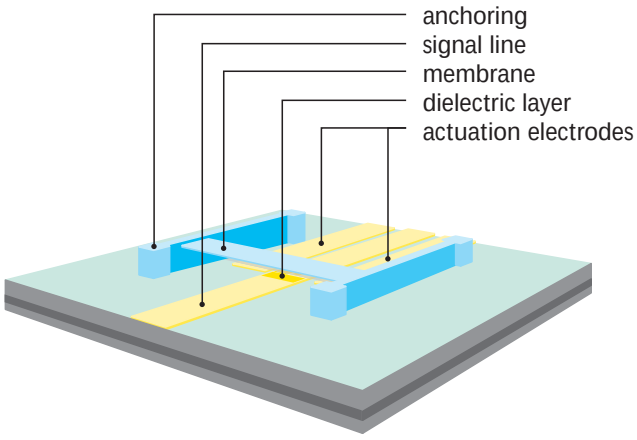
Figure 2:
High shear-rate viscosity of untreated and wet-jet milled fumed-silica slurries. The difference between commercially available fumed and colloidal silica is distinct (dotted lines). AE90 is an untreated fumed-silica test dispersion. Treatment of the test dispersion with very high milling energies changes the viscosity behaviour from fumed to colloidal-like. The measurements have been performed by the project partner Degussa.

The condition is different for structured wafers where the distance between pad and wafer locally might be smaller. If the distance between pad asperities and "up" structures decreases to 1 µm, local shear rates of 1 000 000 s^{-1} might occur. From lubrication theory it is known that the coefficient of friction and therewith the removal rate depends on the viscosity.
In shear rate regimes with higher viscosity, the local material removal might be different from the result with a blanket wafer. By taking these considerations into account, it is planned to perform intelligent polishing experiments in order to achieve a better explanation of local CMP effects like dishing or erosion.

RF MEMS Switches for Wireless Communication

MEMS based switching and actuating devices have emerged as a promising alternative to solid state GaAs or Si based devices in microwave applications. Compared to PIN diodes or FET-based switches RF MEMS devices are characterized by very low losses, a very high isolation, a very low power consumption and an excellent linearity. Within the European IST-project MELODICT ISIT has started the development of micromachined variable capacitors and varactors to be used in mobile applications (frequency range 0.8...3 GHz).
Figure 1 shows a schematical view of a capacitive RF MEMS switch. The suspended movable structure of the device consists of Ni only.
The metallic signal line beneath is covered with a dielectric layer below the membrane.
In the inital state the gap between signal line and membrane is in the range of 2 to 3 µm. Usually the off-capacitance of such a switch is very low and an RF signal on the signal line can pass without disturbance. In this state the switch is open. By applying a voltage between the membrane and the signal line (or additional actuation electrodes) the membrane can be pulled downward. If the capacitance change is high enough the RF signal is reflected nearly completely. In this state the switch is closed.

Figure 1:
Schematic view of a parallel-plate switch (varactor) with a metallic membrane suspended by a metallic anchoring above a metallic sinal line.



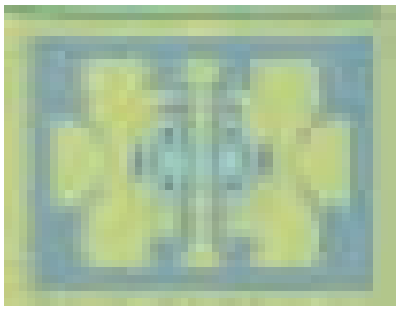


Figure 2:
Photo of a varactor with actuation electrodes embedded in the ground area, two stiffening bars on top of the membrane and a gold sealing ring for solder bonding of a ceramic cap with vertical feedthroughs.
Chip size: 1,7 mm x 2,2 mm.

Figure 2 shows a completed device. The spring-type anchoring facilitates the compensation of thermally induced drift effects caused by the difference in thermal expansion between the metallic structure and the silicon substrate.
The two actuation electrodes embedded in the ground area of the coplanar wave guide allow to switch the varactor independently from the voltages applied to the signal line. Figures 3 and 4 present the RF behaviour for a switch shown in figure 2. At 2 GHz the transmission in the off-state (switch actuated) is around –0.2 dB and the reflection around –29 dB.

It has been found that the varactors developed at ISIT survive heat treatments at up to 450°C without degradation. This allow the application of standard packaging techniques on wafer level. A first step will be the solder bonding of a 1"x 1" ceramic cap panel with vertical feedthroughs, see figure 5.

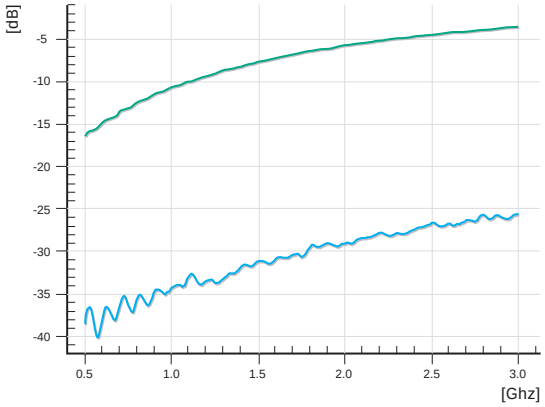


Figure 3:
Reflection in the on-state (green) and the off-state (blue).

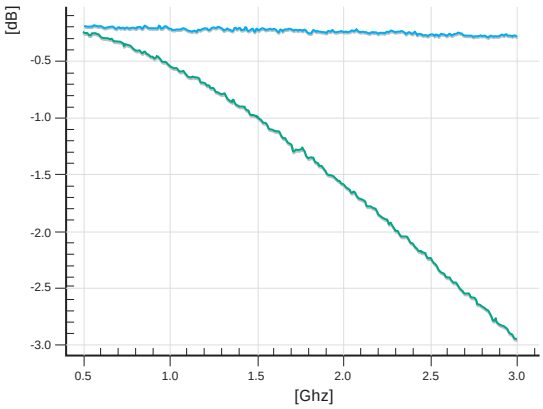


Figure 4:
Insertion loss in the on-state (green) and the off-state (blue).

Wide-range tuning varactors have been realized extending the fabrication technology for parallel-plate devices by additional fixed electrodes above the membrane. Figure 6 and figure 7 show a device with a membrane parallel to the signal line. The touch down area of the membrane can be actively tuned by independently applying voltages to the signal line and to the upper electrodes. The characterisation is still in progress.

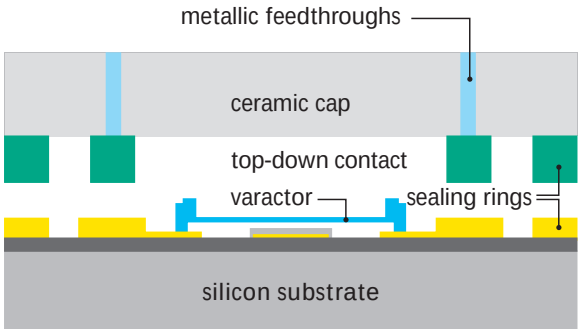


Figure 5:
Schematic cross-sectional view of a wafer-level packaging using ceramic caps with vertical metallic feed-throughs.

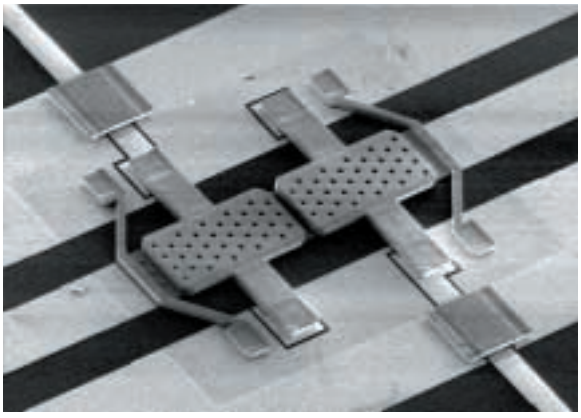


Figure 6:
SEM foto of a tunable capacitor with fixed electrodes above the membrane.

Figure 7:
Detail of the anchoring with 15 µm thick Ni beams.

Development of a Bistable Thermomechanical Micro Relay

(Project: MELODICT funded by the EC,
project number: IST-1999-10945)

Beside the electrostatic drives, thermomechanical driving principles have been realised very early in MEMS [Riethmüller et al. "Micromechanical silicon actuators based on thermal expansion effects" Transducer 1987, pp 834 – 837, June 87] Thermally driven micro actuators have been realised for the construction of micro devices which requires a maximum of force. Despite of the big advantages of thermomechanical drives, the specific restrictions of this kind of driving principles inhibits very often their use. A bistable approach which includes thermal drives would overcome the most important drawback for the use of thermomechanical drives. In this concept only during the short switching period electrical power is consumed. In our approach the bistable behaviour is achieved by using an additional actuator which clamps the switching device in the on-state. The use of two actuators in one µ-relay offers the opportunity to combine both, large stroke length and high contact forces.
The arrangement of the two actuators allows the construction of a µ-relay that can be fixed in two stable states without further power consumption. Therefore the µ-relay requires only electrical power during the switching cycle.

Based on this concept a so called configuration switch was developed. The term configuration switch describes a low speed, low loss switch with low power consumption and moderate life time requirements (< 1 million cycles). Typical applications for this kind of micro switch are end user defined re-configurations of an electronic component like a telephone network or a complete mobile phone.

The complete relay consists of two thermally driven actuators, the first actuator moves in-plane over the surface while the second actuator moves perpendicular to the surface up and down. These actuators are arranged in such way, that the lateral actuator can be moved right under the activated vertical actuator and can be clamped by the vertical actuator when this actuator moves downwards. The electrical contacts are located beside the vertical actuator and can be closed by the clamped lateral actuator (figure 1).

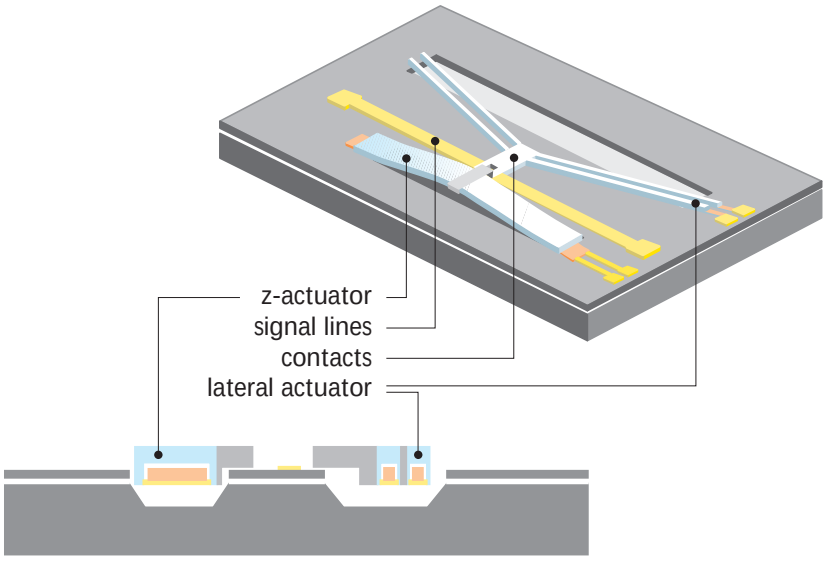


Figure 1:
3D-view of the µ-relay. The complete µ-relay consists of two actuators, the first actuator moves laterally over the substrate surface, the second actuator moves vertically up and down. Both actuators are thermally driven by a heater located under the nickel structures. The µ-relay here is shown in the on-state.

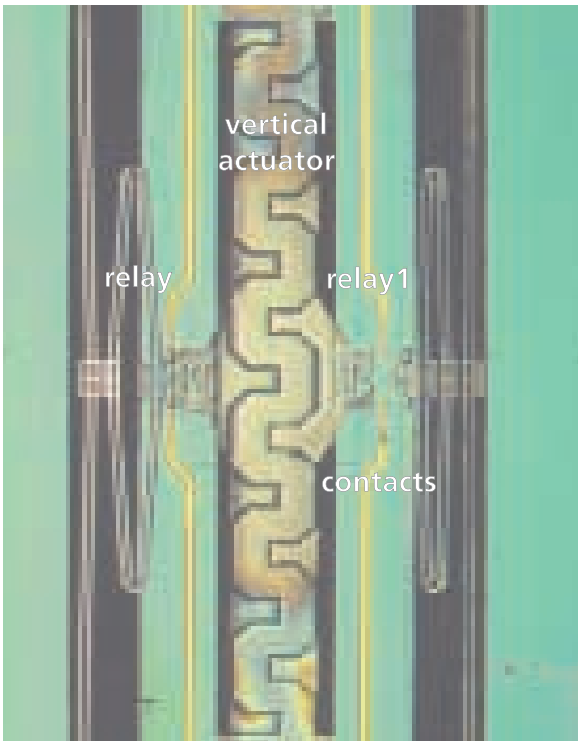


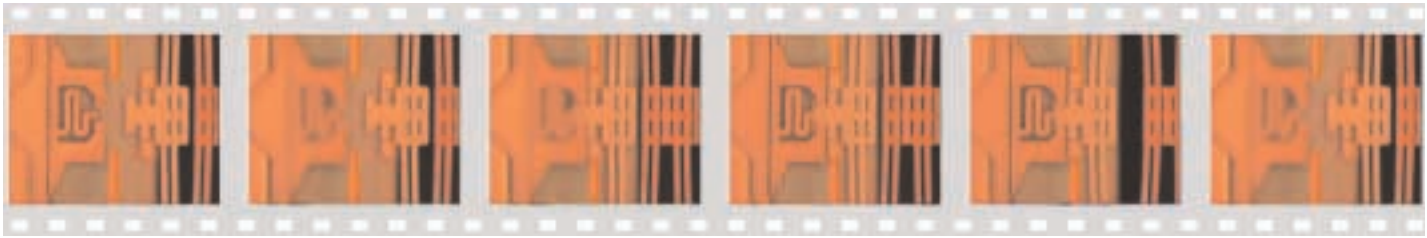
Figure 2:
Picture of a new bistable micro relay. Beside the common vertical actuator the two lateral actuators allow the switching of two separated pairs of signal lines. In this situation the left contacts are closed while the right contacts are still open. The thermal drives are the two pairs of small beams to the left and to the right side of the vertical actuator. Next to the drives the folded springs are located which reduces the restoring forces on the contact bridge of the micro relay.

The contact forces generated by the vertical actuator per contact are in the range of 10 mN. The required chip area for realising both micro actuators is about 0.5 mm x 2.5 mm (figure 2).

For switching the µ-relay into the on-state, both actuators will be activated (figure 3.1). Therefore the central plate of the lateral actuator will be moved under the central plate of the vertical actuator (figure 3.3). For closing the electrical contacts the vertical actuator is switched off and moves downwards to the substrate and clamps the lateral actuator onto the contacts. Finally the lateral actuator can be also switched off (figure 3.5). For switching the relay into the off state both actuators are first activated but then the lateral actuator has to be switched off first. The movement of the lateral actuator into the initial position also opens the electrical contacts (figure 3.6).

For switching the vertical actuator into the on-state a voltage of 3.5 V is necessary, while the lateral actuator requires a voltage between 7.5 and 8.0 V (depending on the design). For switching into the off-state only the vertical actuator must be activated (U =2.5 V). The lateral actuator moves back only driven by the restoring force of the spring between the contact bridge and the thermal drives of the micro relay.

Figure 3:
Picture sequence illustrating the working principle of the micro relay:



1) before activating the actuators: off state.

2) activating the vertical actuator: U = 3.5 V.

3) activating the lateral actuator: U = 7.7 V.

4) switching off the vertical actuator.

5): switching off the lateral actuator, bending of the spring between contact bridge and drives on state.

6) switching on of the vertical actuator, U = 2.5 V, the lateral actuator moves back, driven by the restoring force of the spring.

In the figures 4 and 5 the deflection measurements of the vertical and lateral actuators of the relay are summarised. The measured values agree very good with the calculated behaviour of the different actuators. For the dynamic characterisation two different set ups were used: a laser Doppler interferometer for the vertical and a microscope together with a stroboscope as a light source for the lateral movements (figures 6 and 7). Using the laser Doppler set up the deflection vs. frequency and phase with respect to the driving signal could be measured.

Using the microscope in combination with the stroboscopic light it was impossible to determine the phase shift between driving signal and actuator response and in consequence only the deflection were measured. The cut off frequencies of about 13 Hz for the lateral actuator are in good agreement with the estimated switching times of 35 msec for the lateral actuator.

During the tests of the µ-relay a minimum total resistance of the relay was found to be 3.40 Ohm. During the first 20 switching cycles the total relay resistance decreased continuously to reach a final value of 3.40 Ohm, while the contact resistance per each contact was found to be lower than 30 mOhm.

During the experiments the µ-relay was tested under small loads with 3 V and 3 mA current. The test was done under hot switching conditions which means that the load was not switched off externally during the switching of the relay. During off switching of the relay the lateral actuator was not activated. Only the vertical actuator was switched on and the lateral actuator slipped out of the clamping state.

After 500 000 switching cycles some damage on the contact and clamping areas was observed, but the relay has been successfully tested for more than 0,8 million switching cycles (figure 8).

Running the µ-relay in a driving mode which avoids the slipping effect during the off switching procedure by activating the lateral actuator should allow a drastically increase in expected life time of the relay. The tests showed that the bistable micro relay works and meet the specifications of a configuration switch. Especially the measured contact resistances of lower than 30 mOhm and the cycles tests with a total life time of more than 1 million cycles are major achievements of this bistable micro relay.

Figure 4:
Deflection vs. power consumption for the lateral actuator of the relay.

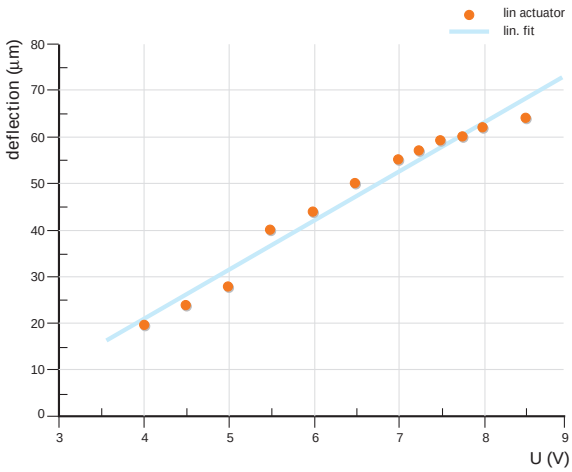


Figure 5:
Deflection vs. power consumption for the vertical actuator of the relay.

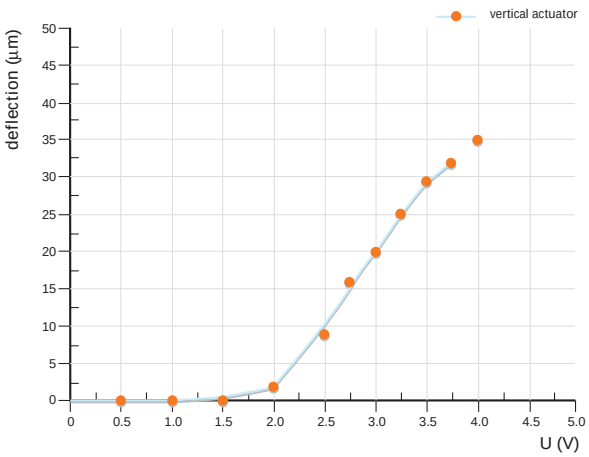


Figure 6:
Test of the dynamic behaviour of the vertical actuator. The actual deflection of the actuator was measured using a laser Doppler interferometer.

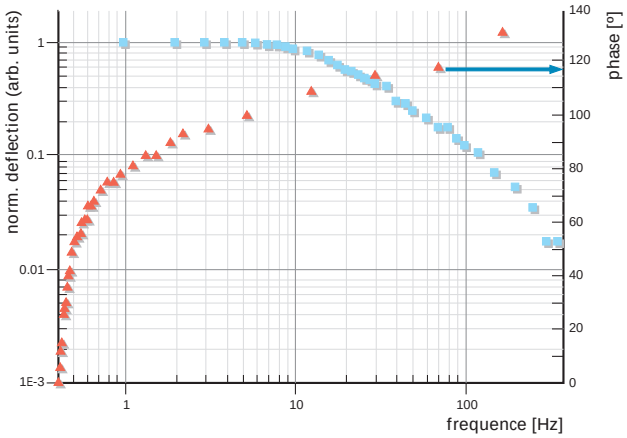


Figure 7:
Results for the dynamic tests of the lateral actuator. Since a stroboscope was used as a light source for the deflection measurements the phase of the movement could not be determined. Using the linear fit the cut-off frequency can be estimated to 13 Hz.

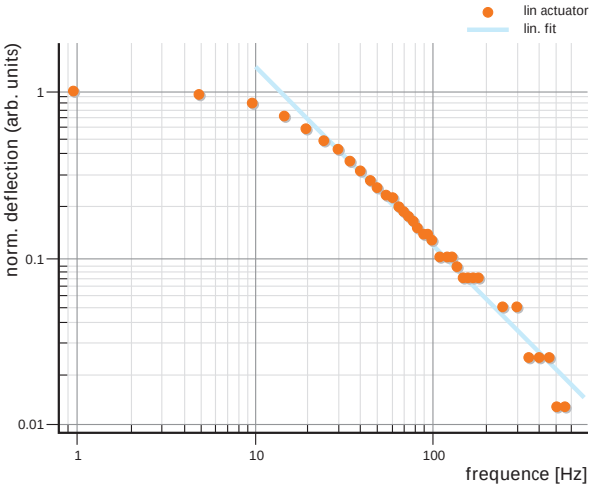
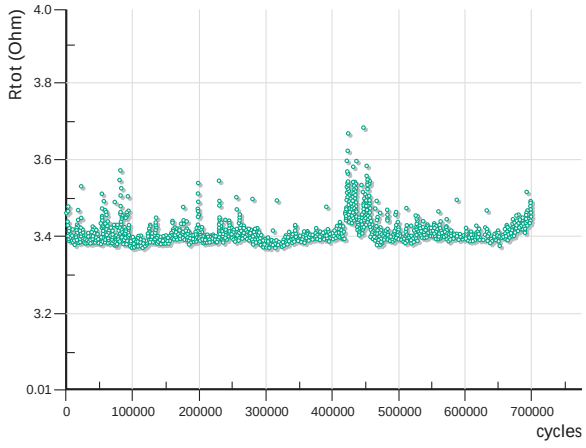
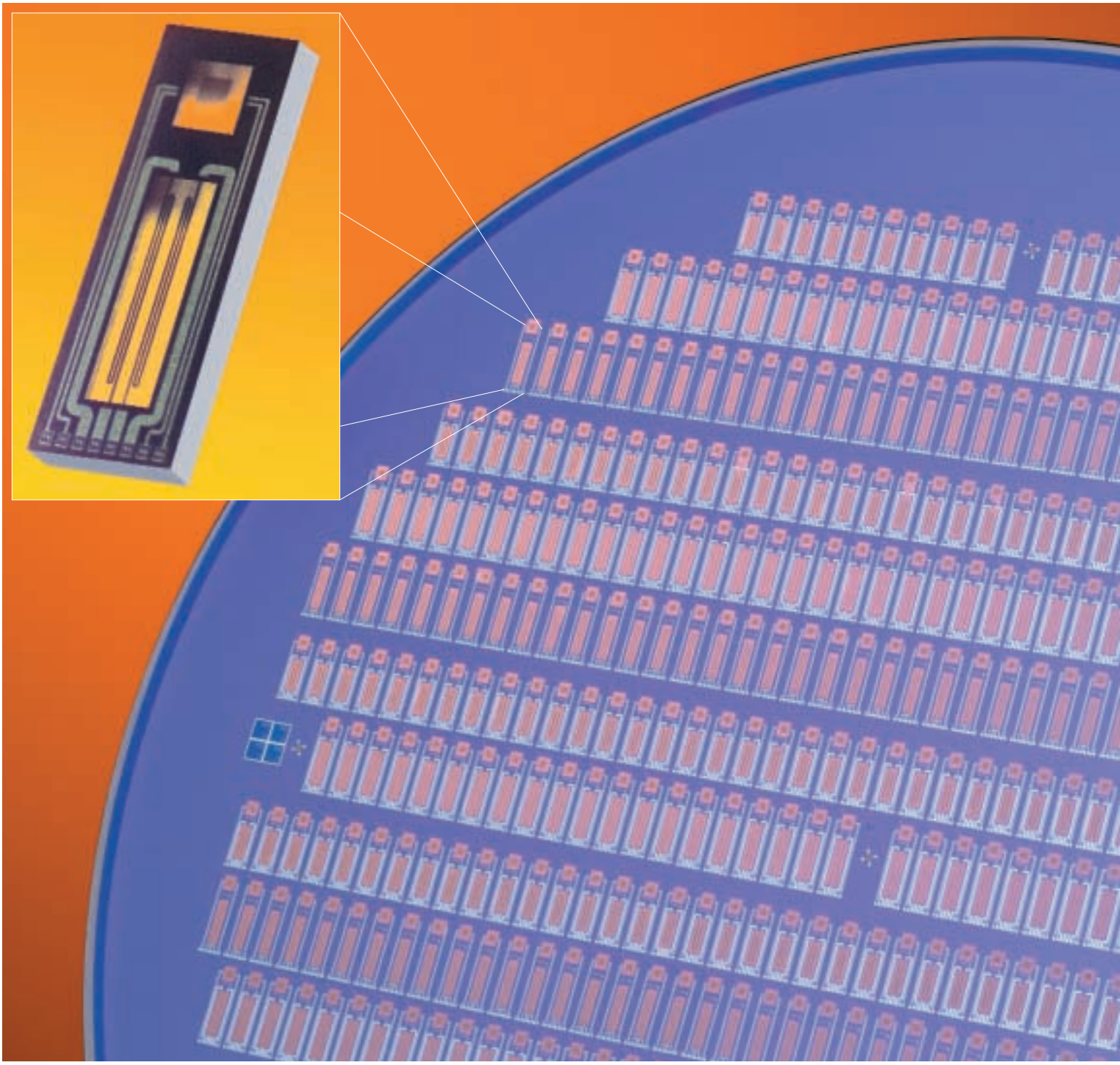


Figure 8:
Total resistance vs. switching cycles. During the first 800 000 cycles only small changes in the resistance were observed. The tests were performed under normal ambient conditions with a load of 3 V and 3mA.



Representative Results of Work
Microsystems Technology



A completely processed wafer
with three different MAF designs
for evaluation purpose.
Insert: a diced chip.

Mass Air Flow (MAF) Sensor with Recognition of Pulsation

In fuel and diesel engines in automotive application the exhaust gas recirculation (EGR) is controlled by a mass air flow (MAF) sensor. EGR is managing a mixing of intake air and exhaust gas in order to reduce NO content and particularly the number of particels and carbonhydrogens.

The working principle of a MAF sensor is based on a hot film anemometer (figure 1). Thereby a heater resistance (RH) is held at an elevated temperatur against the environmental temperature (RT). The resistance value according to a given temperature can be calculated if the temperatur coefficient of the resistor material is known. This resistor cools down during air flow but is held constant by a wheatstone bridge. The current which flows through the bridge is proportional to the air flow. Deviations according to the "Kings law", a nonlinearity between output signal and air flow, can be compensated by proper signal conditioning. For the detection of forward and backward air flow (recognition of pulsation), the measurement principle comprises two seperate measurement bridges. Therefore the MAF sensor itself is equipped with two complete half-bridges (figure 2). Each halfbridge is part of a wheatstone bridge. As the flow comes from the left side, the first heating resistor has a larger temperatur loss than the second resistors and vice versa, thus the change in resistance and the respective currents is different, this is shown in figure 3. Both signals are compared and fed into a microprocessor. From the amount and the sign of this signal the air flow values and the direction of flow can be calculated.

Figure 1:
Principle of a conventional anemometer

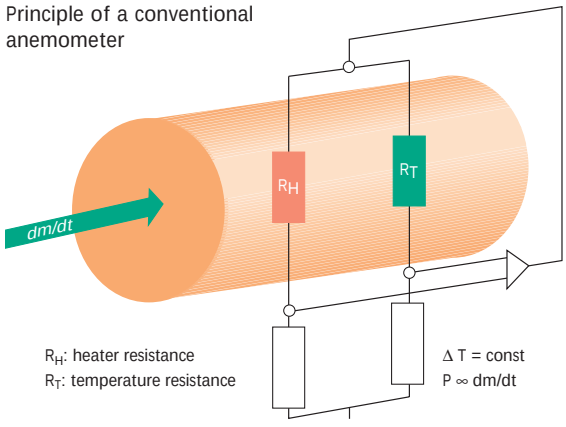
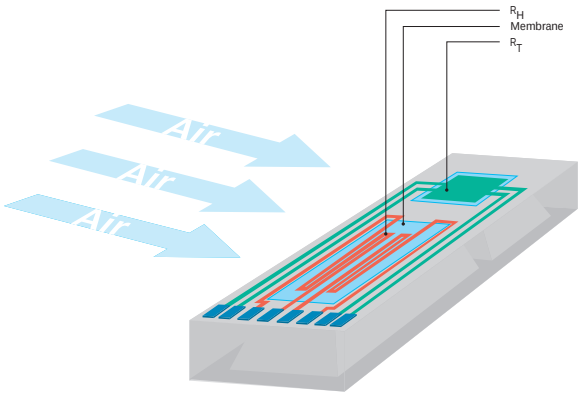


Figure 2:
Structure of mass air flow sensor



In the MEMS (Micro Electro Mechanical System) solution that was developed at ISIT, the resistors for heating and reference temperature are placed on a thin membrane. The resistors are made of Titanium coated for passivation with a thin TiN layer. The Ti/TiN thin film has a sufficient high temperature coefficient (3800 ppm/K) and is stable over a long period of time and at elevated temperatures (< 400°C). The membrane has a thickness of 1 µm and is made of siliconoxide and siliconnitride, deposited in Low Pressure Chemical Vapour Processes (LPCVD). A glass passivation with 1µm thickness is protecting effectively against environmental exposures. The freestanding membranes were formed in classical volume micromaching using an anisotropic KOH etching process. Therefore the application of double sided polished wafers and lithography from both wafer sides is neccesary. The membrane has an overall thickness of 2 µm and shows slightly tensile stress which is

appropriate for MEMS application. This ensures a excellent mechanical stability, high thermal insulation up to the chip edge, fast thermal response and high sensitivity. A cross-section of the sensor structure is given in figure 4. The application of Ti/TiN thin film technology is compatible with modern CMOS process technologies. Thus the design of the MAF sensor is based on standard MOS semiconductor batch processes, available for high volume, low cost production at ISIT.

The process flow was set up in PROMIS (Production Monitoring Information System). This ensures a lot and data tracibility for example for all process steps, load maps, alternate recipes, alternate process-chambers, parameters, controls, specs and limits, reworks, data collection and calculation. Also an advanced reporting system is available. After freezing the process flow an FMEA (Failure and Error Analysis) and control plan was developed. The critical processes which were identified therin are controlled by SPC (Statitistical Process Control), data charts and regular generation of cpk (critical process capability indicies).

Prototype testing was carried out either by the vendor or by ISIT and was succesfully performed to date. In particular:

- functional sensor test (reg. electrical specification)
- active test on corrosion: salt mist test (passivation layer)

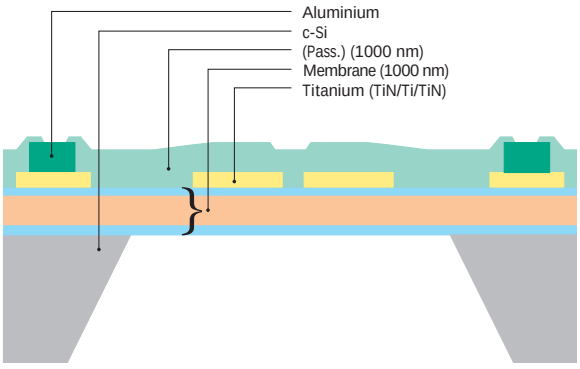


Figure 4:
Cross section of the sensor structure.

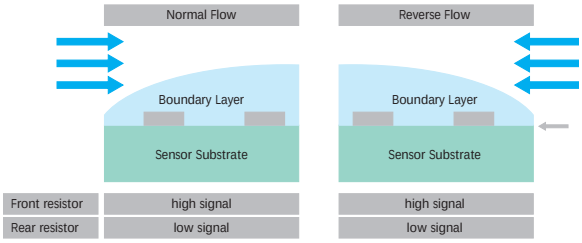


Figure 3:
Operating principle of a bidirectional mass air flow sensor.

- dynamic pressure test (10^7 load swings at 800 mbar)
- temperatur stability and water resistance
- shock stability
- life time (especially under current stress)

In the following the general data for a first overview are listed:

Dimensions	
chip	
- length	7750 mm
- width	2650 mm
membrane area	
- heater	1215 mm x 4000 mm
- sensor-reference	1215 mm x 1315 mm
membrane thickness (overall)	2 mm
passivation thickness	1 mm
Electrical data	
heater	
- resistance	50 Ω
- synchronism	0,01%
reference	
- resistance	2 Ω
- synchronism	0,05 %
flow range	7 to 2,500 kg/h
	2 to 5000 cm/s on sensor surface
	(depends on application and geometrical conditions)

This MAF sensor was originally designed for automotive specification but is also suitable for applications in medical care, air-conditioning and ventilation.

Fabrication and Replication of Large Area 3-D Nano- and Microstructures

Surfaces with shaped structures in the range from 500 nm to 20 µm can solve problems for several areas. For optical components the use of micro structured surfaces can reduce reflectance ("motheye effect"). Micro prisms can split light in two or more optical pathes and guide them in different directions ("daylighting systems"). Retro reflective structures can be applied for roadway marking or traffic signs. Non optical applications of microstructured surfaces are selfcleaning surfaces ("lotus effect"), artifical skin for reduced flow resistance, abrasive papers or microreactors.

The master structures for such funtional surfaces are shaped by stock removal (e.g. fly cutting) or lithographic processes (e.g. graytone lithography). The tooling is done by electroplating in nickel, the replication by hot embossing, UV casting or injection molding. In spite of the relative high mastering costs the replication costs per molded device for mass production are only a few cent.

The project NanoFab

The BMBF supported project NanoFab (FKZ 13N7746) had the goal to develop the basic machine- and process technology for fabrication and replication of such 3D nano- and micro-structures for large areas of about 1 m^2 and more. Five master tasks were defined (table 1) by the nine partners (table 2) to cover the whole process chain.

Table 1: Master tasks of NanoFab

1. Small area mastering by shape cutting chipping technology, lithography and holography and tool fabrication
2. Replication and recombination of small area embossing tools to large area embossing tools with stitching errors less than 1 µm
3. Fabrication of large area nickel tools for roll embossing
4. Assembly of a roll embossing machine with 100 cm working width
5. Development of application specific measurement tools for shaped surface characterisiation

Table 2: Project partners of NanoFab

- Fresnel Optics GmbH
- FRT Meßtechnik GmbH
- Kugler GmbH
- Nanofocus Meßtechnik GmbH
- Scana Holography Company GmbH
- TESA/Beiserdorf AG
- FhI für Produktionstechnologie IPT
- FhI für Siliziumtechnologie ISIT
- FhI für Solare Energiesysteme ISE

Table 3: Typical graytone lithography parameters

max. structure height:	23 µm
max. design area:	32 mm x 40 mm[1]
design grid:	about 1 µm
graytone levels:	up to 500
overlay error:	0
substrate:	6" Si-Wafer

[1]restricted by data amount

The main contribution of ISIT focused on mastering by graytone lithography, replication by UV casting, characterisation of an adapted UV illumination source and recombination on laboratory scale. Some exemplary results will be consecutively discussed.

Lithography based mastering

Graytone lithography is applied for mastering. This process offers the opportunity to control beside x- and y-direction also the z-direction of the resist shape during the exposure and development. Figures 2 and 3 show shaped surfaces with typical dimensions. Tab. 3 shows a set of possible parameters.

Fabrication of the Nickel tool

The process for fabricating a Nickel tool for UV casting is shown in figure 4, based on Nickel evaporation and electroplating. The tool has the negative tone surface with respect to the master (figure 5).

Figure 1:
Technology chain for replication based on resist mastering.

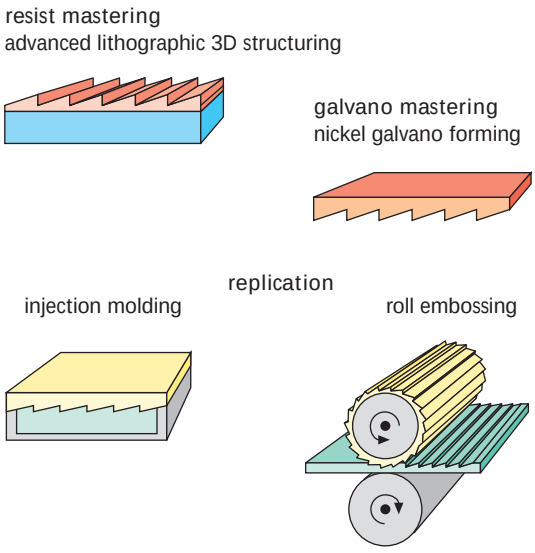


Figure 2:
Micro lens array, 50 µm pitch.

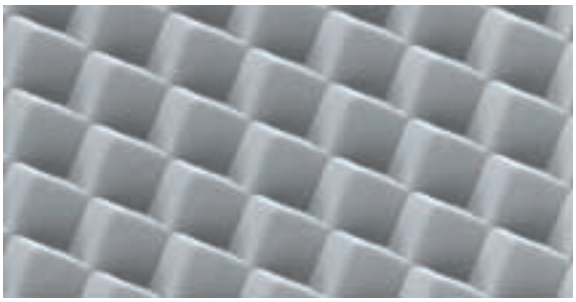


Figure 3:
Retroreflector (full corner cubes), 20 µm cube egde length.

UV casting materials

The evaluation of an applicable replication process shows, that only UV casting has the potential to fulfill the requirements for recombined embossing with field stitching less than 1 µm. A specific ORMOCER® developed by FhG-ISC has been selected as a promising candidate for the UV-casting because of its good processability and good contour accuracy (figure 6).

Evaluation of UV source

Beside the UV material also the UV illumination is important to achieve the stitching goal.
The concept for the UV based recombination is shown in figure 7. As UV lightsource a mercury-arc lamp has been used in combination with a projection optics from a lithography stepper tool and a chromium glass mask for defining the illuminated area. The evaluation of a suitably specified illumination system shows that the required intensity change from 1 to 0 within 1 µm inside the ORMOCER® can be realized. This is demonstrated by the line and space structure in figure 8.

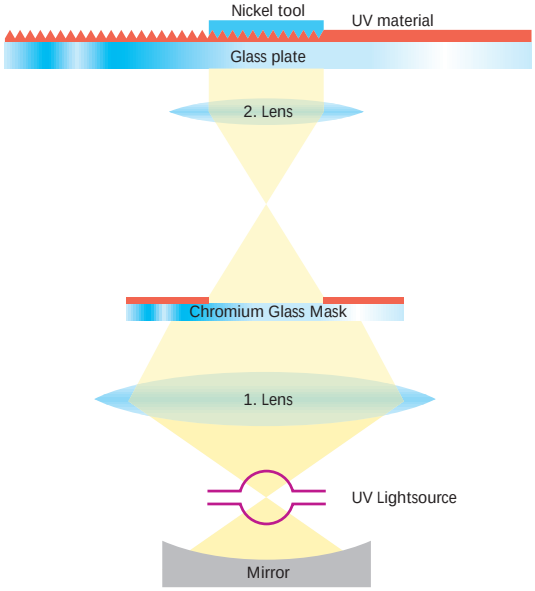
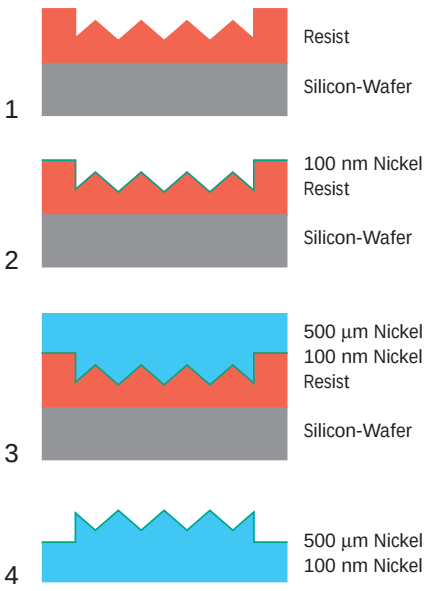


Figure 7:
UV illumination system for the recombination machine.

Figure 4:
Process chain for Nickel tool fabrication



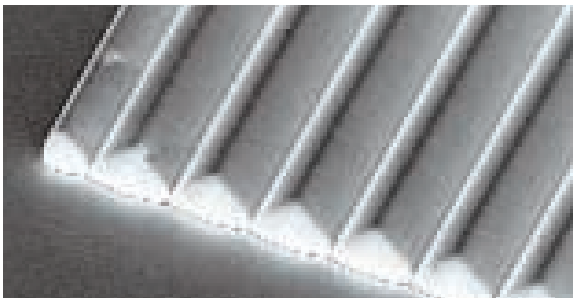


Figure 5:
Nickel tool for UV casting of V-grooves.

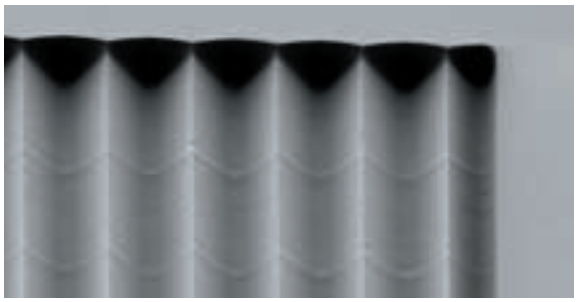


Figure 6:
V-grooves UV casted in ORMOCER®, 17 µm pitch, 45° tilted.

Service offer

Based on this experience and together with industrial partners ISIT integrates in unique way the knowledge and technological skills of fine mechanics, plastics engineering and silicon technology. High precision surface topography is generated by advanced lithography process technology. Beside digital lithography with thin and thick resist layers ISIT uses its profound knowledge in graytone lithography. Digital or arbitrary shaped surface reliefs from nanometer to micrometer scale can be formed enabling the production of arbitrarily formed 3D surface topographies. Furthermore diffractive gratings and dot matrix holograms for decoration or security application can be created. The resist structures are then copied to metal shims by the special electroplating process. These Nickel shims are available for polymer replication processes like roll embossing (Scana Holography Company) or injection molding (OK Media Disc Service). The complete technology chain can be offered as a global service for production from small to big volumes.

Applications areas

- refractive micro optics
- diffractive micro optics
- beam forming elements
- security labels
- holographic structures
- nano- and micro-structured foils

Table 4: Typical replication parameters

injection molding	
materials :	Polycarbonate, PMMA
max. size :	CD size
thickness :	0,6 mm / 1,2 mm
options :	coatings of Al, Au etc.
roll embossing	
materials :	PET, BOPP, Polycarbonate
thickness :	23 µm – 100 µm
roll-width :	up to 200 mm

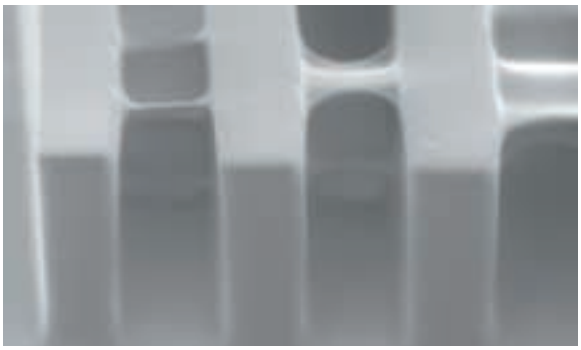


Figure 8:
UV exposed ORMOCER®, 50 µm pitch, 72 µm thick.

Figure 9:
Injection molding.

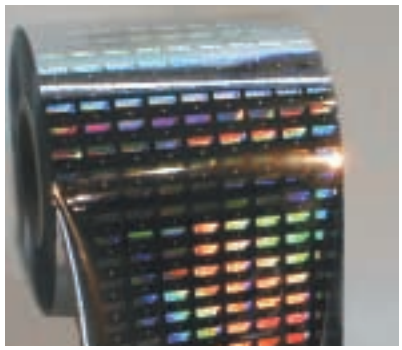


Figure 10:
Roll embossing.

Representative Results of Work
IC-Design

Development of a Fast and Precise ASIC to Control CNT's for Nanolithography

The three years NANOLITH project (IST-1999-11806) aimed at demonstrating the feasibility of high throughput and high resolution (10 nm range) parallel e-beam lithography for mask making. The project was performed in co-operation with Thales/Thomson-CSF, the University of Cambridge and the University of Lyon. The electron microguns, each delivering a 10 pA current, were independently driven by CMOS circuits.

The purpose of the microgun electronics is to select an Carbon Nano Tube (CNT) pixel and control a CNT emission current flow within a fixed time interval by switching a high voltage transistor. It is the goal to ensure a constant current-time-product, which is equivalent to a specific dose value for resist exposure. That means, a fixed time interval per pixel corresponds to a minimum current value in order to reach a required exposure dose for the resist. If the emission current is e.g. 1 nA the exposure time needed for a resist sensitivity of 20 µC/cm2 amounts to 2 µs for a pixel size of 100 nm x 100 nm. In case the current value is higher the exposure time has to be reduced by the dose control circuit. In conclusion, the dose control unit ensures the required dose also in case of varying current values of the CNT emitters. In addition the ASIC is able to control whether the CNT delivers a current or not to avoid an under exposure.

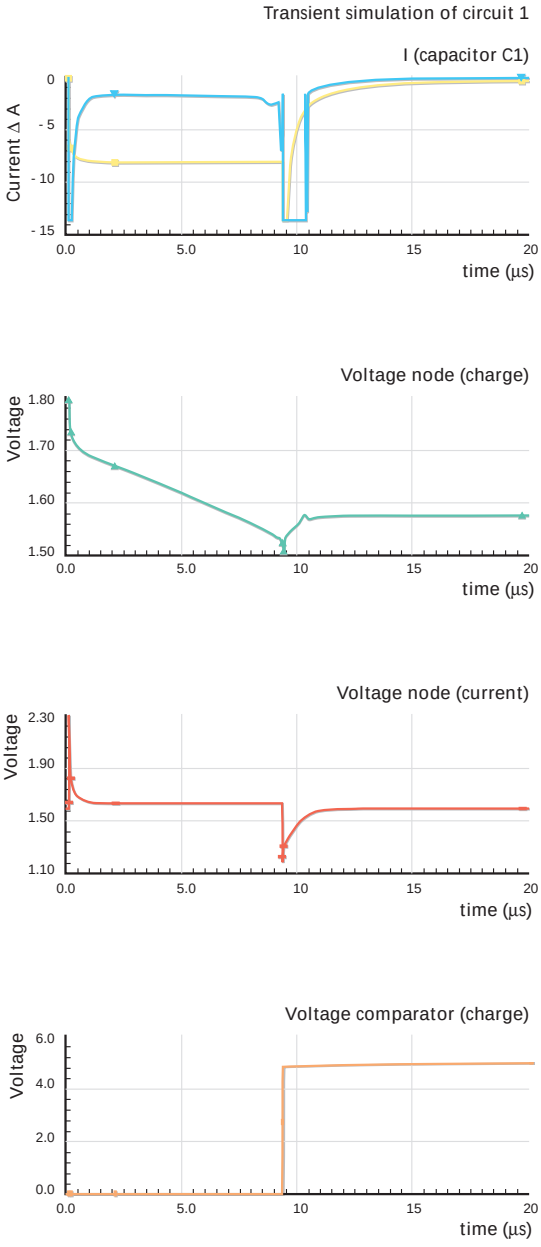


Figure 1:
Results of the electrical simulation of the circuit.

Figure 2:
Small ASIC placed in the open measurement box.

Figure 3:
Set-up including the measurement box with the ASIC inside, that was controlled by a PC by using TESTPOINT program.

The main problematic was the combination of switching a high voltage of 50 V and measuring a small current of a few 10 to 100 nA in a short time frame of up to 10 µs. Two main problems occurred: first switching on and off of higher voltages results in a fast change of the voltage of the node involved with a time schedule of the measurement time determined by the capacitors and resistors in the network, i.e. the RC time constants. Secondly the charge taken to load or unload the nodes is the charge, and current respectively that has to be measured. To reduce both problems a circuit was developed, that runs with a constant bias current through all branches that drastically reduces the ringing of the nodes and delivers the charge for loading.

The simulation results in figure 1 show the behaviour of the most important nodes in the circuit. The blue curve shows the current that flows from the capacitor 1 and the green curve below the voltage across this capacitor representing the charge flown. The red curve shows the voltage of node „current“, that represents the actual current flowing.

The brown curve shows that after roughly 9 µs the comparator detects that enough charge is flown and it switched the CNT off.

Figure 4 shows the good linearity for the charge measurement for different bias currents, starting from 40 nA to 800 nA in 5 steps, that was measured with the set up shown in figures 2 and 3.

In figure 5 the ASIC was used with an open CNT-pin, i.e. no current could flow into the circuit. For different bias currents the reference voltage applied to the comparator that controls the current, was changed. Hence, this results show the voltage drop of the bias current across two transistors and that the circuit works well.

Overall it could be shown that for the control of the charge amount the specifications were reached:
- specified:
1 nA – 10 nA in 10 µs => 10^{-14} - 10^{-13} As
- measured:
200 nA for 50 ns – 16 µs => 10^{-14} - 3,2 x 10^{-12} As.

Figure 4:
Measurement of the time needed to charge C1 for different bias currents and reference voltages.

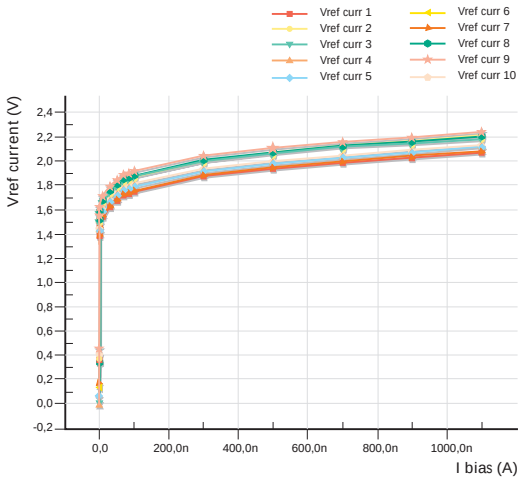
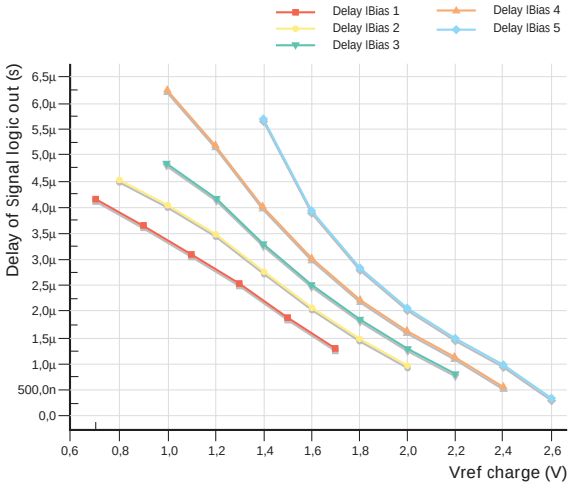


Figure 5:
Switching behaviour of different circuits of the current control function for different bias currents.



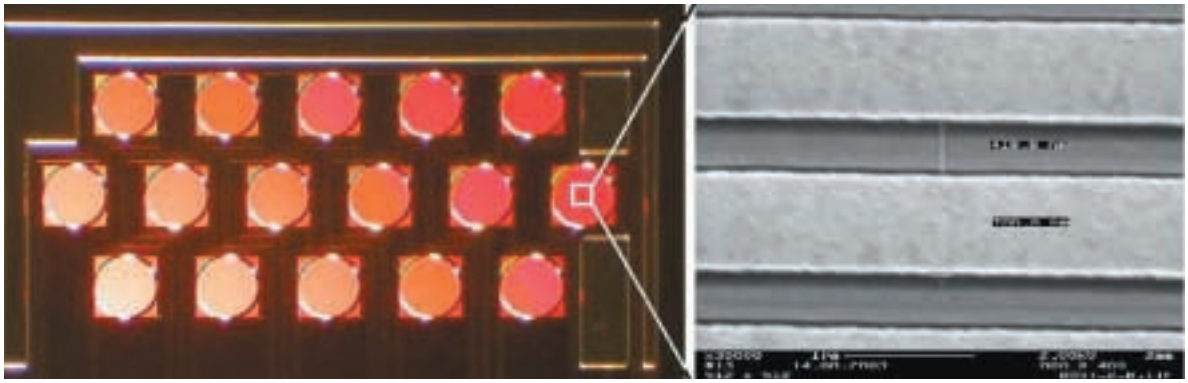
Electrical Biochips with Microelectrode Arrays for Detection of Antibiotics

The rapid and inexpensive detection and quantification of antibiotics in food is of high commercial interest. Available methods are dipstick tests or enzyme linked immunosorbent assays (ELISAs) mostly with optical detection (1). Rapid tests for parallel identification of the common used antibiotics like penicillin G (PenG) and chloramphenicol (CAP) with high sensitivity and reproducibility are not at the market today.

We have developed a PenG-Assay in a competitive ELISA format on an electrical biochip array with 16 positions. Each position (500 µm in diameter) consists of interdigitated gold ultramicroelectrodes (IDAs) with 800 nm width and 400 nm gap (figure1). All positions have a main cathode while the 16 anodes are read out individually by a multiplexed 16 channel potentiostat (model "CiPo", eBiochip Systems GmbH), which enables the redox recycling of an enzyme product.
The biological interface of this assay is illustrated in figure 2.

A PenG protein conjugate was spotted by an automated microdispensing device onto seven chip positions. These capture molecules were immobilised via thiol links to the gold electrodes. Another six positions were covered with a biotinylated protein for positive control. Three positions were left uncovered for negative control. The sample containing PenG together with biotinylated Anti-PenG antibody was pumped over the chip surface by an automated fluidic device. The competition of PenG in the solution and on the chip for binding the Anti-PenG antibody results in a quantifiable amount of biotinylated complexes on the position's surface. Because of this competition effect the PenG positions do not reach the values of the positive control positions. After labelling of these positions with a label enzyme, a substrate was added. This substrate was converted by the label enzyme alkaline phosphatase into its redox active form and could be measured position specifically in a stopped flow modus.

Figure 1:
Left: microscope picture of the 16 chip positions surrounded by a counter electrode.
Right: SEM picture of the gold IDA electrodes with 800 nm width and 400 nm gap.



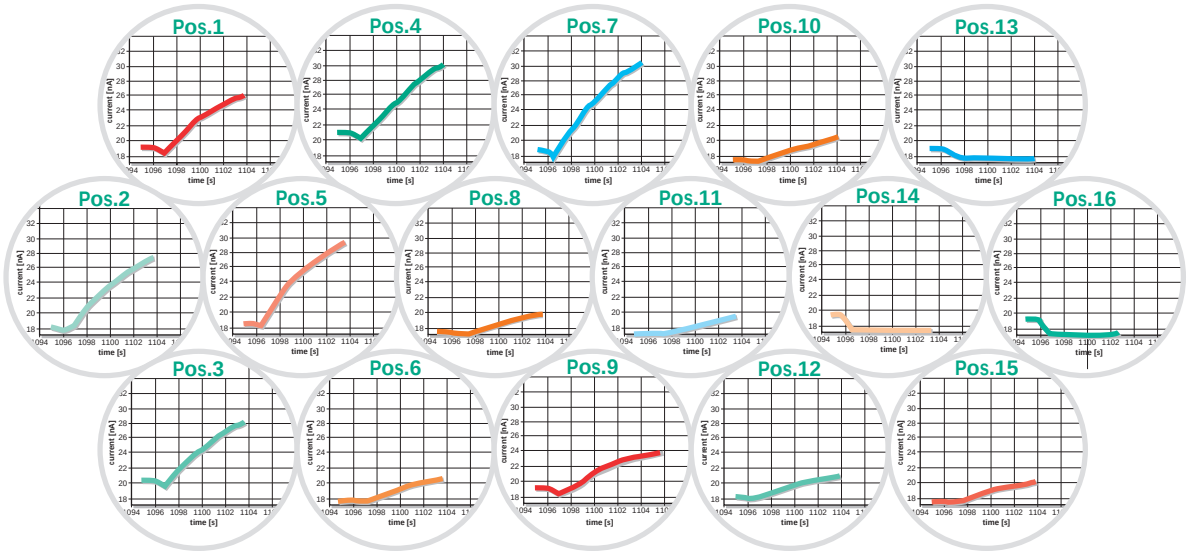


Figure 3:
Current response curves of all 16 positions.
Position 1, 2, 3, 4, 5, 7 were used for positive control, position 6, 8, 9, 10, 11, 12, 15 were used for PenG detection and position 13, 14, 16 for negative control.

The resulting current response curves for each position as shown in figure 3 represent a sample containing 6 ng/ml PenG.

An internal calibration was made by using the positive and negative control positions. For this assay the linear fit is between 2 and 10 ng/ml PenG. The maximum residue limit (MRL) of PenG in food is 4 ng/ml (2). Our detection limit is 2 ng/ml. To obtain higher reproducibility, multiple positions were used for averaging. This electrical array platform could also be used for simultaneous detection of more antibiotics in parallel.

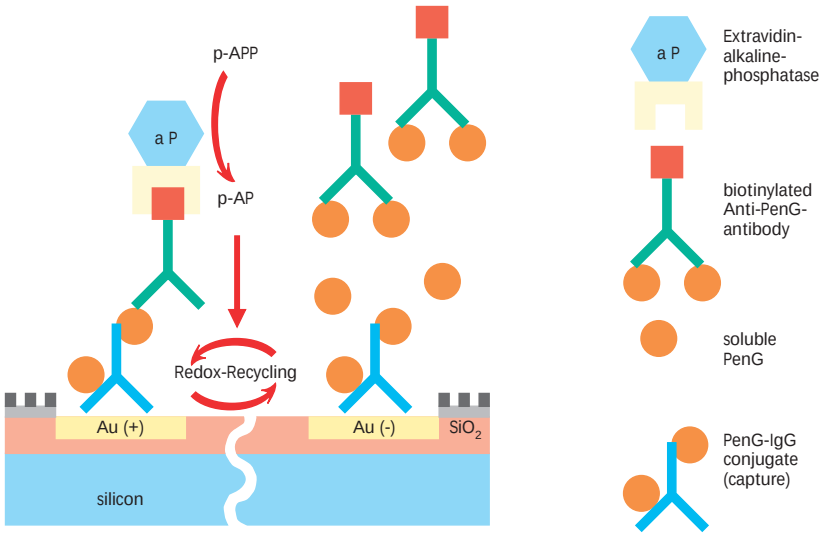


Figure 2:
Scheme of the biological interface at a PenG position. In absence of PenG a high signal results from redox recycling of the enzymatically converted substrate p-aminophenyl phosphate (p-APP) into p-aminophenol (p-AP), (left part of position). In contrast to this a PenG containing probe shows no signal (right part of position).

Literature:
1) Suhren, G., Kieler Milchwirtsch. Forschungsber. 2002, 54, 35-73

2) Commission Regulation (EEC) No. 2377/90, Off. J. Eur. Communities 1990, L224,1-8

Demonstration Line for the Industrial Handling of Ultra-Thin Silicon Chips

The international electronics manufacturing exhibition Productronica 2003, Munich was the place to demonstrate the industrial user the assembly of ultra-thin silicon ICs in production scale. This demonstration shows the results of the european funded IST-project FLEX-Si that aimed at the developement of the basic process flow for the handling of ultra-thin wafers and chips and the project FLIBUSI that evaluated and optimized a full automatic Datacon flip chip bonder for the assembly of ultra-thin ICs on industrial scale.

On the basis of a smart-label transponder, a complete assembly line with integrated in-line test was demonstrated in production mode. The line concept was jointly developed with the company Fuhrmann Consulting Network, Munich. A Philips MIFARE transponder IC was selected for the application. The chip was thinned down to 50 µm on 200 mm wafer. The chips have been bumped at Fraunhofer ISIT with 5 µm electroless NiAu for a soft solder flip chip attach on flexible substrate. This processing sequence was found the most reliable during the FLEX-Si project:

1. wafer test
2. wafer bumping
3. wafer thinning
4. wafer mounting on UV-tape
   (best at the thinning provider)
5. UV-tape exposure directly after dicing
6. assembly

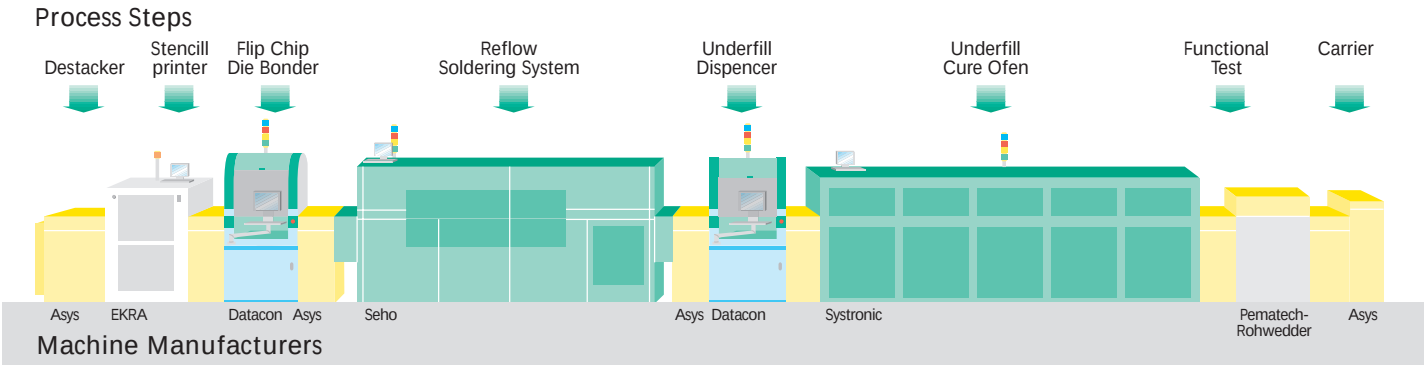
The solder material is stencil printed on a flexible substrate attached to a carrier. A Heraeus lead-free class 5 solder paste (SnAg3,5) was selected for the flip chip assembly to demonstrate that ultra-thin ICs can be assembled to green electronics. The carrier concept is manufactured by the company Schnaidt Lötrahmensysteme. The main benefits are the fast substrate mounting and that no vacuum support is needed in the single machines of the production line.

In the FLIBUSI-project a smart label was selected as one example for application of ultra-thin chips in the larger field of transponder technology. Here, the thin and flexible silicon memory chips can be embedded in paper, foil or fabric. The intelligent electronic labels can communicate contactless with their environment. In the future, these labels will be an integral part of our life. The expected volume is estimated to be in the range of billions, when consumer articles will be fitted with transponder chips. These will carry different information about price, production date and production site, quality class and will ease or even automate the purchase, clearing and quality controll. Security functions are implemented into the transponder electronics to prevent misuse or fraud.

Power electronics is a second example for the need to assemble ultra-thin chips. The thinner these chips become the better are their electrical properties. Such devices will reduce the energy consumption of refrigerators and other household appliances when cost-effective, intelligent adapted controllers can be applied for the 230 V household mains supply.

The handling of ultra thin Silicon wafers is quite difficile and is putting high demands on the further processing technology. Completely new equipment infrastructure must be developed for the processing, which is expensive and time consuming, or standard industrial equipment and processes have to be modified and optimized for the handling of ultra-thin wafers and chips. The FLIBUSI line is evidence of the feasibility of the second way, successfully realized by Fraunhofer ISIT. In the following the most important results are presented. In the first step after the wafer processing, the devices are thinned from the backside with several grinding steps. This procedure generates layers with a degraded cristal structure that makes the wafers fracture sensitive. The degraded layers are removed by etching or polishing. The originally stiff Silicon disk is now a flexible foil with a thickness below 50 µm that bends under gravity.

Ultra-thin wafers can be diced on a standard wafer dicer. The wafers are mounted on a



Production: Smart Labels PAV Card

Figure 1:
FLIBUSI-LINE. Main steps of the demonstrated process flow.

Figure 2:
Transponder assembled as solder flip chip device.

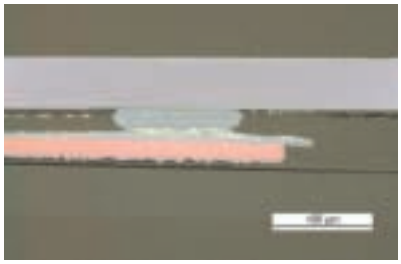


Figure 3, right:
Danfoss Silicon Power module manufactured during the FLIBUSI project.

selected UV-tape, that provides a very low residual adhesion during the chip release. The tape is mounted on a frame, that supports the wafer. All further handling is performed on the frame reducing mechanical stresses on the wafer to a minimum. The dicing is performed with a diamond blade at high RPM with high feed speeds. The productivity of the dicing process could be more than doubled with the same quality results compared to silicon wafers with standard thickness. Although the dicing generated microscopic edge defects in the silicon chips, it could be demonstrated during the FLIBUSI project that the yield loss during the chip assembly is neglectable. Over 100.000 flip chip assemblies have been produced, with a yield loss due to chip fracture < 0,2 %. The handling of ultra-thin wafers on dicing tape is robust and the chip release could be demonstrated to be stable even for more than 24 months after UV-exposure of the tape. The UV-exposure itself was found to be a critical step. A too low UV-density does not reduce the ahesion strength of the tape enough to secure a gentle chip release. ISIT recommends to expose the tape directly after dicing, using a high density UV-source and to test the chip release after exposure before sending the diced wafers out.

A die or flip chip bonder applies a set of needles to release chips from the dicing tape. For standard chip thickness, sharp needles are used that penetrate the tape and delaminate the chip from the tape. The impulse and stress introduced by this standard process exceed the mechanical strength of the ultra-thin silicon chips. Still the needle eject can be used, but with rounded needles, a synchronous eject and a take over process. The non-penetrating needles with a top radius of up to 350 µm release the chip from the UV-tape with a reduced needle amplitude of below 400 µm and do not generate needle induced defects on the chip backside. While the needles move the chip upwards, also the vacuum die tool is moved upwards. This synchronous movement prevents a buildup of high forces onto the ultra-thin chip. The process itself is much faster than the standard release from blue tape with the additional benefit that the rounded needles do not wear out. The robust handling of ultra-thin flip chips was demonstrated within the FLIBUSI project with a cycle time of below 1,2 sec including a camera alignment of the ejected devices. This is a very acceptable value for a demanding process.

Beside flip chip on flex, ISIT is able to use the technology also for flip chip on wafer assembly and chip stacking. A wide range of applications can be assessed with these basic packaging technologies.

ISIT offers to adapt the assembly technology for ultra-thin silicon devices to customer needs and to perform the application specific characterization. Using the automated assembly equipment available at ISIT, close to production demonstration series of industrial samples can be manufactured to test the market response.

ISIT greatly acknowledge the funding by the European Commission under the project no. IST-1999-10205 and IST-2001-32315.

Damage Mechanisms in Lead-Free and Tin-Lead Solder Joints at Elevated Temperatures

Introduction

Electronic assemblies are increasingly applied by the automotive industries. Conventional soldering alloys are not capable to withstand the temperatures and temperature shocks which occur e.g. inside the electronic control system right next to the engine. Operating temperatures of 150°C and more subject the soldered connections to material stress factors which are sufficiently powerful to change their interior structure. This in turn allows and promotes the growth of intermetallic phases, causing – in combination with the large temperature differences – the generation of cracks, which will cause failure of the entire assembly. Additional load is generated by high-power components whose temperatures may also approach the melting temperature of the solder. Therefore, alternative soldering alloys with higher melting points are needed. Additionally, legislation restricts the use of lead beyond 1st July 2006 in electronic products. Thus, the use of Pb in solder alloys has to be avoided. The reliability of these alternative solders under full operational conditions, meanwhile, has not been sufficiently established.

Lead-free solders SnAg3.5 and SnAg4Cu0.5 were evaluated (in reference to the conventional solder SnPb37Ag2) for the connection of power transistors on a thick-film circuit. Defined loads (exposure to elevated temperatures and temperature cycling) were used to accelerate the ageing of the solder joints in order to allow comparative analyses regarding their long term behaviour,

Figure 1: Microstructure as soldered, SnAg4Cu0.5.

for instance in automotive applications. Metallographic techniques such as optical microscopy (OM) and energy-dispersive X-ray analyses (EDX) in a scanning electron microscope (SEM) were used to explore the damage-causing processes and the sites where these damages most frequently occur. Aim of the work was the quantitative description of the growth of the intermetallic phases between solder alloy and metallisation as well as the fatigue behaviour of the solder alloys in a comparative analysis using the example of a TO220 component on a thick-film circuit.

Description of experiments

Production of samples, exposure to heat and temperature shocks

The components were conventionally soldered (maximum temperature about 20°C above the melting point of the soldering alloy for a duration of app. 30 s). Accelerated ageing was achieved by exposing the samples to temperatures of 125, 150 and 175°C for a duration of 140 and 400 h each. Furthermore, some of the samples were subjected to temperature cycling tests (temperature range: -40 to +125°C; cycle times:

Figure 2: Phase growth between solder SnPb37Ag2 and AgPt-thick film; 150°C/140 h.

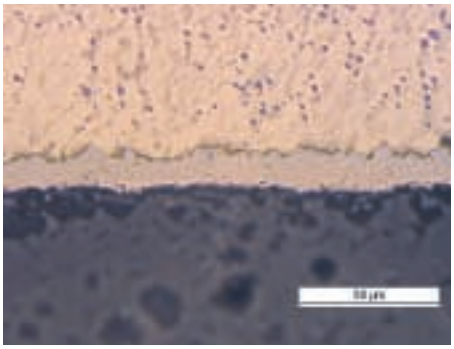


Figure 3: Phase growth between solder SnAg3.5 and AgPt-thick film; 150°C/140 h.

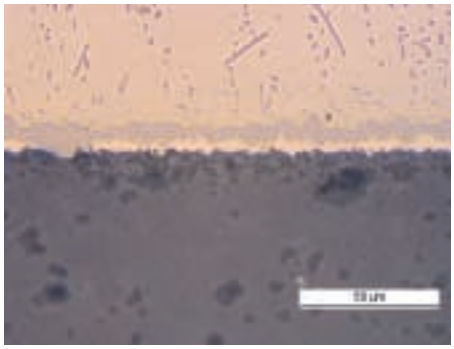
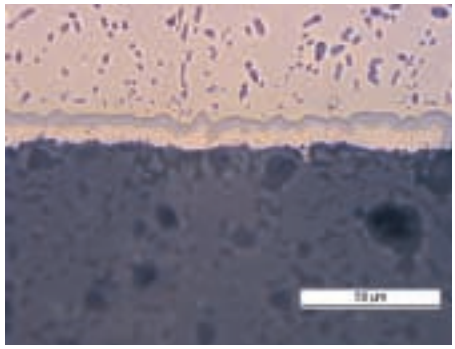


Figure 4: Phase growth between solder SnAg4Cu0.5 and AgPt-thick film; 150°C/140 h.



40 min and 3.2 h) to test the fatigue resistance of the solder joints. Between 250 and 1000 of such temperature cycles were applied. The crack growth in the solder layer was observed by measuring the thermal resistance.

Metallographic preparation and evaluation

Power electronic assemblies consist of different materials with correspondingly various properties. Therefore, the metallographic preparation of such material compounds is a difficult task, since preparation artefacts such as rounded edges, the generation of reliefs between hard and soft materials, erosions of the softer materials and break-out of the brittle component ingredients all need to be avoided. The bottom side of the transistor component TO220 (app. 5 µm Ni on Cu, figure 1) was soldered on the thick-film circuit (Al_2O_3-ceramic with an AgPt-thick film metallisation, figure 1). The cross-section was typically placed through the centre of each component.

Results

Exposure to elevated temperature

After having been exposed to 150°C for 140 h, the samples had developed differently on the thick-film side: The AgPt-metallisation had already been completely converted into an intermetallic phase layer with the lead-containing solder, see figure 2. In comparison with the lead-containing solder, the solder SnAg3.5 had developed a thinner intermetallic phase. A residual Ag-layer of the metallisation is clearly visible, see figure 3. The intermetallic phase generated with the solder SnAg4Cu0.5 is even thinner, and the residual silver of the thick film is still thicker than the intermetallic phase, see figure 4. A high Ag-content in the solder apparently retards the conversion of the AgPt-thick film, i.e. the growth of the intermetallic phase layer.

Damage caused by fatigue due to thermal cycling

Crack patterns appear similar in all three soldering alloys. In the eutectic solder SnPb37Ag2 the fatigue crack propagates through the solder, usually adjacent to the interface to the AgPt thick film, figure 5. The fast temperature shock cycles in particular seem to generate a clearly discernible band of recrystallised Sn and Pb grains which is less resistant to any further cyclic deformation and (eventually) any further crack growth than the original as-solidified microstructure. Creep mechanisms such as grain boundary diffusion and grain boundary sliding can operate more easily in the recrystallised microstructure which is why temperature shock cycles accelerate fatigue crack growth. Slow temperature changes allow a more homogeneous creep deformation which inhibits a localisation of the deformation. In order to recrystallise the eutectic SnPb-microstructure, a certain period of time is required (here: about 250 cycles) during which no discernible differences between the three solders occur, figure 6. It is only after this "incubation period" that the damage / the fatigue crack growth is progressing faster in the SnPb-solder

Figure 5:
Cracks in the SnPb37Ag2 solder joint after 400 temperature shock cycles (-40/+125°C, 40 min cycles).

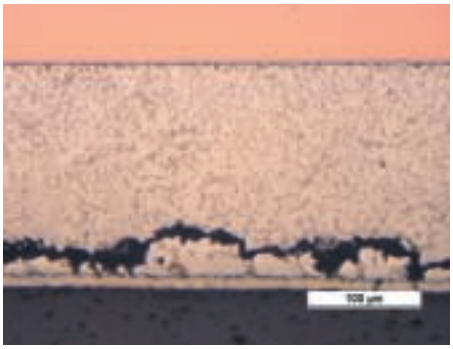


Figure 6:
Increase of the thermal resistance with temperature shock cycles (-40/+125°C, 40 min cycles).

than in the more creep-resistant SnAg-solders.

Following these considerations, the three solder alloys are characterised by essential differences in their resistance to microstructural changes under a given fatigue load (temperature range, cycle time). The geometry and elasticity of the joined partners define a certain rigidity of the bonded structure. The different thermal expansion coefficients of the bonding partners together with this rigidity subject the solder gap to displacements and forces which are balanced by the creep properties of the soldering alloy (and the solder gap's geometry).

In rigid structures, the displacement amplitude of the solder gap is mainly independent from the cycle time of the temperature shock tests ("displacement controlled"). The faster the deformation takes place, the more likely it is that the deformation will take place in a localised band of recrystallised microstructure and that it will increase the effective strain amplitude while decreasing the number of tolerated cycles. Under these conditions (which apply to the TO220 component on a ceramic substrate), fast cycles are more damaging. The SnAg-solders are less susceptible to recrystallisation than SnPb, which is why their fatigue behaviour hardly seems to depend on cycle times at all. If, however, the structures are less rigid (i.e. if at least one partner is elastically compliant), a given displacement amplitude will cause different creep strain amplitudes in the solder gap, depending on the individual cycle time, because the displacement can partly be absorbed by an elastic deformation ("load controlled"). The higher the temperature and the longer the time, i.e. the more slowly the change in temperature proceeds, the larger is the creep strain amplitude in the solder and therefore the fatigue-induced damage. Under these conditions, slower cycling will be more damaging. The transition between the two is fluent, since the creep behaviour depends on the solder alloy, temperature, time and stress. Therefore, general predictions on the fatigue behaviour of a given structure are difficult.

Combination of loads and damage-causing mechanisms

Figures 7 to 9 show the state of all three solders after having been exposed to high temperatures (150°C/400 h) and additionally to temperature cycles (-40°C/+125°C, 3.2 h, N = 450). The most conspicuous characteristic is the delaminated thick film of the SnAg3.5-soldered specimen in figure 8 and the rapid increase of damage, depicted by the strongly increasing thermal resistance, figure 10. The fracture here occurred in the metallisation, because the SnAg3.5-solder is significantly more creep-resistant than SnPb37Ag2. This is why the connection – due to the deformations which have been caused by additional temperature shocks – is subjected to higher stresses than the softer SnPb-solder. The latter softens by coarsening during the heat exposure and particularly due to the temperature shocks by recrystallisation in the cyclically deformed zone (in figure 7, close to the thick film) which also marks the preferred path of the fatigue crack. The extensive relaxation in the solder prevents the damaged thick film metallisation from being subjected to significant

Figure 7:
SnPb37Ag2 solder joint exposed to thermal ageing (150°C/400 h) with subsequent temperature cycling (-40/+125°C, 3.2 h, N = 450).

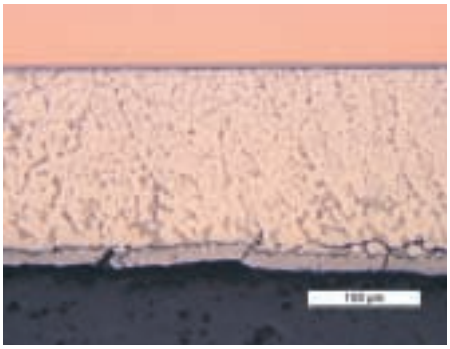


Figure 8:
SnAg3.5 solder joint exposed to thermal ageing (150°C/ 400 h) with subsequent temperature cycling (-40/+125°C, 3.2 h, N = 450).

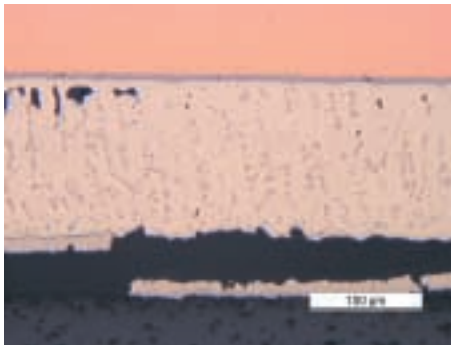
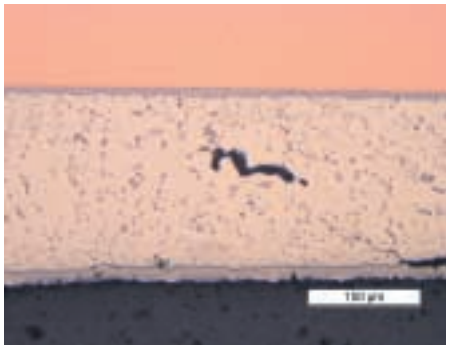


Figure 9:
SnAg4Cu0.5 solder joint exposed to thermal ageing (150°C/400 h) with subsequent temperature cycling (-40/+125°C, 3.2 h, N = 450).



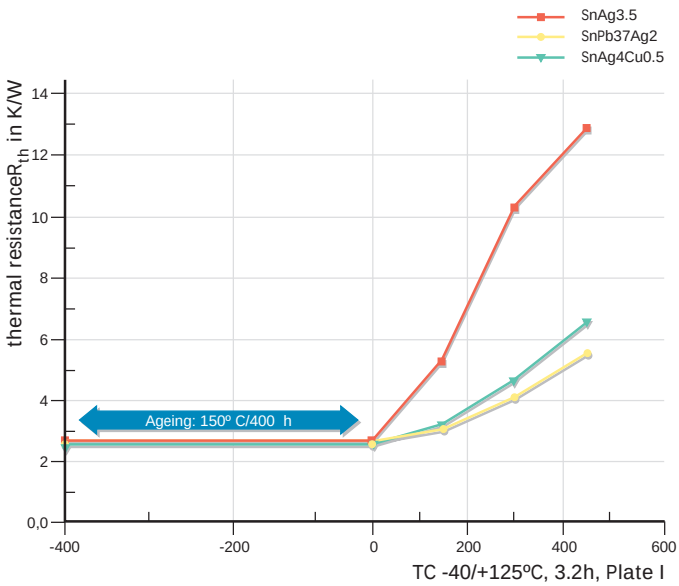


Figure 10: Increase of the thermal resistance with temperature cycling (-40/+125°C, 3.2 h cycles) applied after thermal ageing (150°C/400 h).

stresses, figure 7, keeping the connection from failing as in the case of the SnAg3.5-solder. Although the solder SnAg4Cu0.5 is at least as creep-resistant as SnAg3.5, a residual AgPt thick film remains (discernible in figure 9), due to the slower phase growth under the experienced thermal stress, providing a sufficient adhesive strength between metallisation and ceramic substrate and preventing the connection from failing. Concerning the changes in the thermal resistance, the performance of the conventional SnPb37Ag2-solder under a combination of loads is nearly as good as the (more creep-resistant) solder SnAg4Cu0.5.

Conclusions

The study demonstrates that ageing processes such as coarsening, recrystallisation and the growth in the layer thickness are not only subject to the composition of the soldering alloy, but are also influenced by the metallisations of the bonding partners. The material combinations evolving from the soldering process influence the behaviour of the solder joint as a whole and have a particularly large (and complex) impact on how these properties change with different temperatures, duration and to mechanical stress. Any prediction of the likely technical life span of an electronic assembly, particularly if this assembly is about to be subjected to elevated temperatures, needs to be based upon a thorough test of the respective material combination, under the conditions in question.

The alternative solder alloys which were the subject of the present investigation, demonstrated better intermetallic phase growth properties and a superior resistance to fatigue when exposed to temperature cycling than the conventional lead-containing solder. The combination of loads, however, i.e. the exposure to heat and temperature shocks, caused an early failure of the joints made with the solder SnAg3.5. Initially, there was no sufficient explanation, and it was only on the basis of a metallographic analysis that these phenomena were understood. Depending on the conditions to which the solder joints are being subjected, different strengths and weaknesses of the alloys are revealed and become relevant. The assumption that SnAg-solders with their higher melting points are generally superior cannot be supported on the basis of these results. Higher operating temperatures favour the generation and acceleration of damage-causing mechanisms based on diffusion processes. Copper and nickel in conjunction with tin, once exposed to high temperatures, lead to an extraordinarily fast growth of intermetallic phases which can be observed in all their variety in the joint. The (fairly common) combination of Cu and Ni as a soldering terminal is a critical weak point of assemblies subjected to high temperatures.The Kirkendall effect which occurs in some material combinations is not less critical: diffusion-induced void growth makes the solder joint brittle and more likely to fracture – which it inevitably does, with or without mechanical stress.

It is barely possible to list all currently employed material combinations (metallisations on components and circuit-boards, soldering alloys with three or more ingredients) or their respective properties, and based on current development trends, one should not expect the number of materials involved in solder joints to decrease or become more standardised. The alternative lead-free solder alloys have not been as thoroughly researched as the lead-containing conventional solders such as SnPbAg2. Since legislation forbids the unrestricted use of lead beyond 1st July 2006, more research is required in this area. Meanwhile, the manufacturers of electronic assemblies are well advised to subject the material combinations of their products (defined by the components, the substrate, the solder, the resist, the adhesive etc.) to the same range of temperatures they are likely to encounter under full operational conditions, and to do this already at the development stage. This is the best way to establish their product reliability – and to avoid unpleasant surprises.

Representative Results of Work Module Integration

Rework Systems as an Economic Means to Qualify Components for Lead Free Soldering

From July 1st, 2006 the use of lead containing solder in electronic assemblies is restricted by RoHS (The Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment, European Directive 2002/95/EG). The world wide investigated alternative alloy system is close to the eutectic composition SnAg3.8Cu0.7, with melting point near 217°C. This is almost 40°C above the liquidus temperature of current near eutectic solder alloys, e.g. SnPb36Ag2. Therefore, higher temperatures are needed for the solder process for melting the solder alloy and wetting the contact surfaces. This poses higher heat resistance requirements on the components, beside the need to adapt to RoHS compliant compositions with regard to lead free contact finish and non brominated flame retardants. Unfortunately, the decomposition temperature of the industry standard polymer packages, plus the strong temperature dependence of the MSL (moisture sensitivity level) which classifies the danger of delamination during reflow soldering put a close upper limit to the process window. Revision B of JSTD-020 (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices. July 2002) describes this in terms of time allowed above liquidus (60-150 s) and maximum temperature not to be exceeded (225/245°C, solder with lead; 245/250°C, lead free solder, for large/small active components, respectively). In the discussion at moment is an extension of the upper temperature limit to 260°C for small components, provided that the moulding compounds and package design qualify for this.

Fabrication trials show that up-to-date manufacturing equipment is able for the higher process temperatures. Components are the key factor for the conversion to lead free electronics. The art of solder profiling is renewed for all running and new products, and the task is more delicate, as the process window is decidedly smaller. To shorten the down time on the production line, necessary for development of the component-compatible solder profile, Fraunhofer ISIT recommends to use computer controlled rework stations to test the solder heat requirement in an assembly, as well as the solder heat resistance. The close control of time and temperature is reproducible by temperature measurement and program development, exactly as in the procedure used in the mass reflow soldering process. In the Fraunhofer ISIT Rework Center, various brands of rework/repair equipment are

Figure 1a:
Solder profile for Sn62Pb36Ag2
3 min. to peak, ΔT at peak 17°C

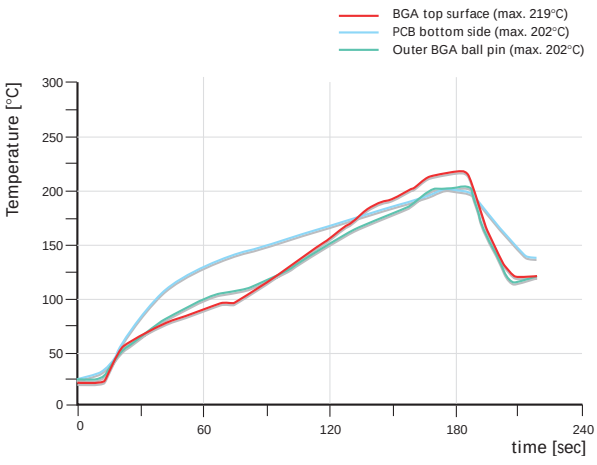
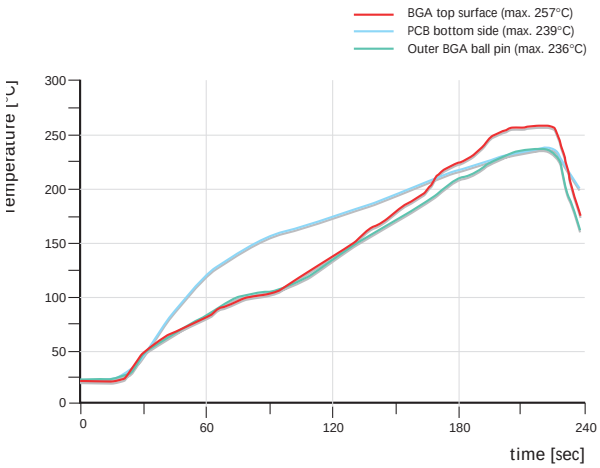


Figure 1b:
Solder profile for Sn95.5Ag3.8Cu0.7
3:30 min. to peak, ΔT at peak 21°C



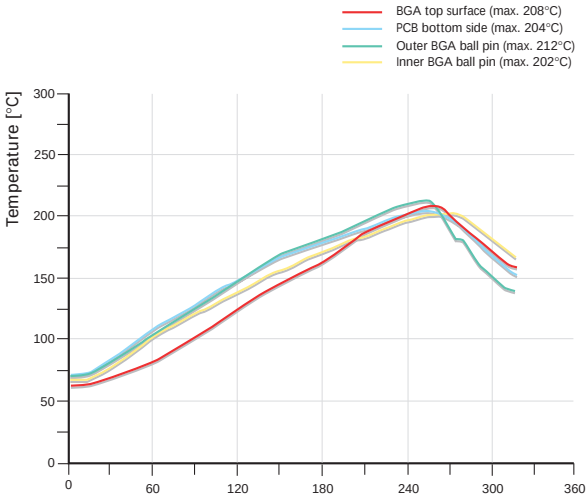


Figure 2a:
Solder profile for Sn62Pb36Ag2
4:15 min. to peak, ΔT at peak 10°C

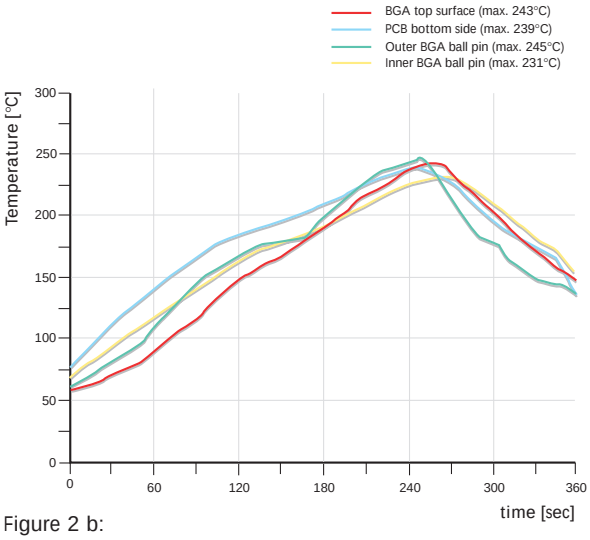
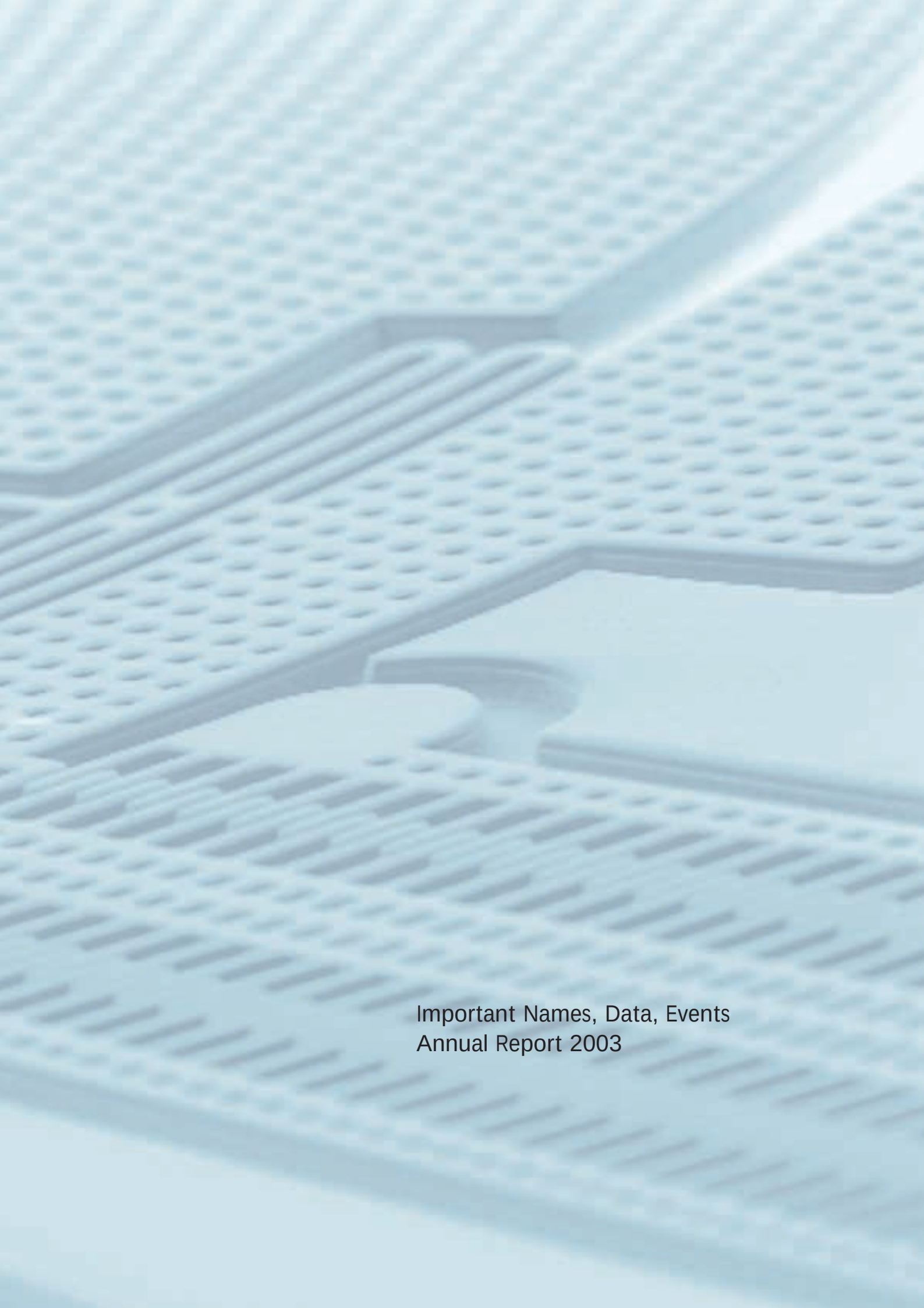


Figure 2 b:
Solder profile for Sn95.5Ag3.8Cu0.7
4:30 min. to peak, ΔT at peak 14°C

used in the sense of selective reflow soldering systems. Hot gas systems, infrared systems and mixed systems are used for customer specific tasks, e. g. desoldering and soldering of high pin count active devices. The resulting solder joint quality is tested non destructive by optical inspection, microfocus x-ray, and electrically, if applicable. For process window verification, microsections show the metallurgical integrity of solder joints, components and circuit boards to make sure that the solder profile was within the limits.

As an example, temperature profiling results are shown in the four images provided here. They were produced on a hot gas system which can be operated with nitrogen or air. Hot gas is provided through a large diffuser from the bottom, and through a component-specific nozzle from the top. The nozzle acts also as desoldering and as a placement tool. Figures 1a and b show short solder profiles, measured with thermocouples on different spots around a P-BGA292 (Plastic Ball Grid Array) component; compared are a profile for lead containing solder (1a) and a lead free solder (1b). The task was to remain below 260°C on the component package top side. In this case, the difference between the coldest and hottest measured spot on the component (ΔT) is 17°C with lead (1a), and 21°C without lead (1b). Figures 2a and b show the resulting solder profiles, after the task was modified to remain below 245°C package body temperature. In this case, as the process window is reduced with regard to the upper temperature limit, the ΔT must be smaller. To leave more time for temperature equilibration, the profiles must be extended to times well above 4 min., gaining a smaller ΔT of 10°C with lead (2a) and 14°C without lead (2b). As a matter of fact, comparing 1b and 2b, the ΔT between the outer BGA pin and the BGA top surface has decreased from 21°C to 2°C, however on the cost of almost 1 min. extension of the solder process time.

Practising solder profiling like in this example on rework equipment takes ca. one hour per profile, provided all systems including profiler and thermocouples are set up properly. The results can serve directly as experience with new components or a new technology, such as “lead free” for the line production process, without interrupting the production. ISIT offers this kind of test as a service to customers, but provides also training on the various rework systems to enable R&D as well as production personnel to make best use of the equipment on the production floor.



Important Names, Data, Events
Annual Report 2003

Lecturing Assignments at Universities

H. Bernt:
Halbleitertechnologie I und II, Technische Fakultät der Christian-Albrechts-Universität, Kiel

A. Heuberger:
Lehrstuhl für Halbleitertechnologie, Christian-Albrechts-Universität, Kiel

Memberships in Coordination Boards and Committees

T. Ahrens:
Coordinator of AOI-Anwenderkreis (Automated Optical Inspection)

T. Ahrens:
Member of DVS Fachausschuss Löten

T. Ahrens:
Member of DVS Fachausschuss Mikroverbindungstechnik

T. Ahrens:
Member of Hamburger Lötzirkel

W. H. Brünger:
Member of Steering Committee: Electron, Ion and Photon Beams and Nanofabrication, EIPBN, USA

W. H. Brünger:
Member of VDI Fachausschuss: Maskentechnik, VDI, Düsseldorf

W. H. Brünger:
Section Head: Micro and Nano Engineering, MNE 03, Grenoble

J. Eichholz:
Member of MEMSTAND Workshop International Steering Committee

T. Harder:
Member of European Network ˝Adhesives in Electronics˝

A. Heuberger:
Advisory Editor of International Journal of Semiconductor Manufacturing Technology; Microelectronic Engineering

A. Heuberger:
2. Chairman of an International Conference on Micro Electro, Opto, Mechanic Systems and Components

K. Pape:
Member of VDI Fachausschuss Assembly Test, VDI, Frankfurt

K. Pape:
Member of BVS, Bonn

K. Pape:
Member of FED

W. Reinert
Member of Arbeitskreis A 2.4 Drahtbondtechnik, DVS

M. Reiter:
Member of Gf Korr "Arbeitskreis Korrosionsschutz in der Elektronik"

M Reiter:
Member of "Arbeitskreis Lotpasten"

M Reiter:
Member of "Arbeitskreis Bleifreie Verbindungstechnik in der Elektronik"

M Reiter:
Member of "Industrie-Arbeitskreis Know-How-Transfer mikrotechnischer Produktion"

G. Zwicker:
Head of Fachgruppe Planarisierung/ Fachausschuss Verfahren/ Fachbereich Halbleitertechnologie und -fertigung der GMM des VDE/VDI

Distinctions

"Best Paper Award 2002" for:
F. Hofmann, A. Frey, B. Holzapfl, M. Schienle, C. Paulus, P. Schindler-Bauer, R. Hintsche, E. Nebling, J. Albers, W. Gumbrecht, R. Thewes: "Passive DNA Sensor with Gold Electrodes Fabricated in a CMOS Backend Process" ESSDERC 2002 (European Solid-State Device Research Conference), Firenze, Italy, September 24 – September 26, 2002

"ISSCC 2002 Jack Raper Outstanding Technology Directions Paper Award" for:
R. Thewes, F. Hofmann, A. Frey, B. Holzapfl, M. Schienle, C. Paulus, P. Schindler, G. Eckstein, C. Kassel, M. Stanzel, R. Hintsche, E. Nebling, J. Albers, J. Hassmann, J. Schuelein, W. Goemann, W. Gumbrecht: "Sensor Arrays for Fully-Electronic DNA Detection on CMOS" ISSCC 2002, Session 21-Sensors and Microsystems, San Francisco, USA, November 2002

Cooperation with Institutes and Universities

Aalborg University, Denmark

Cranfield University, Bedford, UK

Euspen, Bedford, UK

Hahn-Meitner-Institut, Berlin

Technische Universität Braunschweig, Fachbereich Elektrotechnik, Institut für Elektrophysik

Technische Universität Braunschweig, Institut für medizinische Informatik

Technical University of Budapest, Department of Electronic Technology, Ungarn

Cambridge University, UK

Applied Microengineering Ltd. (AML), Didicot, UK

Rutherford Appleton Laboratories, Didicot, UK

Technische Universität Dresden, Institut für Halbleiter- und Mikrosystemtechnik

EMPA, Dübendorf, Schweiz

VTT, Espoo, Finnland

Fachhochschule Flensburg

University of Gdansk, Polen

University of Greenwich, UK

Ernst-Moritz-Arndt-Universität (EMAU), Greifswald

CEA Leti, Grenoble, France

Max-Planck-Institut für Mikrostrukturphysik, Halle

Universitätskrankenhaus Eppendorf, Hamburg

Universität Hamburg, Abteilung für Biochemie und Molekularbiologie

Universität der Bundeswehr, Hamburg
Fachhochschule Westküste, Heide

University of Technology, Helsinki, Finland

Technische Universität, Ilmenau Institut für Fügetechnik und Werkstoffprüfung (IFW), Jena

Christian-Albrechts-Universität, Technische Fakultät, Kiel

Fachhochschule Kiel

École Polytechnique Fédérale de Lausanne, Switzerland

IMEC, Leuven, Belgien

University of Linkoeping, Sweden

University of Southern California, Los Angeles, USA

Fachhochschule Lübeck

CNRS-Université Claude Benard, Lyon, France

Max Planck Institut für Polymerforschung, Mainz

Universität, Madrid, Spanien

Institut für Diabetesforschung, München

Technische Universität München

CSEM, Neuchâtel, Schweiz

SINTEF, Oslo, Norway

Universität Oulu, Finland

Universtity of Pavia, Italy

University of Perugia, Italy

Sevola Superiore, San´t Anna, Pisa, Italy

Telemark University College, Porsgrunn, Norway

Royal Institute of Technology (KTH), Stockholm, Sweden
NPL, Teddington Middlesex, UK

VDI/VDE-Technologenzentrum Informationstechnik, Teltow

Fachhochschule Wedel

Technische Universität Wien, Austria

Trade Fairs and Exhibitions

Semicon Europe 2003.
April 1 – April 3, 2003, München

Hannover Messe 2003.
Forum Micro Technology: World Fair for Applied Microsystems and Nanotechnology.
April 7 – April 12, 2003, Hannover

SMT Hybrid Packaging 2003.
System Integration in Micro Electronics, Exhibition and Conference, May 6 – May 8, 2003, Nürnberg

Sensor 2003.
11th International Trade Fair and International Congress.
May 13 – May 15, 2003, Nürnberg

IMAPS 2003. 14th European Microelectronics and Packaging Conference & Exhibition.
June 23 – June 25, 2003

6th China International Battery.
Raw Material, Producing Equipment and Battery Parts Fair.
October 15 – October 17, 2003, Exhibition Center, Shanghai, China

Productronica 2003.
15th International Trade Fair for Electronics Production, November 11 – November 14, 2003, München

Miscellaneous Events

Baugruppenfertigung mit Schwerpunkt im Lötprozess
FED-Baugruppen-Seminar. VDI-Haus, January 31, Stuttgart; May 13, München; September 18, Ludwigsburg; December 4, Bonn, 2003

Inspektion in der Baugruppenfertigung
Seminar. February 19 – February 20, 2003, ISIT, Itzehoe

Der Lötprozess in der Fertigung elektronischer Baugruppen
Seminar. March 24 – March 26, September 29 – October 1, 2003, ISIT, Itzehoe

10. CMP Users Meeting
April 4, 2003, Amazeum, Munich

SMT-Rework-Praktikum
Seminar. April 8 – April 10 and November 4 – November 6 , 2003, ISIT, Itzehoe

Manuelles Löten von SMT-Bauelementen
Seminar. April 8 – April 10 and November 4 – November 6, 2003, ISIT, Itzehoe

Mobiles-Rework-Praktikum
Seminar. June 4 – June 5, 2003, ISIT, Itzehoe

ISIT-, Vishay-Presentation at Tag der beruflichen Bildung
organized by Berufliche Schule des Kreises Steinburg.
June 24, 2003, Itzehoe

ISIT-Presentation at 4th Hamburger Venture Lounge
Mikrosystemtechnik/Nanotechnologie September 17, 2003 ISIT Itzehoe

ISIT Presentation at Halbleiter-Industrie 2003
Seminar. 7. Handelsblatt Jahrestagung.
September 29 –September 30, 2003, Berlin

11. CMP Nutzertreffen
October 17, 2003, ISIT, Itzehoe

Scientific Publications

Journal Papers and Contributions to Conference

T. Ahrens, H. Schimanski, J. Pontow, D. Prochota: Bleifreies Reparaturlöten – Lötprofil an erster Stelle. DVS-Berichte Band 227, DVS-Verlag, p. 64, Düsseldorf, 2003

J. Albers, T. Grunwald, E. Nebling, G. Piechotta, R. Hintsche: Electrical Biochip Technology – A Tool for Microarrays and Continuous Monitoring. Anal. Bioanal. Chem., October, 377(3): 521-7.,Electronical Pub. Review, August 30, 2003

H. Bell, M. H. Poech, C. John: Temperaturprofile für das Reflowlöten. Elektronik Produktion & Prüftechnik, EPP 6/7, p. 24, 2003

W. H. Brünger, J. Eichholz, H. Hanssen, D. Friedrich: Fabrication and Electrical Characteristics of Carbon Nanotube-Based Microcathodes for Use in a Parallel Electron-Beam Lithography System. Journal Vacuum Society, B 21(2), March – April 2003,

T. Diersing, R. Feuerstein, E. Gailing, H. Göpel, R. Holzmann, T. Kiel, K. Pape, H. Roth, L. Tschimpke: Einfluss von bleifreiem Lot auf den Test elektronischer Baugruppen – Teil 1. Produktion von Leiterplatten und Systemen, E. Leuze Verlag, p. 1527 – 1532, Bad Saulgau, October, 2003

T. Diersing, R. Feuerstein, E. Gailing, H. Göpel, R. Holzmann, T. Kiel, K. Pape, H. Roth, L. Tschimpke: Einfluss von bleifreiem Lot auf den Test elektronischer Baugruppen – Teil 2. Produktion von Leiterplatten und Systemen, E. Leuze Verlag, p. 1766 – 1770, Bad Saulgau, November, 2003

R. Dudde, Th. Vering: Advanced Insulin Infusion Using a Control Loop (ADICOL). Proceedings 4th Intl. IEEE EMBS Conference on IT Applications in Biomedicine, ITAB, p. 280, 2003

T. Harder: Low Profile and Flexible Electronics Assemblies Using Ultra-Thin Silicon - The European Flex-Si Project. In Foldable Flex and Thinned Silicon Multichip Packaging Technology, ed. John W. Balde, Kluwer Academic Publishers, 2003

P. Merz, H. J. Quenzer, H. Bernt, B. Wagner, M. Zoberbier: A Novel Micromachining Technology for Structuring Borosilicate Glass Substrates. 12th International Conference on Solid – State Sensors, Actuators and Microsystems, Proceeding of Transducers '03, Boston, USA, Vol. 1, p. 258 – 261, 2003

P. Merz: Herstellung von mikrostrukturierten Oberflächen in Glas und Polymer durch replikative Verfahrenstechnologien. Berichte aus der Mikrosystemtechnik, ISBN 3-8322-1628-6, Shaker Verlag, Aachen, 2003

M. Nowottnick, U. Pape, S. Wege, T. Lauer, T. Ahrens: Die Lötbarkeit bleifreier Lotlegierungen (SnCu, SnAgCu) im Vergleich zu konventionellen Loten. DVS-Berichte Band 227, DVS-Verlag, p. 44, Düsseldorf, 2003

H.J. Quenzer, K. Reimer, P. Merz: Three-Dimensional Micro-Structuring for Optical Applications Proc. DGG Symposium Processing and Applications of Optical Components, Glass Sci. Technol. 76 C2, 13-22, Leipzig, 2003

A. Spiegel, W. H. Brünger, C. Dzionk, P. Schmuki: Resistless Deposition of Metallic Nanostructures on Ion Projection Sensitized p-Si. Microelectr. Eng., 67-68, p. 175, 2003

A. Spiegel, W. H. Brünger, C. Dzionk, P. Schmuki: Ion Projection Sensitized Selective Cu Electroplating on Uncoated p-Si. J. Vac. Sci. B, 20, 2713, November – December, 2002

Talks and Poster Presentations

T. Ahrens: AOI-Test. Seminar: Technologien für die elektronische Baugruppe, Colonia de Sant Jordi, Mallorca, March 19 – March 23, 2003

T. Ahrens: Lötqualität. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, March 24 and September 29, 2003

T. Ahrens: Baugruppen- und Fehlerbewertung. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, March 25 and September 30, 2003

T. Ahrens: Metallurgie der Lötstelle. Seminar: Manuelles Löten von SMT-Bauelementen, ISIT, Itzehoe, April 8 and November 4, 2003

T. Ahrens: Leadfree Alloys for Soldering. ATV-SEMAPP Workshop on Leadfree Soldering, Odense, Denmark, April 30, 2003

T. Ahrens: Stress Conditions, Failure Modes and Reliability. Workshop on Leadfree Soldering, Odense, Denmark, April 30, 2003

T. Ahrens: Bleifrei Löten. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, October 1, 2003

T. Ahrens: Die Lötbarkeit bleifreier Lotlegierungen (SnCu, SnAgCu) im Vergleich zu konventionellen Loten. Seminar: Bleifreies Löten, Ergebnisse aus der aktuellen Forschung, DVS, Wirges/Westerwald, December 3, 2003

T. Ahrens, H. Schimanski: Selektives Löten. EUREKA-Sitzung, Leadfree E, EMPA, Dübendorf, Switzerland, March 27 - March 28, 2003

T. Ahrens, H. Schimanski: Rework-Stationen für komplexe SMT-Baugruppen. Seminar: Mobiles-Rework-Praktikum, ISIT, Itzehoe, June 4, 2003

T. Ahrens, H. Schimanski: Qualitätsbewertung der Lötverbindungen. Seminar: Mobiles-Rework-Praktikum, ISIT, Itzehoe, June 5, 2003

T. Ahrens, H. Schimanski, J. Pontow, D. Prochota: Bleifreies Reparaturlöten – Lötprofil an erster Stelle. Seminar: Bleifreies Löten, Ergebnisse aus der aktuellen Forschung, DVS, Wirges/Westerwald, December 3, 2003

W. H. Brünger: Direkte Strukturierung von Oberflächen durch Ionenprojektion. Wissenschaftliche Fachtagung: Schwerionen als Werkzeug, Wernigerode, May 12 – May 13, 2003

W. H. Brünger: Ion Projection Direct Structuring of Surfaces. Max Planck Institut für Polymerforschung, Mainz, July 3, 2003

W. H. Brünger: Ion Projection Lithography, Technology and Applications. EU-Workshop: Modifications Following Different Interaction Processes at Surfaces, San Sebastian, Spain, September 8 – September 13, 2003

V. Dharuman, E. Nebling, J. Albers, R. Hintsche, S. Deckers, E. Spillner, R. Bredehorst, L. Blohm, T. Grunwald: Nanoskalige elektrische Messverfahren für portable Analysesysteme niedermolekularer Verbindungen. BMBF Symposium Nanobiotechnologie, Hannover, BIOTECHNICA, October 7 – October 8, 2003

R. Dudde: EUROPRACTICE Microsystems, Microsystem Development, Device Design and Production. Forum VDI/VDE, Hannover Messe, April 10 – April 11, 2003

Diploma Theses

D. Friedrich:
Silizium-Hochratenätzen zur Herstellung tiefer Trenches für Super-Junction-Strukturen in der Hochvolt-PowerMOS Anwendung. DFG Abschluss-Kolloquium "Halbleiterbauelemente hoher Leistung", Aachen, September 24, 2003

T. Grunwald, A. Paul, T. Pommerencke, E. Spillner, L. Blohm, J. Albers, R. Bredehorst, R. Hintsche:
Electrical Biochips in Protein Analytics – Highly Sensitive Detection of Biowarfare Toxins. Dechema Status-Seminar Chiptechnologien, Campus Westend, Universität Frankfurt am Main, February 24 – February 25, 2003

T. Harder:
Introduction to Ultra-Thin Si Packaging and the European IST Projects FLEX-SI and FLIBUSI. Workshop Ultra Thin Silicon Packaging, Semicon Europe, München, April 1 – April 3, 2003

A. Heuberger:
Technologische Innovation im Bereich Steuerung und Elektronik. Workshop: Stiftung "Brandenburger Tor", Bankgesellschaft Berlin, May 13, 2003

A. Heuberger:
Rolle und Inhalt staatlich geförderter Innovationsforschung – aus Sicht von Forschungsinstituten. Workshop Stiftung "Brandenburger Tor", Bankgesellschaft Berlin, October 15, 2003

W. Pilz:
Microsystem Technology at Fraunhofer ISIT. Micro Techcafé, Oslo, April 3, 2003

M. H. Poech:
Das Reflow-Lötprofil. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, March 24 and September 29, 2003

M. H. Poech:
Modellierung der thermischen Vorgänge im Reflow-Lötprozess. Seminar: 16. Treffen des Arbeitskreises "Bleifreie Verbindungstechnik in der Elektronik", TUB Forschungsschwerpunkt Technologien der Mikroperipherik/ Fraunhofer IZM, Berlin, December 2, 2003

K. Reimer:
Micro Plastic – Competence Cluster, Kostengünstige Herstellung von Mikrosystemen: Verbundtechnik von Kunststoff und Silizium Vitamin W. Mikrotechnologie in der Produktionstechnik, TZL Lübeck, August 26, 2003

W. Reinert:
Packaging of Ultra-Thin Chips. Workshop: Ultra Thin Silicon Packaging, Seminar: Semicon Europe, München, April 1 – April 3, 2003

W. Reinert, T. Harder, H. Schimanski, L. Bertels, M. Zoberbier:
Wafer-Level Encapsulation of MEMS Using Solder Sealing. Micro System Technologies, München, October 7 – October 8, 2003

M. Reiter:
Bleifreies Löten. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, March 26 and October 1, 2003

H. Schimanski:
Qualitätsfaktor Leiterplatten. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, March 25 and September 30, 2003

H. Schimanski:
Rework-Strategien. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, March 26 and September 30, 2003

H. Schimanski:
Reparatur komplexer SMTBaugruppen. Seminar: Manuelles Löten von SMT-Bauelementen, ISIT, Itzehoe, April 8 and November 4, 2003

H. Schimanski:
Rework Strategien für bleifreies Wellenlöten. Seminar: 15. Fachforum Produktion elektronischer Baugruppen, Würzburg, ' May 20 – May 21, 2003

H. Schimanski:
Rework-Strategien im bleifreien Prozess. Bleifreitechnologietage bei ERSA, Kreuzwertheim, May 20 – May 21, 2003

H. Schimanski:
Laserlöten von Silizium/Glas mittels Glaslot zur Kapselung von Mikrosensoren auf Waferebene. Poster, 77. Glastechnische Tagung, DGG, Leipzig, May 26 – May 28, 2003

H. Schimanski, T. Ahrens:
Reparatur von Lötstellen. Seminar: Neuntes Fachforum Otti Technik Kolleg, Regensburg, October 21 – October 22, 2003

O. Schwarzelbach:
Design Service and Software Solutions to Enhance the Access to MEMS Foundries. Bosch-Foundry-Workshop-Day, Reutlingen, June 5 – June 6, 2003

C. Werlich:
Arbeitsprinzipien mit AOI-Systemen. Seminar: Inspektion in der Baugruppenfertigung, ISIT, Itzehoe, February 19, 2003

G. Zwicker:
MEMS Fabrication by Using CMP. 10. CMP User Meeting, Amazeum, Munich, April 4, 2003

A. Heuberger:
Technologische Innovation im Bereich Steuerung und Elektronik. Workshop Stiftung "Brandenburger Tor", Bankgesellschaft Berlin, May 13, 2003

A. Heuberger:
Rolle und Inhalt staatlich geförderter Innovationsforschung – aus Sicht von Forschungsinstituten. Workshop Stiftung "Brandenburger Tor", Bankgesellschaft Berlin, October 15, 2003

G. R. Aloise:
Development of Boron Doping and Trench Filling Processes for a Superjunktion Based Diode. Christian-Albrechts Universität Kiel, September, 2003

R. Buchner:
Entwicklung und Charakterisierung eines HF-Gasphasen-Ätzprozesses. Technische Universität Carolo-Wilhelmina, Braunschweig, March, 2003

R. Hübner:
Anforderungen an Prüfstrukturen für automatische optische Inspektionssysteme in der Fertigung elektronischer Baugruppen. Fachhochschule Wedel, February, 2003

H. Jacobsen:
Evaluierung von Slurries in einem CMP Prozess. Fachhochschule Wedel, February, 2003

O. Lawin:
Automatisierung einer Benetzungs – Kraft – Messung mit optischer Inspektion. Fachhochschule Westküste, Heide, September, 2003

M. Pawelzik:
Charakterisierung von mikromechanischen kapazitiven Hochfrequenzschaltern. Fachhochschule Westküste, Heide, May, 2003

T. Pommerencke:
Konfiguration und Automatisierung eines Messsystems zur Toxindetektion mittels elektrischer Biochips. Hochschule für Angewandte Wissenschaften (HAW), Hamburg, March, 2003

Overview of Projects

- Prozesse/ Verfahren für die Herstellung ultradünner Trench-IGBTs auf sub-100µm Silizium-Substraten
- Entwicklung einer UBM/BCB Technologie für Wafer Level Packaging
- Fabrication of Si-Microstructures based on SOI-Wafers
- Prozessentwicklung und Unterstützung bei der Produktion von Philips-Wafern
- Entwicklung von Super-Junction-Strukturen für Hochvolt-PowerMOS-Anwendungen
- Prozessierung von Wafern mittels Silizium-Trockenätzen zur Erzeugung spezieller Si-Strukturen
- Fabrication of Capacitor Structures
- Herstellung von Nanostrukturen in Siliziumnitrid
- Einsatz der Ionen-Projektions-Lithographie im Fertigungsprozess für die kontaktlose Strukturierung planarer magnetischer Speichermedien
- P-ML 2, Projection Maskless Lithography; Development of an Aperture Plate System
- Arrays of Microguns for Parallel e-beam Nanolithography, NANOLITH
- Entwicklung von Post-CMP-Reinigungsprozessen für die Fertigung von zukünftigen integrierten Schaltkreisen in der Si-Technologie
- Evaluierung von Slurries zum chemisch-mechanischen Polieren von SiO2
- Schleifen und Rückseitenpolieren von Wafern für MEMS-Anwendungen
- Maskenentwurf für „Integrated Discretes“
- Untersuchung an mikromechanischen Drehraten-Sensoren
- Entwicklung eines mikromechanischen Luftmassensensors
- Entwicklung eines in Siliziumtechnologie hergestellten pneumatischen 3/2-Wege-Mikroventils
- European Access to Manufacturing Service for MEMS on SOI Micromachining Technologies
- Herstellung und Replikation von großflächigen 3D-Nano- und Mikrostrukturen, NanoFab
- Entwicklung von kapazitiven HF-Schaltern
- Musterfertigung von Blendenkarten mit Soft-Blenden
- Fertigung eines Spiegelarrays mit elektrischem Anschluss und Beurteilung der Mikrospiegeltechnologie
- Herstellung von Kalibriermustern zur Messung des Polarisationszustandes emittierter IR-Strahlung
- Entwicklung von piezoelektrischen Schichten für Si-Mikroaktuatoren
- Design schaltbarer optischer Netze
- Fabrication, Assembly and Testing of a Miniature Two-Axis Laser Scanner and a High Voltage Amplifier
- Kostengünstige Herstellung von Mikrosystemen: Verbundtechnik von Kunststoff und Silizium (MP-CC)
- Entwicklung eines hochdruckfesten Drucksensors
- Herstellung mikrooptischer Linsenarrays aus Glas
- Herstellung mikrooptischer Linserarrays in Polycarbonat
- Entwicklung eines Wasserstoffsensors
- Electric DNA Chips for Bioprocess Control
- Silizium-Chipsystem für die biochemische Analysentechnik: Technologische Plattform und Systemintegration Teilvorhaben: Messverhalten und biochemische Assays
- Silizium-Chipsystem für die biochemische Analysentechnik: Technologische Plattform und Systemintegration, Teilvorhaben: Testchips und Testverhalten
- Entwicklung von Ultramikroelektrodenarrays und Integration in ein automatisiertes fluidisches Analysesystem
- Nanoskalige elektrische Messverfahren für portable Analysesyteme niedermolekularer Verbindungen
- Aufbau einer technologischen Plattform zur Erregerdiagnostik mit Elektrischen Biochips (TTZ Kiel)
- Online Programmierung komplexer Biosysteme in rekonfigurierbarer bioelektronischer Hardware BMBF-Verbundprojekt BioPro
- intelligent Controll Assistent for Diabetes, INCA
- Microsystem Manufacturing Cluster, EUROPRACTICE AMICUS
- Customer Support and Design Centre for Physical Measurement Systems, EUROPRACTICE CCMeSys
- Microactuator Competence Centre, EUROPRACTICE CCMicro
- Laserlöten von Silizium-Pyrex mittels Glaslot zur Kapselung von Mikrosensoren
- Bonden mit Cu-Draht in der Leistungselektronik
- Chipkartenbestückung mit Grautonblenden
- Ultra-Thin Packaging Solutions using Thin Silicon
- Flip Chip Die Bonder for Ultra-Thin Silicon
- Alternatives Löten von Mikrobausteinen
- Untersuchung zur Unterfüllung von Bauteilen mit flächig verteilten Lötanschlüssen in der Oberflächenmontagetechnik, CSP Underfill
- Long-Term Stability of Vacuum-Encapsulated MEMS Devices Using Eutectic Wafer Bonding, VABOND
- Federating a Packaging and Interconnection Transeuropean Industrial Activity, PATRIA
- Stressarme Montage von Sensoren und Mikrooptik – Komponenten mittels Mikroklebtechnik
- Entwicklung eines marktfähigen Micro-Drehgebers zur absoluten Winkelcodierung nach dem Prinzip der optischen Abtastung, Centro, BMBF
- Evaluation of packaging concepts for the gyro-sensor, Gyrosil, BMBF
- Fertigung von Testwafern zur Justierung von Bestückungsanlagen
- Bleifreies Wellenlöten, EUREKA
- Herstellung porenarmer Weichlötverbindungen
- Reflow und Wellenlöten mit bleifreien Loten
- Die elektronische Baugruppe der Zukunft
- Stressoptimierte Montage und Gehäusetechnik für mikromechanisch hergestellte Silizium-Drehratensensoren
- Bleifrei-Eigenschaften des Reflow-Lotes SnAg 3,9 Cu 0,6 und des Wellen-Lotes SnCu 0,7
- Ag thick Film Bumping on Wafer Level
- Entwicklung einer AOI Kalibrierprobe
- Einfluss von Poren auf die Zuverlässigkeit von Weichlötverbindungen
- Whiskerbildung an Zinnoberflächen und Sprödbruch an Nickel-/Gold Oberflächen für bleifreie Lötverbindungen
- Thin Wafer Handling for Backsite Processing
- Festkörper-Lithiumakkumulatoren
- Entwicklung von hochzyklenfesten Li – Festkörper – Polymerakkumulatoren mit einstellbarer, konstanter Ausgangsspannung
- Hearing – Aids with Rechargeable Power Supply, HARPOS

Patents

W. Benecke, B. Wagner,
R. Hagedorn, G. Fuhr, T. Müller:
Method of Continuously
Separating Mixtures of Microscopic
Dielectric
Particles and Apparatus for
Carrying Through this Method
JP 3453136

P. Birke, F. Salam-Birke:
Films for Electrochemical
Components and a Method for
Production Thereof
TW 172250

W. H. Brünger:
Method of Examining and/or
Modifying Surface Structures of a
Sample
US 006661005B1

J. Eichholz, H.-J. Quenzer,
P. Staudt-Fischbach:
Verfahren zur Herstellung einer
digitalen Gatterschaltung mit
herabgesetztem Querstrom
DE 19819867

J. Eichholz:
Verfahren und Schaltungsvor-
richtung zur Ansteuerung einer
Mehrzahl von Schaltungen
DE 1293042

F. Heinrich, U. Bänziger:
Vorrichtung zur großflächigen
Plasmaerzeugung
DE 19548657

U. Hoffmann, M. Witt,
B. Wagner, S. Mühlmann:
Kippbarer Mikrospiegel und
Verfahren zur Herstellung
EP 1081528

J. Janes:
Verfahren zur Herstellung eines
optischen MxN-Schalters
DE 10148276

T. Lisec, H. J. Quenzer,
B. Wagner:
Microvalve
JP 3418741

T. Lisec, B. Wagner:
Michromechanic Pump
EP 1179139
Micromechanical Pump
US 6,655,923