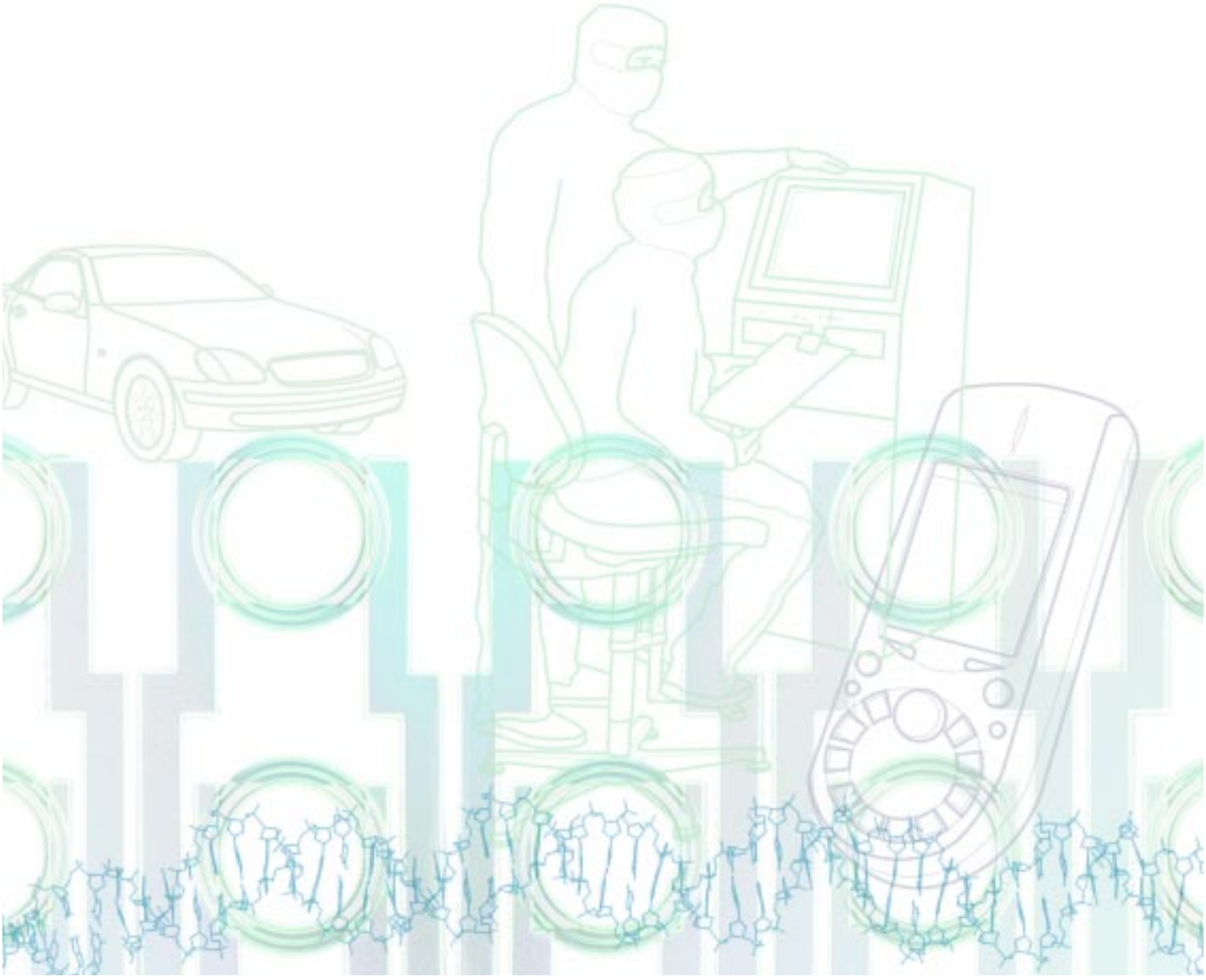
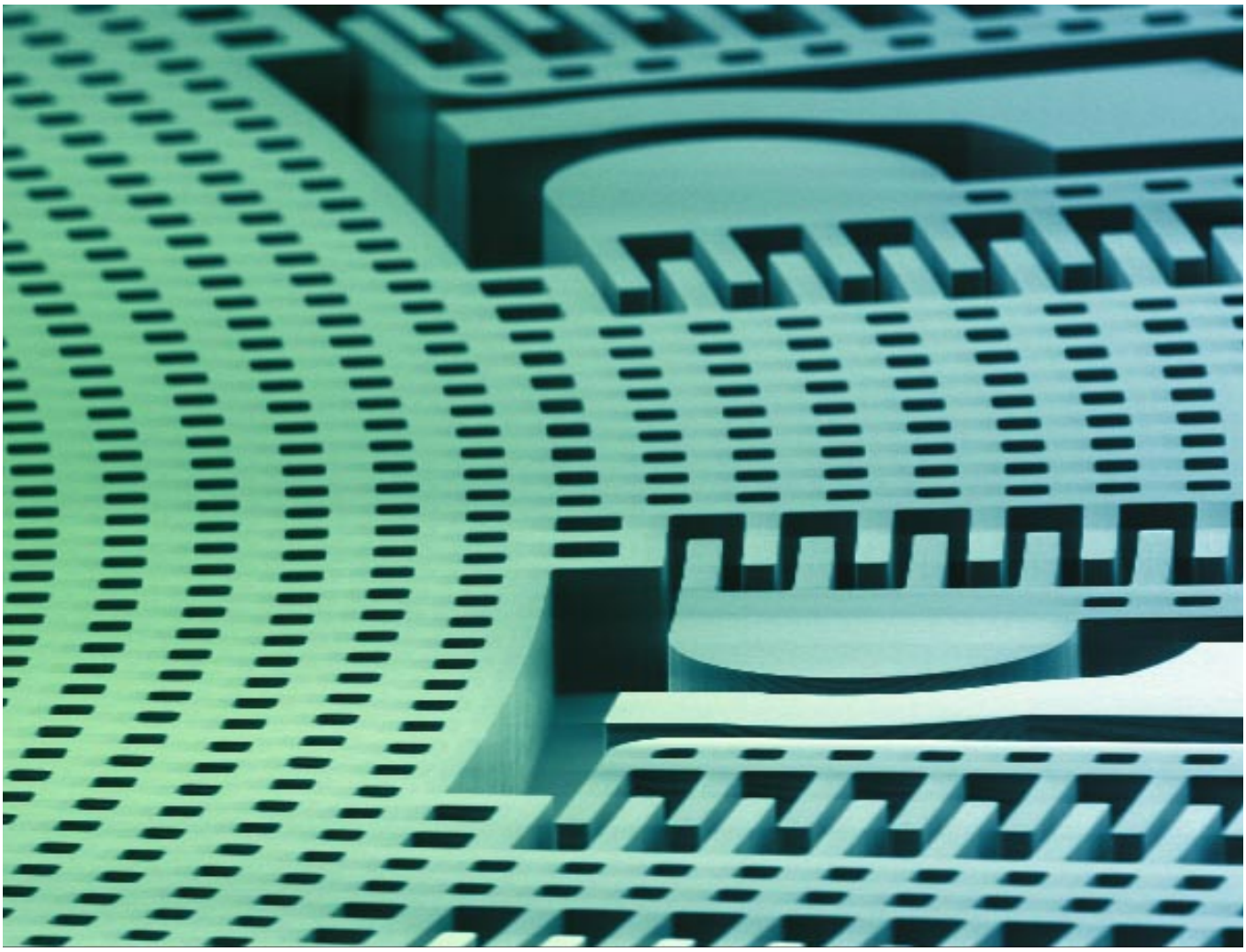
ISIT

Fraunhofer Institut Siliziumtechnologie

Achievements and Results
Annual Report 2004





Surface micromachined polysilicon
structure for inertial sensing.

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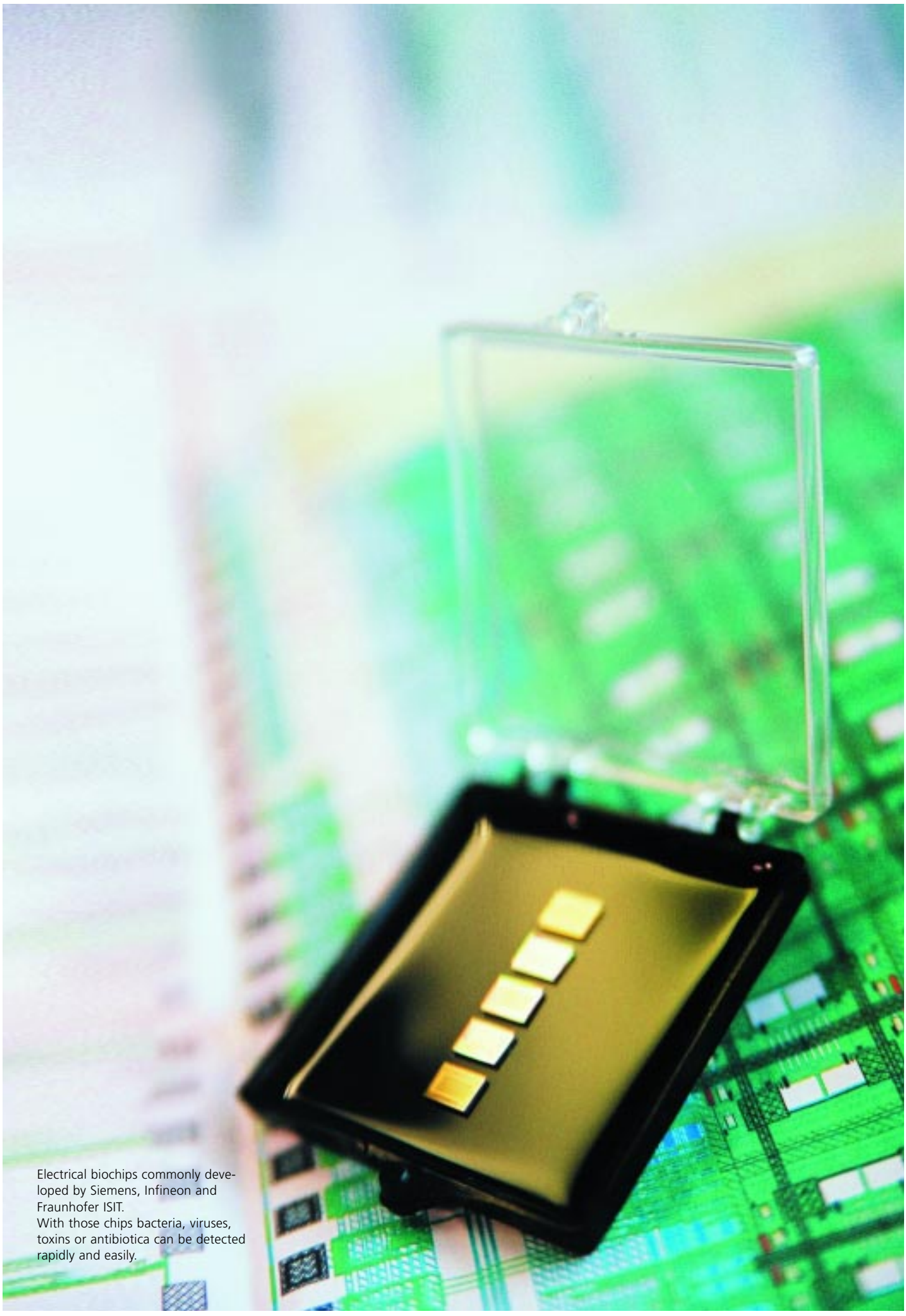


Electrical biochips commonly developed by Siemens, Infineon and Fraunhofer ISIT.
With those chips bacteria, viruses, toxins or antibiotica can be detected rapidly and easily.

Preface

2004 was a year of noteworthy decisions for the further development of Itzehoe as a high-tech research and manufacturing address.

By far the most important of these was the decision by Vishay/Siliconix to build their first production line for power components on 8" (200-mm) wafers in Itzehoe, after having considered a number of other sites outside Germany. This decision confirms the high quality of the infrastructure in Itzehoe and the excellent skills and motivation of the workforce at Vishay Semiconductor Itzehoe and the staff of Fraunhofer ISIT.

These facility modernization plans were able to go ahead because Vishay and ISIT, in consultation with the BMBF, were quickly able to agree on terms for the renewal of their cooperation agreement. A contract has been negotiated for a period of ten years, following on from the present cooperation agreement which is due to expire in 2007. This safeguards the future of the Itzehoe site, with the known example of cooperation between a research laboratory site and manufacturers, for many years to come.

Over the next three years, Vishay and ISIT intend to invest around € 100 million in order to upgrade their manufacturing plant to deal with the larger-diameter wafers, and to increase production capacity. The workforce will grow by around 100 employees. Vishay will carry well over half of the necessary investment, and also provide the most new jobs. It is appropriate at this point to express our very grateful thanks to the Schleswig-Holstein Ministry of Economy, and most particularly to Professor Rohwer and Dr. Ross, who have given us their support in many ways. With these new facilities, Itzehoe is well on the way to becoming the center of Vishay/Siliconix's R&D activities in the field of new power components.

The transition to the new wafer size makes Itzehoe a world pioneer in the development and manufacturing of power electronics and microsystems components. – There are nowhere else any significant activities using 8" wafers in these particular areas of microengineering. The production of microsystems on 8" wafers calls for an exceptional degree of stability in the engineering parameters, not only with respect to electrical properties but also in mechanical terms, and thus represents a huge technological challenge. In this context we would like to thank the BMBF (nanoelectronics department) for their technical and financial support.

A further important milestone in the realization of the ISIT's concept for developing closer links between R&D and manufacturing was reached in 2004 in cooperation with SILICON Manufacturing Itzehoe (SMI). The outlines of a contract have been drafted that will enable SMI and ISIT to collaborate in the field of microsystems engineering in much the same way as Vishay and ISIT now work together in the field of power electronics. In other words, ISIT will concentrate on the development of new

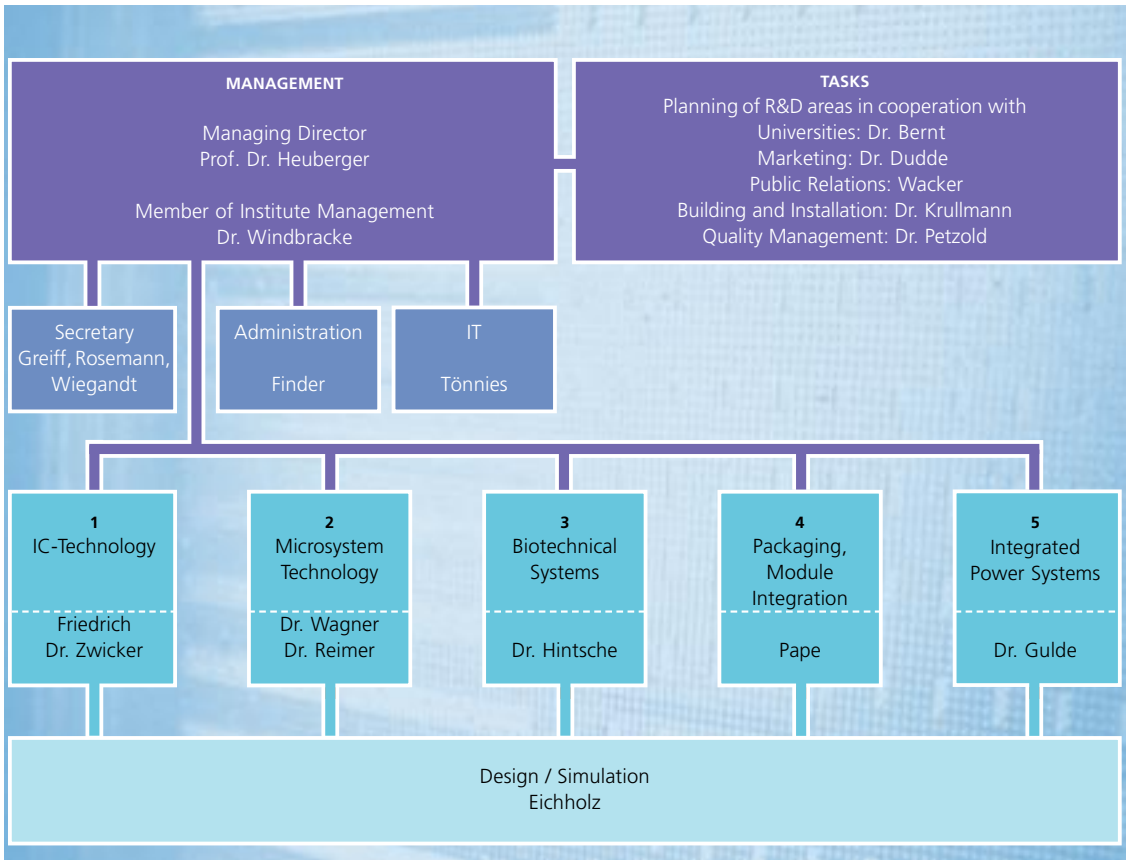
Dr. Peter Merz was honoured with the MAZ Award 2004 for the development of a new process for the manufacturing of microoptical lenses.

technologies and components while SMI focuses on the appropriate production engineering and quality assurance. Owing to the fact that ISIT's clean room for back-end microsystems engineering is stretched to the limits of its capacity – in preparation to the transition to 8" wafers and provide space for a large number of projects for external customers – SMI and ISIT intend to construct and operate their own joint clean room module on SMI's premises, equipped with the necessary 8" equipment. Itzehoe will then possess an optimized infrastructure for microsystems engineering, enabling customers to be offered end-to-end service from development to every scale of production.

The first major collaborative project between SMI and ISIT, the production line for chip-size packaging, has grown out of the teething stage and is now operating as a stable, high-yield production line, as demonstrated by the rising production volume. Chip-size packaging is an advanced technology that allows high-scale-integrated microelectronic circuits and microsystem components to be assembled and connected in extremely small packages, not much bigger than the silicon chip itself. Here too, the transition to 8" wafers represents an important milestone.

The expertise built up at the institute over the last 10 years, especially through its policy of creating close links between R&D and manufacturing industry, has started to arouse the interest of a wider public and is earning a certain acclaim. The most outstanding honor was the award of the German President's Future Prize for Technology and Innovation to

ISIT Organigram



On November 11, 2004, Dr. Walter Gumbrecht, Dr. Rainer Hintsche and Dr. Roland Thewes (from left to right) have been honoured by Bundespräsident Horst Köhler in Berlin with the "Deutscher Zukunftspreis", Germany's prestigious Future Award for Innovation and Technology.

Dr. Rainer Hintsche of ISIT and his colleagues Dr. Walter Gumbrecht of Siemens and Dr. Roland Thewes of Infineon Technologies. This prize, worth € 250,000, is one of the most prestigious awards for scientists in the German-speaking community. The three researchers received the award for their work on electric biochip technology. Dr. Hintsche and his team at ISIT have spent almost 10 years developing the fundamental scientific basis for applications of electric biochip technology. Out of this work, and in collaboration with a team of industrial partners headed by Walter Gumbrecht and Roland Thewes, has emerged a platform that will enable electric biochip technology to be implemented on an industrial scale. The key to the project's success has been its interdisciplinary approach, which brings together electrochemistry and biochemistry on the one hand with the universe of microstructures and silicon-chip technology on the other. The new technology has now fully entered the phase of transfer to manufacturing and deployment in a production environment.

ISIT has succeeded in launching a number of joint projects with future users to develop application-specific solutions using biochips in test and analysis systems, covering a whole range of molecules from DNA/RNA to proteins and haptens. The fields of application are diverse, and include monitoring for biological toxins, safety engineering, food processing, biotechnology and medical devices.

Dr. Rainer Hintsche with Prof. Hans-Jörg Bullinger, President of the Fraunhofer-Gesellschaft in Berlin.

Preface

Planned commercial application of the electrical biochip technology. The chipcard, developed by Siemens, contains a biochip, that can for example be used for the rapid testing of blood samples.

Open Day at the High-Tech location Itzehoe: Approximately 700 visitors were getting information about the actual main focus of work and research at the Fraunhofer ISIT, Vishay, the TF of the CAU-Kiel, SMI, Solid Energy, Condias and the IZET.

One particular success was the development of a detection system for biowarfare agents, which represents one of the main focuses of the new working field of "homeland security". ISIT has agreed on a strategic partnership with the engineering and defense supply company Diehl. An initial version of the new test system has undergone successful trials at various German army establishments.

Further members of ISIT staff who have been honored this year include Dr. Peter Merz, who together with his colleagues Jochen Quenzer and Arne Schulz-Walsemann received the MAZ Award for their development of a new process for manufacturing micro-optical lenses. The MAZ Award is a regionally based innovation prize awarded by MAZ level One, a financial services provider for young startup ventures, in consort with two north-German competence networks, Hanse-NanoTec and Hanse-Photonik e. V. This prize recompenses research papers that demonstrate the greatest potential for the creation of new business opportunities in the fields of nanotechnology and optical technologies in northern Germany.

The process developed by Peter Merz and his colleagues – called glass flow process – enables the manufacturing of microlenses at low cost and high volume in almost any required size. There is a huge demand for such lenses. They are used in telecommunications, for example, to feed optical signals into the fibers of optical cables. But miniaturized lenses are also required in security systems such as fingerprint sensors – for credit card authentication or car immobilization devices, etc.

ISIT meanwhile possesses the largest capacity and greatest expertise in microsystems development in Germany. This is clearly illustrated by the two projects that won awards in 2004, but also in a multitude of other scientific advances that have emerged from the institute. In the context of its industrial contract research work in recent years, ISIT has built up a stable customer base of more than 350 companies, including around 50 located in Schleswig-Holstein. In 2004, the foundations have been laid for further expansion of the local research infrastructure that will assure its viability well into the future.

JAHR DER TECHNIK 2004

Zukunft made in Germany

Close cooperation between research organizations and manufacturing companies is one of the unique selling points supporting Itzehoe's claim to excellence as a favored destination for investments in the high-technology sector. This was also a good reason for organizing a public open day in connection with the "Year of Technology" initiative launched by the BMBF. The purpose of this event was to give visitors a comprehensive picture of the new ways in which research and industry can work together, and to explain why microelectronics and microsystems engineering are of such continued importance to our future lives. The day was a great success. In a varied series of events, including video presentations and guided tours of research facilities and company sites, the members of the Itzehoe high-tech community, including ISIT, Vishay, SMI, the faculty of engineering at the University of Kiel, Sollith Batteries, Condias and the Itzehoe innovation center IZET, demonstrated their work. Some 700 visitors – school classes, students, friends and family of employees, and members of the general public – came to find out more about the latest developments in the participants' areas of activity and engaged in lively discussions with the members of staff present. The visitors were visibly impressed by the enthusiasm and dedication of the people they met.

These achievements are the result of the persevering efforts and hard work of the entire staff of ISIT. I would therefore like to thank all employees for their excellent performance and their willingness to take up all these challenges. They are responsible for the Institute's success.

Anton Heuberger

Brief Portrait

Fraunhofer ISIT
Research and Production at one Location

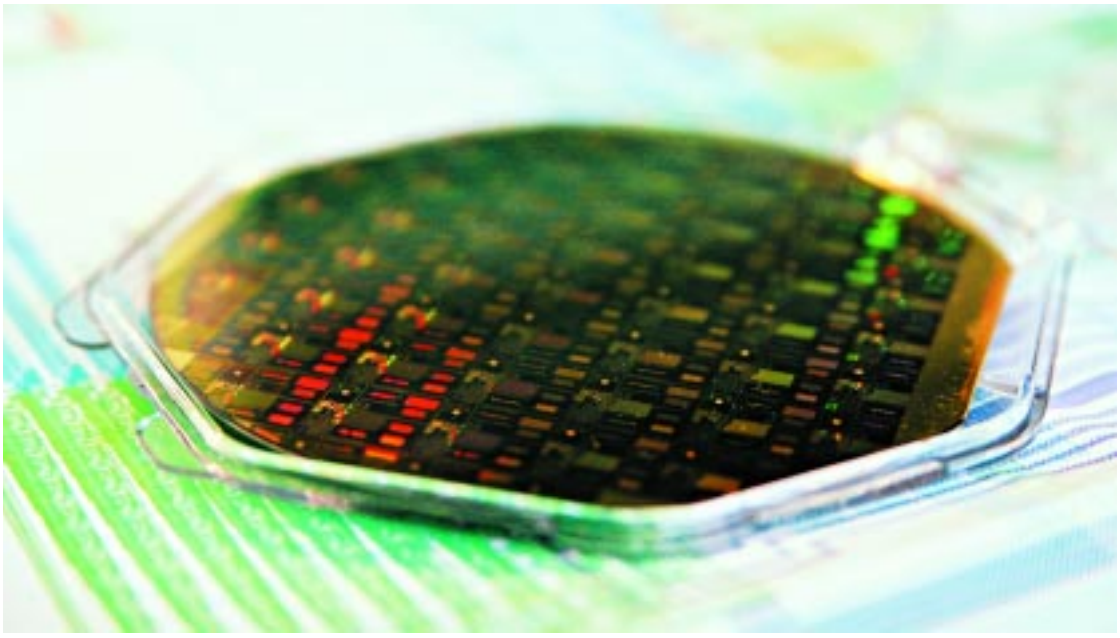
The Fraunhofer-Institut für Siliziumtechnologie (ISIT) develops and manufactures components in microelectronics and microsystems technology, from the design phase – including system simulation – to prototyping and fabrication of samples, up to series production. Though components such as valves and deflection mirrors manufactured by Fraunhofer ISIT often measure just a fraction of a millimeter in size, their range of applicability is anything but small: the devices are implemented in areas as diverse as medicine, environmental and traffic engineering, communication systems, automotive industry, and mechanical engineering. Working under contract, ISIT develops these types of components in accordance with customer requirements, also creating the application-specific integrated circuits (ASICs) needed for the operation of sensors and actuators. Included in this service is the integration into the overall microsystem using miniaturized assembly and interconnection technology.

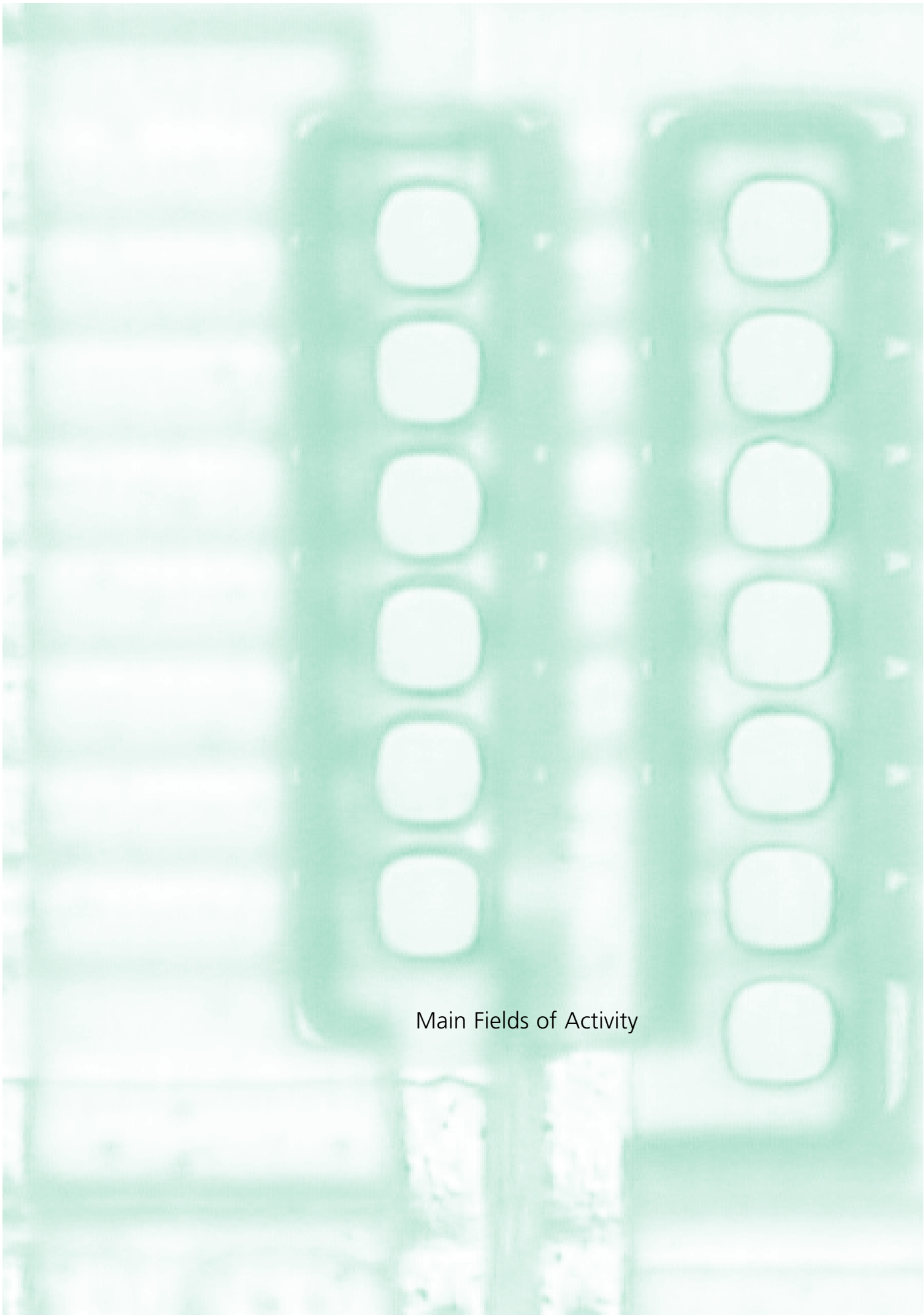
Together with Vishay Semiconductor Itzehoe GmbH, the institute operates a professional semiconductor production line which is up-to-date in all required quality certifications. The line is used not only for producing microelectronic components (PowerMOS) and microsystems, but also for R&D projects aimed at developing new components and technological processes. An ISO-9001-certified quality management system serves as the basis for the development, qualification and production of micro-engineered components.

Other groups at ISIT carry out work on assembly and packaging techniques for microsystems and sensors, analyze the quality and reliability of electronic components, and develop advanced power-supply components for electronic systems.

The institute employs a staff of around 150.

Wafer with electrical biochips.





Main Fields of Activity

Microsystems Technology (MEMS) and IC Design

The work performed at the institute focuses predominantly on microsystems technology, an area which ISIT pioneered in Germany. For over 20 years ISIT scientists have been working on the development of micromechanical sensors and actuators, micro-optic and fluidic components, and components for radio-frequency applications (RF-MEMS). Their work in this area also includes integrating these components with microelectronics to create novel systems. A multitude of components and systems have originated at ISIT.

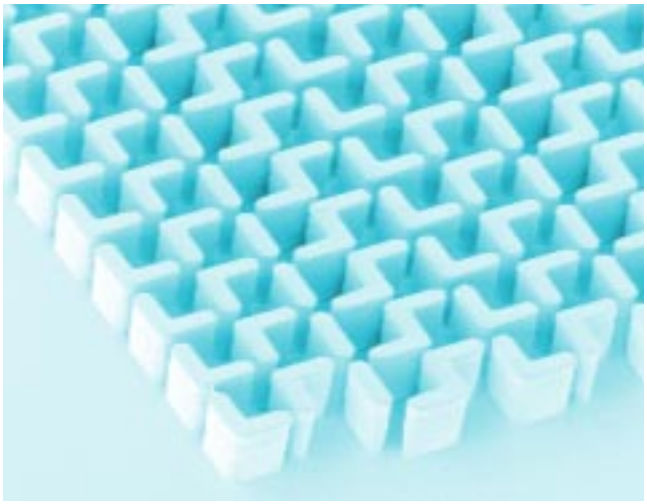
The current emphasis in the area of sensor technology is on inertial sensor technology (motion, inclination, acceleration, angular rate, IMU) and pressure, temperature and flow sensors (particularly gas flow), all with integrated electronics (ASICs). The development of customized integration concepts, ranging from simple, cost-effective assembly in a common package to complete monolithic integration, represents the core of ISIT's offerings in this area. One integration technique that customers may find particularly valuable is the ability to mount a microsystem on the surface of a fully processed ASIC wafer using a low-temperature process such as electroplating.

Among the key fluidic components created at ISIT are pneumatic valves, bi-stable fluid valves, sensor-controlled automatic microdosing devices, and micropumps, all of which can also be employed in Lab-on-Chip systems.

ISIT also develops optical microsystems, primarily for optical communication and instrumentation. Examples include micromirrors for laser displays, laser scanners and digital light modulators, and passive optical elements such as refractive and diffractive lenses, prisms, or aperture systems.

Radio-frequency microsystems developed at ISIT, designed primarily for use in wireless communication devices, include microrelays, high-frequency switches and tunable capacitors.

Systems which utilize actuators need to be able to generate the forces necessary for the device to interact with its environment. In order to meet



Detail of a programmable aperture platesystem for mask less projection lithography.

Different microoptical lenses by injection molding in polycarbonate.

Principle of a two axes micromirror chip (left).

Mobile laser projections displays are possible applications for MEMS-scanners (right).

the special requirements of microscopically small systems, ISIT implements electrostatic, thermal and – more recently – piezoelectric power.

The ISIT approach enables the institute to offer its customers all of these components as prototypes and also to manufacture them in series according to the customer's specific needs, utilizing the institute's in-house semiconductor production line wherever possible. The services provided also include application-specific micro-system packaging at the wafer level, using advanced wafer bonding methods.

Should a customer's requirements fall outside the scope of the institute's technological capabilities, ISIT can utilize a European network to gain access to other manufacturers and processes, like production lines at Bosch, SensoNor, HL Planar, ST and Tronic's. ISIT organizes the production as a foundry service for interested customers. And with the settlement of SMI GmbH in Itzehoe, the institute has gained a key partner for producing microsystems and related components as a foundry service under customer contract.

One of the prerequisites for developing original microsystems and microelectronic components is a highly capable circuit design group. The staff at ISIT are specialists in the design of analog/digital circuits, which enable the electronic analysis of signals from silicon sensors. The circuit designers at ISIT also devise micromechanical and micro optic elements and test their functionality in advance using FEM simulation. To carry out these assignments, the team has modified commercial design tools to meet the specialized challenges of microsystems technology.

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Concept for a tire pressure sensor.

Microsensor structure for inertial measurements.

IC Technology and Power Electronics

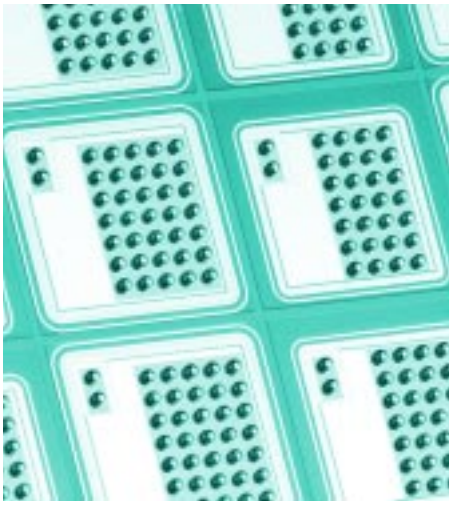
The power electronics and integrated circuits group develops and manufactures active integrated circuits as well as discrete passive components. Among the active components the main concern lies on power devices such as smart power chips, IGBTs, bi-directional components, PowerMOS circuits and diodes. Thereby ISIT primarily uses Vishay's customized, individual production sequences. Additional support for work in this area is provided by an array of modified tools for simulation, design and testing. ISIT also benefits from years of experience in the design and construction of CMOS circuits.

The passive components developed and fabricated at ISIT are primarily chip capacitors, precision resistors and inductors. Materials development and the integration of new materials and alloys into existing manufacturing processes play an important role in the development process.

ISIT develops individual processes, process modules and complete process flows for diverse applications. The institute also offers customer-specific silicon components processing in small to medium-sized batches on the basis of a qualified semiconductor process technology.

To support the development of new semiconductor production techniques, production equipment of particular interest is selected for testing and optimization by the ISIT staff. This practice provides the institute with specialized expertise in challenges related to etching, deposition, lithography, and planarization methods. Planarization using chemical-mechanical polishing (CMP) in particular is a key technology for manufacturing advanced integrated circuits and microsystems.

The intensive work done by ISIT in this area is supported by a corresponding infrastructure: The institute's CMP application lab is equipped with CMP cluster tools, single- and double-sided polishers and post-CMP cleaning equipment for wafers with 100 to 300 mm in diameter. The CMP group at ISIT works in close relationship to Peter Wolters Surface Technologies GmbH since many years, as well as other semiconductor fabrication equipment manufacturers, producers



Power balling for IGBTs.

High current implanter in the ISIT cleanroom.

of consumables, CMP users and chip and wafer manufacturers.

The CMP group's work encompasses the following areas:

- Testing of CMP systems and CMP cleaning equipment
- Development of CMP processes for
  - Dielectrics (SiO_2, TEOS, BPSG, low-k, etc.)
  - Metals (W, Cu, Ni, etc.)
  - Silicon (wafers, poly-Si)
- Testing of slurries and pads for CMP
- Post-CMP cleaning
- CMP-related metrology
- Implementation of customer-specific polishing processes for ICs and microsystems

IC Technology and Power Electronics
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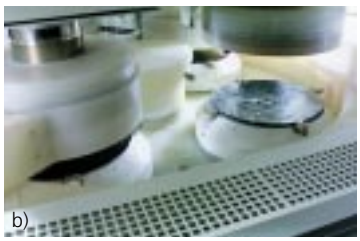
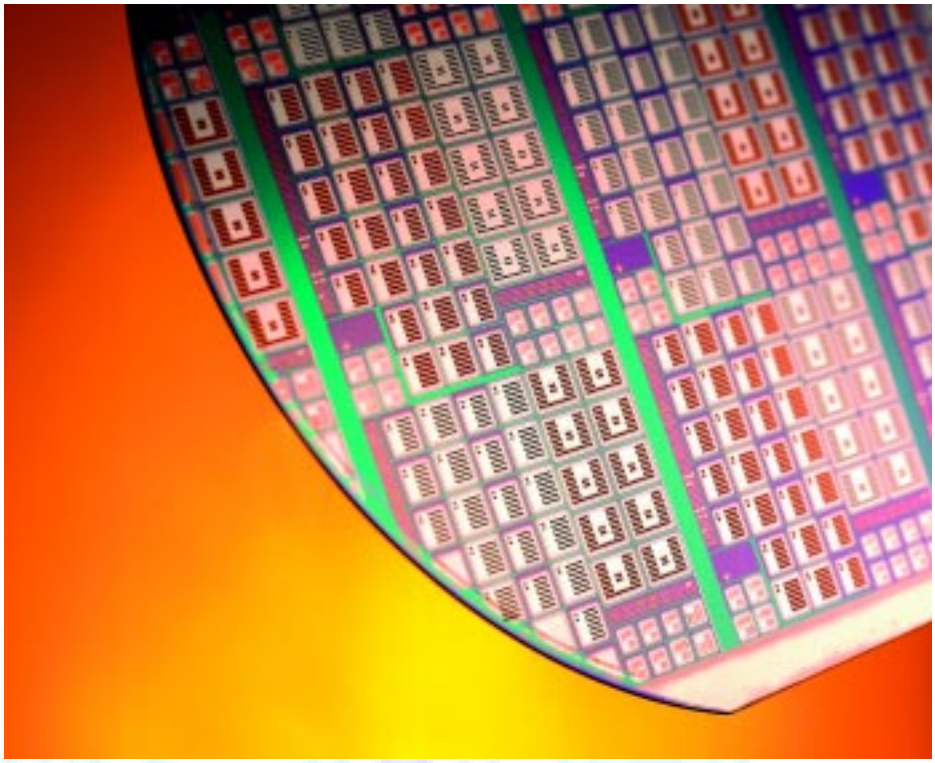
Peter Wolters HT-Cube, a high throughput CMP cluster for 300 mm wafers, small pictures details:

a) handling robot,
b) wafer transfer,
c) polishing table.





Wafer with different balled power devices.

Biotechnical Microsystems

ISIT is worldwide leading in electrical biochip technology, and is holding around 20 patents in the area. The electrical biochips offer intrinsic advantages vs. optical biochips because of direct miniaturization and transmission of responses of biochemical reactions into computing networks. Employing new ultramicroelectrodes and integrated reference and auxiliary electrodes the construction enables powerful sensor micro arrays and the use of ultra-sensitive, ultra-selective measurement techniques, such as "redox recycling." In combination with microfluidic components and integrated electronics, these electrical micro arrays represent the fastest and most cost-effective basis for mobile analysis systems, which can be used to identify and quantify DNA, RNA, proteins and haptens.

Those electrical micro arrays, which are packaged into proprietary "eBio-Chip-Sticks" are useful to detect a variety of analytes simultaneously. ISIT works closely with the Itzehoe based company eBiochip Systems GmbH (www.ebiochip.com) , an ISIT spin-off, to facilitate the marketing of these new technologies. Both together developed a variety of smart and portable instruments, from a low end device for education and demonstration to the high end fully automated micro array analyzer. Demonstrating very competititve applications as the identification and quantification of protein and pathogenic biowarfare agents or the antibiotics in raw milk the platform of electrical biochip technology is successfully used in several labs in Europe and in EU granted projects.

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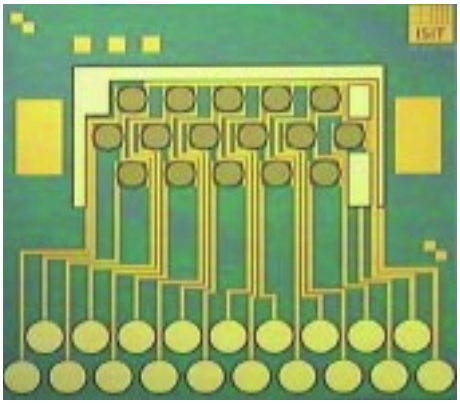
A new generation of a fully automatic eBiochip measuring system for the detection of biological agents.

Layouts for the "Lab on a Chip".

Electrical Silicon biochip.



Packaging Technology for Microelectronics and Microsystems

The assembly and interconnection technology group offers to customers a broad range of services, including precision assembly of microstructured components and development and qualification of customer-specific packaging. Work in this area includes hermeticity and material compatibility tests for assemblies that have to work in aggressive environmental conditions, e.g., analysis of microsystem packages intended for in vivo use in medical technology.

Another focal area is miniaturization of chip and sensor assemblies and packages, which includes direct assembly of bare silicon chips. The institute possesses capabilities in all of the essential technical stages for chip-on-board (COB) technology, from designing the circuit boards to qualified COB assemblies. The bare ICs and microsensors are mounted using the Chip & Wire or Flip-Chip techniques.

The group also develops processes for assembling and packaging chips and sensors/actuators while still on the wafer. Due to the increasing global trend among chip manufacturers to implement this special packaging process, Wafer Level Packaging (WLP) – now considered the assembly technique of the future – has become a central focus of the group's work. WLP technology can also be applied for packaging sensors under vacuum, such as angular rate or acceleration sensors. ISIT has successfully integrated thin film getter layers for high-Q microresonators with improved vacuum lifetime.

Application of solder spheres for wafer level CSP manufacturing in the SMI/ISIT production line.

The institute is active in this area not only as a technology developer, but also as a manufacturer of assemblies for its customers using the available Chip-Size-Packaging production line.

The group also develops ultra-thin electronic assemblies, which involves stacked mounting flexible silicon chips as thin as 50 µm on flexible substrates.

These techniques will ultimately lead to further miniaturization in existing systems, such as laptops, hand held PCs or mobile phones, but will also enable the development of new products like intelligent flexible product labels or smart clothes.

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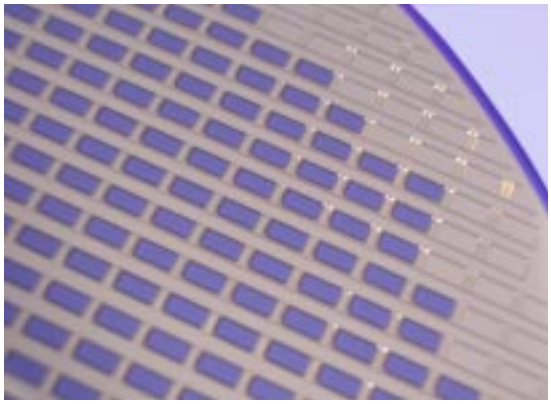
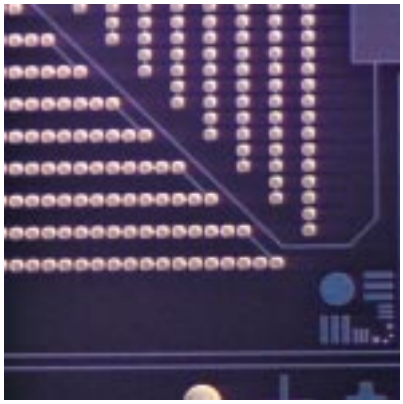
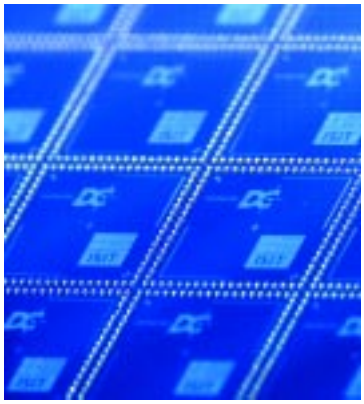
Cap wafer with individual getters for high vacuum sensor encapsulation on wafer level.

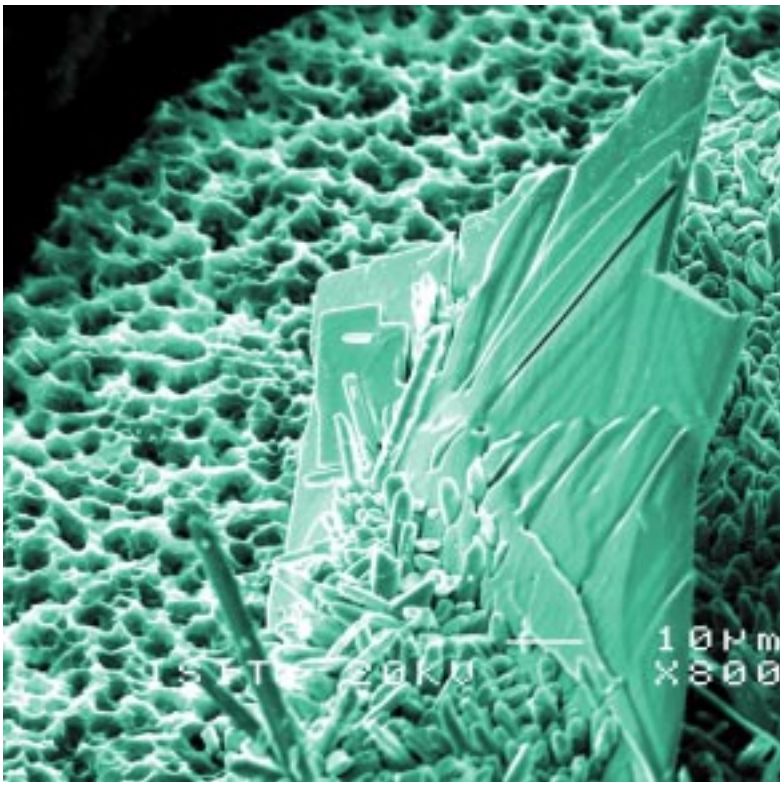


Detail of a testchip with 5000 galvanic Au contacts for evaluation of high precision flip chip bonder.

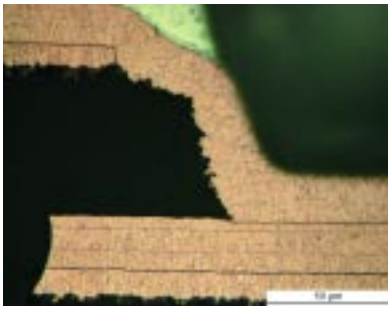


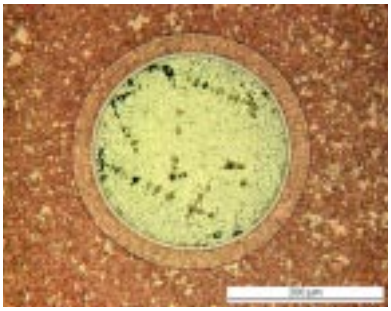
Standard testchip for otimization of flip chip solder processes.





Intermetallic phase particle inside a solder joint after deep etching of tin.





Evaluation of the integrity of different copper layers. Copper has been etched:
Micro via in the build-up layer of a printed circuit board (top).
Printed through hole with tin lead solder in a section view horizontal through an inner copper layer (bottom).

Quality and Reliability of Electronic Assemblies

Quality evaluation – in particular for the soldering work done in pre-production, pilot and main series lots – represents a continuous challenge for ISIT, for example whenever new technologies such as lead-free soldering are introduced, when increased error rates are discovered, or if the institute desires to achieve competitive advantages through continual product improvement. To reveal potential weak points, ISIT employs both destructive and non-destructive analysis methods, such as x-ray irradiation. Working from a requirements matrix, ISIT scientists also evaluate long-term behavior of lead-free and lead-containing assemblies alike. They then formulate prognoses on the basis of model calculations, environmental and time-lapse load tests, and failure analysis.

In anticipation of a conversion to lead-free electronics manufacturing, Fraunhofer ISIT is undertaking design, material selection and process modification projects. To effect a further optimization of manufacturing processes, the institute applies process models and produces samples on industry-compatible equipment. The group also addresses issues related to thermal management and reliability for customer-specific power modules.

In addition to these technological activities, the group regularly holds training sessions, including multi-day classes, at the institute or at company site.

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Lithium polymer battery production line – control of electrolyte dispenser unit.

Integrated Power Systems

The growing use of a wide array of mobile electronic devices is generating an increased demand for rechargeable batteries that are lighter, yet provide increased power density. Along with an exceptional power capacity, consumers expect long battery lifetime, increased safety and a higher degree of environmental compatibility. A new lithium rechargeable battery design developed by ISIT over the last few years – for which the institute has submitted a patent application – is capable of meeting these demands. This new concept, which features solid-state electrolytes, affords the same high power density typical of Lithium-ion rechargeables, but because the materials used in the new battery are inert, it does not need the complicated hermetic packaging technology required with conventional Lithium-ion batteries, which contain liquid electrolytes.
The battery needs only a metallized plastic foil packaging to make it air- and moisture-tight, resulting in a lower overall weight for the finished product.

The base material for ISIT's Lithium battery production process is a foil material. This allows batteries to be made in a much greater variety of shapes and sizes, thus significantly diversifying the range of possible applications.

ISIT offers the following services in this area: development, fabrication and small series production of customer-specific battery formats (ranging in size from microsystems to laptops) in a broad range of available ampere-hour ratings, with various forms of housings and materials (e.g. plastic or Titanium). Following the preparation of samples, ISIT supports the customer in the transition to series production. The institute also provides application-specific material selection of various compounds for cathodes (e.g. Lithium Cobaltite, Lithium Iron Phosphate) and anodes (Graphite, Lithium Titanate, etc.) to ensure optimal conformity to the application requirements (e.g., power density, cycle stability, capacity, product life cycle, self-discharge rate.) ISIT has built an initial production line for an industrial-scale production process.

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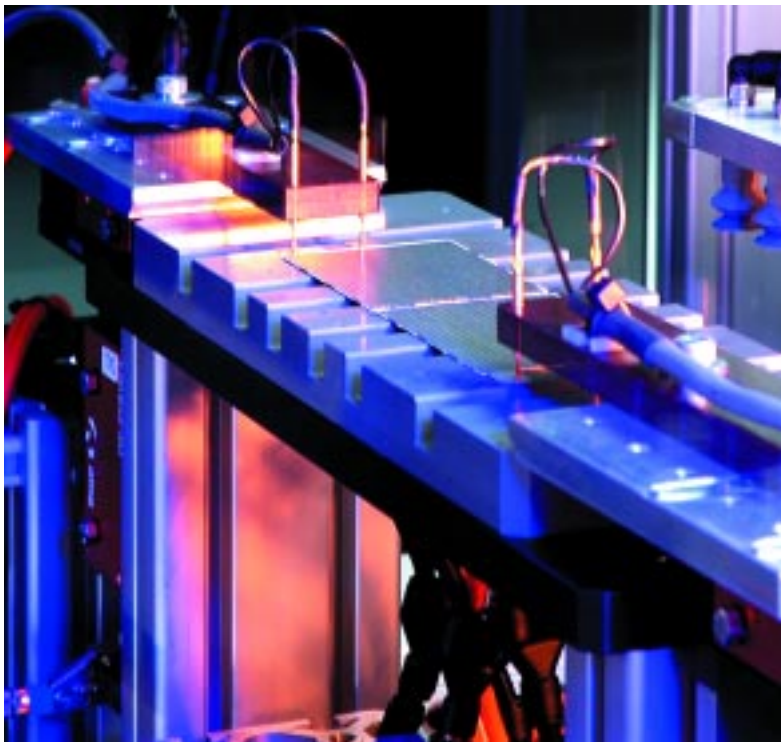
Lithium polymer battery production line – electrical test station.



Rechargeable Lithium polymer battery for hearing aids. Bottom: battery body.

Facilities and Equipment

In terms of both space and technical capabilities, the facilities at Fraunhofer ISIT provide an ideal environment for research & development work as well as production. In addition to its 150-mm silicon technology line and 2500 m^2 of clean-room space, the institute has a further 450 m^2 of clean-room area (class 100) for specific microsystems engineering processes, including: wet-etching processes, high-rate plasma etching, deposition of non-IC-compatible materials, lithography with thick resist layers, gray-scale lithography, electroplating, microshaping and wafer bonding. Further 200 m^2 clean-room (class 10-100) is equipped for chemical-mechanical polishing (CMP) and post-CMP cleaning. ISIT also offers a diverse selection of labs (1500 m^2) that are utilized by working groups for the development of chemical, biological and thermal processes, electrical and mechanical component characterization, and for assembly and interconnection technology. A spin-off arising from the work in assembly and interconnection technology – a CSP (Chip-Size Packaging) production line with an annual capacity of 100,000 wafers – was built in the ISIT clean rooms in collaboration with SMI GmbH (Silicon Manufacturing Itzehoe). The line is jointly operated by ISIT and SMI. The ISIT facility also operates a pilot production line for Lithium-polymer rechargeable batteries with power capacities of up to several ampere-hours.

ISIT cleanroom: lithography area (left), diffusion furnace area (bottom).

Offers for Research and Service

Spectrum of Services

The institute makes its range of services available to companies representing a wide variety of branches, including medical technology, communication systems, automotive industry, and industrial electronics, just to name a few. After industrial customers specify necessary requirements of the components and systems, ISIT engineers work closely with them to design, simulate and produce the components, systems and manufacturing processes. In this context, ISIT follows the technology platforms concept, which entails defining standard process flows that can be used to manufacture a large group of components simply by varying certain design parameters. Applying this modular technology concept is the optimal way to ensure that ISIT continues to offer competitive prices to its customers.

ISIT services have attractive implications for small-and medium-sized enterprises, which can take advantage of the institute's facilities and expertise in realizing technological innovations up to products.

Wafer loading into a Semitool spray clean tool.

ISIT-process demonstration for wafer level CSP manufacturing at the SMT 2004, Nürnberg

Customers

ISIT cooperates with companies of different sectors and sizes. In the following some companies are presented as a reference:

Adaptive Photonics, Hamburg

Alcatel Vacuum Technology, Annecy, France

Alma, Lyon, France

Amic, Uppsala, Sweden

Andus GmbH, Berlin

ARC Seibersdorf Research GmbH, Wien, Austria

ASE, Seoul, Corea

Atotech Deutschland GmbH, Berlin

Autoliv GmbH, Elmshorn

Basler Vision Technologies, Ahrensburg

BDT GmbH & Co. KG, Rottweil

Beru Electronics GmbH, Bretten

Borg Instruments, Remchingen

Bosch, Reutlingen

Bruker Daltonik GmbH, Bremen

Bullith Batteries AG, München

Card Guard, Rehovat, Israel

Cardi plus, Sevilla, Spain

Condias GmbH, Itzehoe

Conti Temic microelectronics GmbH, Nürnberg

DancoTech A/S, Ballerup, Denmark

Danfoss Lighting Controls, Nordborg, Denmark

Danfoss Drives, Graasten, Denmark

Danfoss Silicon Power GmbH, Schleswig

Datacon, Radfeld/Tirol, Austria

Degussa AG, Hanau

Dekati Oy, Tampere, Finland

Diabem, Barcelona, Spain

Diehl Avionik, Überlingen

Disetronic Medical Systems AG, Burgdorf, Switzerland

Dräger Systemtechnik, Lübeck

EADS, Ulm

EADS space, Bremen

eBiochip Systems GmbH, Itzehoe

Elektronik Zentrum Hersfeld, Bad Hersfeld

Elmos Semiconductor AG, Dortmund

Environics Oy, Mikkeli, Finland

Equicon, Jena

ESCD, Brunsbüttel

ESW-EXTEL Systems GmbH, Wedel

EVGroup, Schärding, Austria

EZL, Limburg

Flextronics International, Althofen, Austria

FOS Messtechnik GmbH, Schacht-Audorf

Fuba GmbH, Gittelde

Fujitsu Siemens Computers GmbH, Augsburg

GKSS, Geesthacht

GLAD, Geesthacht

Heidenhain, Traunreut

HL Planartechnik GmbH, Dortmund

H. C. Starck, Leverkusen

Hella KG, Lippstadt

ICT, München

IMS, Jena

IMS, Wien, Austria

Infineon Technologies, München

JLS Designs, Somerset, UK

Jungheinrich AG, Norderstedt

Kapsch, Wien, Austria

Kember Assiciates, Bristol, UK

Kerr McGee, Krefeld

KID Systeme, Buxtehude

Kolbenschmidt Pierburg AG, Neuss

Kristensen GmbH, Harrislee-Flensburg

Kuhnke GmbH, Malente

Legrant, Limoges, France

LEICA, Jena

Litef, Freiburg

Mair Elektronik GmbH, Neufahrn

Mars, Espoo, Finland

MED – EL, Innsbruck, Austria

Miele & Cie., Gütersloh

Motorola GmbH, Flensburg

MRT – Micro-Resist-Technology, Berlin

Nokia Research Center, Nokia Group, Helsinki, Finland

NU-Tech GmbH, Neumünster

OK Media Disc Service GmbH & Co.KG, Nortorf

Osram Opto Semiconductors GmbH, Regensburg

Oticon, A/S, Hellerup, Denmark

PAV Card GmbH, Lütjensee

Philips Semiconductors, Hamburg

Polytec GmbH, Waldbronn

PRETTL Elektronik Lübeck GmbH, Lübeck

Procter &, Gamble, Newcastle, UK

Qinetiq Ltd, Worcestershire, UK

Raytheon Anschütz GmbH, Kiel

Rehm Anlagenbau GmbH + Co. KG, Blaubeuren-Seissen

Robert Bosch GmbH, Salzgitter

SAES Getters S.p.A., Lainate/Milan, Italy

Scana Holography Company GmbH, Schenefeld

Scanbec Oy, Oulu, Finland

Scanbec GmbH, Halle

Schott, Landshut

SEF GmbH, Scharnebek

SensorDynamics (SD), Lebring, Austria

Sentech Instruments GmbH, Berlin

Siemens AG, München

Siemens Mobile, München

Siemens VDO Automotive AG, Schwalbach

Siemens VDO, Karben

SMA Regelsysteme GmbH, Niestetal

SMI GmbH, Itzehoe

Smith Detection, Watford, UK

Sollith Batteries GmbH, Itzehoe

Sonion, Lyngby, Denmark

ST Microelectronics, Crolles, France

ST Microelectronics, Mailand, Italy

Still GmbH, Hamburg

SÜSS Microtec AG, Garching

Su unto, Vantaa, Finland

Technolas, München

Technovision GmbH, Feldkirchen

Telefonica, Madrid, Spain

Thales Avionics, Valence, France

Thales, Meudon la Forêt, France

Thales, Paris, France

Trioptics GmbH, Wedel

Tronic´s, Grenoble, France

Vishay, Holon, Israel

Vishay Semiconductor GmbH, Itzehoe

Wabco Fahrzeugbremsen, Hannover

Peter Wolters CMP Systeme GmbH, Rendsburg

Woowon Technology, Corea

Offers for Research and Service

Innovation Catalogue

ISIT offers its customers various products and services already developed for market introduction. The following table presents a summary of the essential products and services. Beyond that the utilisation of patents and licences is included in the service.

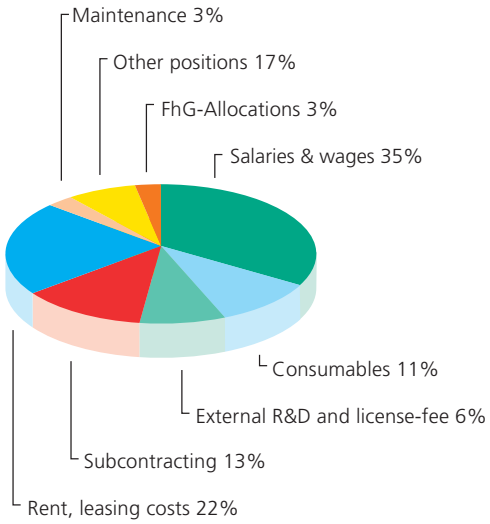
Product / Service	Market	Contact Person
Testing of semiconductor manufacturing equipment	Semiconductor equipment manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
Chemical-mechanical polishing (CMP), planarization	Semiconductor device manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
Wafer polishing, single and double side	Si substrates for device manufacturers	Dr. Gerfried Zwicker + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
IC processes CMOS, PowerMOS, IGBTs	Semiconductor industry IC-users	Detlef Friedrich + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Single processes and process module development	Semiconductor industry semiconductor equipment manufacturers	Detlef Friedrich + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Customer specific processing	Semiconductor industry semiconductor equipment manufacturers	Detlef Friedrich + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Microsystem Products	Electronic industry	Dr. Ralf Dudde + 49 (0) 4821/17-4212 ralf.dudde@isit.fraunhofer.de
Plasma source development	Semiconductor equipment manufacturers	Christoph Huth + 49 (0) 4821/17-4628 christoph.huth@isit.fraunhofer.de
Plasma diagnostics	Semiconductor equipment manufacturers	Joachim Janes + 49 (0) 4821/17-4604 joachim.janes@isit.fraunhofer.de
Etching and deposition process control	Semiconductor industry	Joachim Janes + 49 (0) 4821/17-4604 joachim.janes@isit.fraunhofer.de
Ion projection lithography open stencil mask technology and resist processes	Semiconductor industry	Dr. Wilhelm Brünger + 49 (0) 4821/17-4228 email: wilhelm.bruenger@isit.fraunhofer.de
Inertial sensors	Motorvehicle technology, navigation systems, measurements	Dr. Bernd Wagner + 49 (0) 4821/17-4223 bernd.wagner@isit.fraunhofer.de
Design for commercial MST processes	Micro sensors and actuators	Dr. Bernd Wagner + 49 (0) 4821/17-4223 bernd.wagner@isit.fraunhofer.de
Microvalves for gases and liquids	Analytic, medical technology measurement	Hans Joachim Quenzer + 49 (0) 4821/17-4524 hans-joachim.quenzer@isit.fraunhofer.de
Microoptical scanners and projectors	Biomedical technology, optical measurement industry, telecommunication	Ulrich Hofmann + 49 (0) 4821/17-4529 ulrich.hofmann@isit.fraunhofer.de
Microoptical components	Optical measurement,	Dr. Klaus Reimer + 49 (0) 4821/17-4506 klaus.reimer@isit.fraunhofer.de
Mastering and replication of micro structures in plastic	Microoptics, microfluidics	Dr. Klaus Reimer + 49 (0) 4821/17-4506 klaus.reimer@isit.fraunhofer.de

Product / Service	Market	Contact Person
Design and test of analogue and mixed-signal ASICs	Measurement, automatic control industry	Jörg Eichholz + 49 (0) 4821/17-4213 joerg.eichholz@isit.fraunhofer.de
Design Kits	MST foundries	Jörg Eichholz + 49 (0) 4821/17-4213 joerg.eichholz@isit.fraunhofer.de
RF-MEMS	Telecommunication	Thomas Lisec + 49 (0) 4821/17-4512 thomas.lisec@isit.fraunhofer.de
MST Design and behavioural modelling	Measurement, automatic control industry	Jörg Eichholz + 49 (0) 4821/17-4213 joerg.eichholz@isit.fraunhofer.de
Electrodeposition of microstructures	Surface micromachining	Martin Witt + 49 (0) 4821/17-4541 martin.witt@isit.fraunhofer.de
Digital micromirror devices	Communication technology	Dr. Klaus Reimer + 49 (0) 4821/17-4506 klaus.reimer@isit.fraunhofer.de
Electrical biochip technology (proteins, nucleic acids, haptens)	Biotechnology, related electronics, microfluidics, environmental analysis, Si-Chipprocessing, packaging, chip loading	Dr. Rainer Hintsche + 49 (0) 4821/17-4221 rainer.hintsche@isit.fraunhofer.de
Secondary lithium batteries based on solid state ionic conductors	Mobile electronic equipment, medical applications, automotive, smart cards, labels, tags	Dr. Peter Gulde + 49 (0) 4821/17-4606 peter.gulde@isit.fraunhofer.de
Battery test service, electrical parameters, climate impact, reliability, quality	Mobile electronic equipment medical applications automotive, smart cards, labels, tags	Dr. Peter Gulde + 49 (0) 4821/17-4606 peter.gulde@isit.fraunhofer.de
Quality and reliability of electronic assemblies (http://www.isit.fraunhofer.de)	Microelectronic and power electronic industry	Karin Pape + 49 (0) 4821/17-4229 karin.pape@isit.fraunhofer.de
Leadfree / RoHS transformation in electronic assembly	Electronic industry	Dr. Thomas Ahrens +49 (0) 4821/17-4605 thomas.ahrens@isit.fraunhofer.de
Material and damage analysis	Microelectronic and power electronic industry	Dr. Thomas Ahrens + 49 (0) 4821/17-4605 thomas.ahrens@isit.fraunhofer.de
Thermal measurement and simulation	Microelectronic and power electronic industry	Dr. M. H. Poech + 49 (0) 4821/17-4607 max.poech@isit.fraunhofer.de
Packaging for microsystems, sensors, multichip modules (http://www.isit.fraunhofer.de)	Microelectronic, sensoric and medical industry	Karin Pape + 49 (0) 4821/17-4229 karin.pape@isit.fraunhofer.de
Wafer level packaging, ultra thin Si packaging and direct chip attach using flip chip techniques	Microelectronic, sensoric and medical industry	Wolfgang Reinert + 49 (0) 4821/17-4617 wolfgang.reinert@isit.fraunhofer.de
Vacuum wafer bonding technology	Microelectronic, sensoric and medical industry	Wolfgang Reinert + 49 (0) 4821/17-4617 wolfgang.reinert@isit.fraunhofer.de
Flow sensors	Automotive, fuel cells	Dr. Peter Lange + 49 (0) 4821/17-4118 peter.lange@isit.fraunhofer.de

Representative Figures

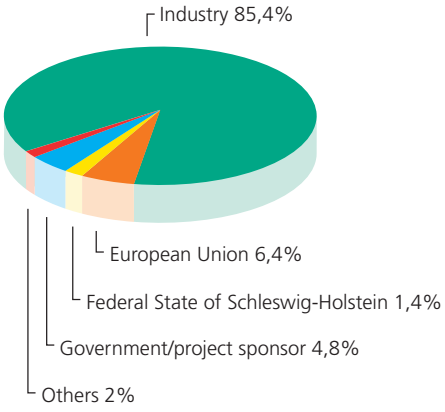
Expenditure

In 2004 the operating expenditure of Fraunhofer ISIT amounted to kEuro 18.314. Salaries and wages were kEuro 6.438, consumables and other costs were kEuro 11.876.



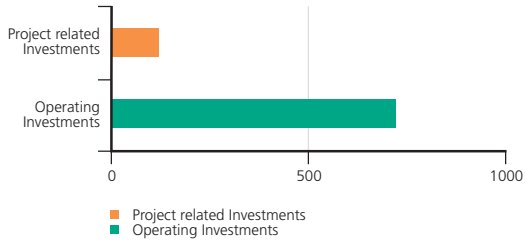
Income

The budget was financed by proceeds of projects of industry/industrial federations/small and medium sized companies amounting to kEuro 13.730, of government/project sponsors/federal states amounting to kEuro 995 and of European Union/others amounting to kEuro 1.354.



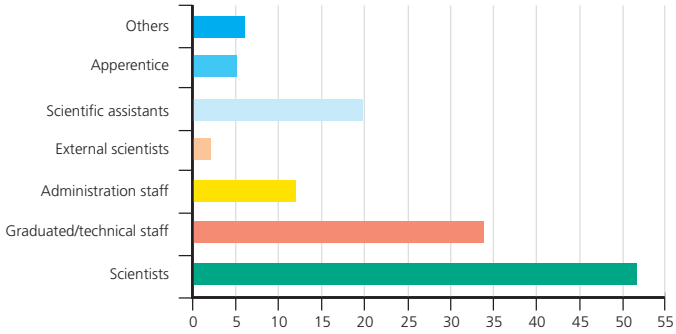
Capital Investment

In 2004 the institutional budget of capital investment was kEuro 837. The amount of operating investment was kEuro 721 and project related investments were amounted to kEuro 116.



Staff Development

In 2004, on annnual average the staff constisted of 98 employees. 52 were employed as scientific personnel, 34 as graduated/technical personnel and 12 worked within organisation and administration. 2 scientist, 20 scientific assistents and 5 apprentice supported the staff as external assistance.



The Fraunhofer-Gesellschaft

The Fraunhofer-Gesellschaft undertakes applied research of direct utility to private and public enterprise and of wide benefit to society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration. The organization also accepts commissions and funding from German federal and Länder ministries and government departments to participate in future-oriented research projects with the aim of finding innovative solutions to issues concerning the industrial economy and society in general.

By developing technological innovations and novel systems solutions for their customers, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. Through their work, they aim to promote the successful economic development of our industrial society, with particular regard for social welfare and environmental compatibility.

As an employer, the Fraunhofer-Gesellschaft offers its staff the opportunity to develop the professional and personal skills that will allow them to take up positions of responsibility within their institute, in other scientific domains, in industry and in society.

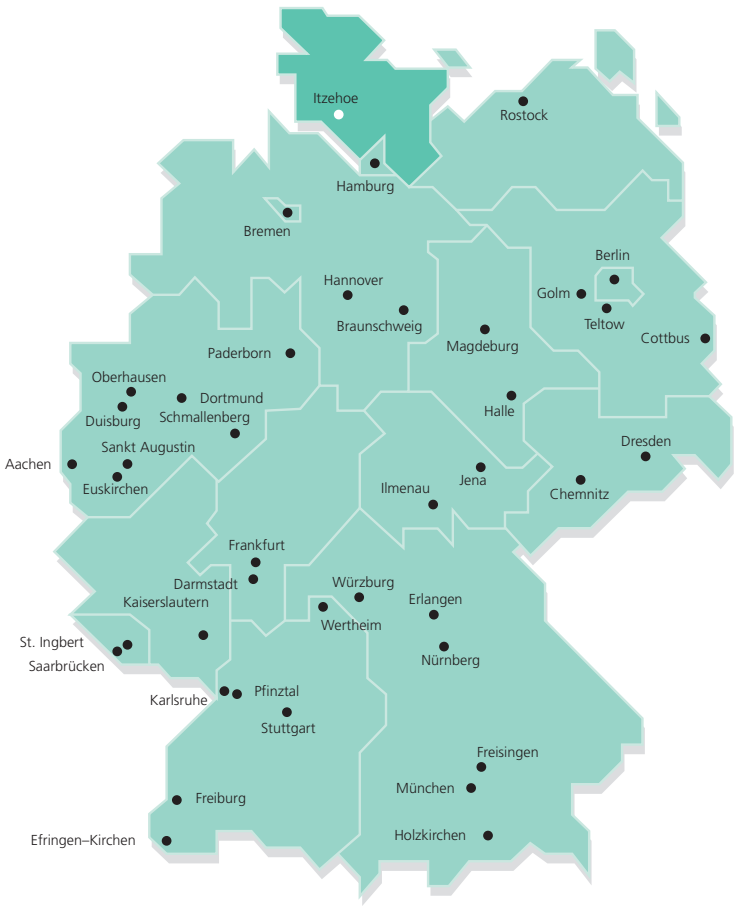
At present, the Fraunhofer-Gesellschaft maintains some 80 research units, including 58 Fraunhofer Institutes, at over 40 different locations in Germany. The majority of the roughly 12,500 staff are qualified scientists and engineers, who work with an annual research budget of over 1 billion euros. Of this sum, more than € 900 million is generated through contract research. Roughly two thirds of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. The remaining one third is contributed by the German federal and Länder governments, partly as a means of enabling the institutes to pursue more fundamental research in areas that are likely to become relevant to industry and society in five or ten years' time.

Affiliated research centers and representative offices in Europe, the USA and Asia provide contact with the regions of greatest importance to present and future scientific progress and economic development.

The Fraunhofer-Gesellschaft was founded in 1949 and is a recognized non-profit organization. Its members include well-known companies and private patrons who help to shape the Fraunhofer-Gesellschaft's research policy and strategic development.

The organization takes its name from Joseph von Fraunhofer (1787-1826), the illustrious Munich researcher, inventor and entrepreneur.

Locations of the Research Establishment



Representative Results of Work

Power Balling, Assembly for Power Devices

State of the art chip assembly of discrete power devices in power modules is realized by backside soldering on a DCB substrate (direct copper bonding) and frontside wire bonding (figure 1). This type of assembly is well established and reliably offering a good cost-performance relation for standard power applications.

However, since the performance of power devices has been improved continously over the last years there is a need for improved assembly techniques, also.

Due to the implementation of trench technology and ultra thin substrate technique in the power device fabrication process the conducting and switching behaviour was improved significantly. In order to enable this performance gain to be used on system level also wire bonding should be eliminated for special applications.

For e.g. low voltage PowerMOS transistors with R_{DSon} values in the mOhm range, wire bond resistance can clearly contribute to the overall on-resistance. This drawback can be overcome by front side solder bump technique of power devices. In addition to reduction of the on-resistance the heat transfer out of the power device can be improved also via front side solder bumps. Further, the parasitic wire inductance is eliminated, too.

The technological realisation of a solderable power device front side is being done by power ballling a specific application of wafer level chip size packaging. This technique comprises of an under bump metallisation (UBM) based on Al-NiV-Cu, a BCB (Benzo Cyclobuten) passivation, and solder ball attach with subsequent solder ball reflow (figure 2).

Power Balling was applied on Trench IGBT wafers in two different variations. In the first case under bump metallisation was located underneath the solder balls only, whereas in the second case UBM was covering the entire actice area in order to reduce the lateral surface resistance. In this case the Cu layer of the UBM can be seen on the chip front side. The gate terminal is located in the middle of the device with four balls being placed (figure 3).

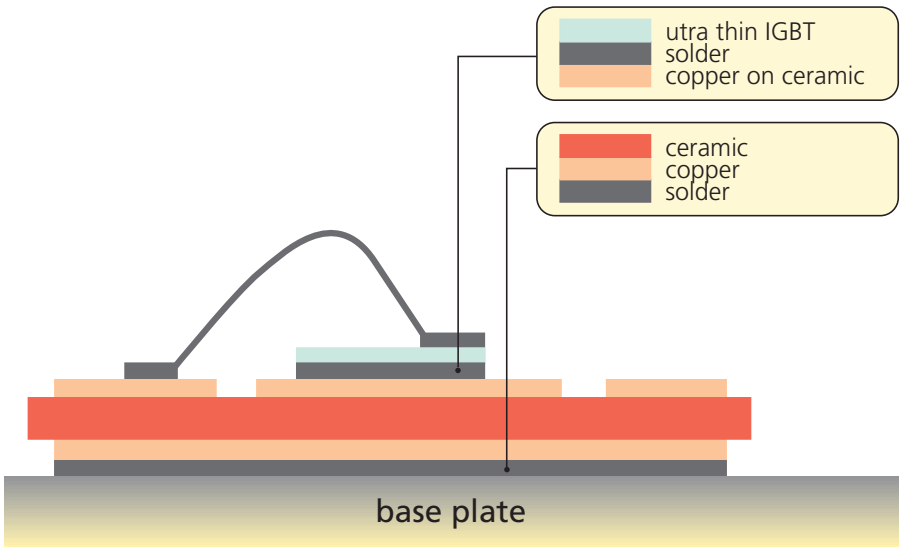


Figure 1:
Power device assembly on a DCB substrate with front side wire bonding in a power module.

It can be concluded that high performance power devices require high performance assembly techniques.

A possible sandwich type assembly of power devices with front side solder bumps is introduced in figure 4. Here, the power devices are soldered with the backside on a DCB substrate.
The frontside solder balls are connected to a special interconnect board with feed throughs to the front side. This offers the possibility of further assembly of e.g. passive components or even ICs in order to increase the overall integration density. Instead of using an interconnect board with feethroughs a simple metallic lead frame is possible also.

In summary, power balling will improve module assembly with regard to conducting and switching behaviour of power devices, to overcome thermal constraints and increase overall integration density. Especially for automotive application with high temperature requirements power balling can be an option for advanced power assembly.

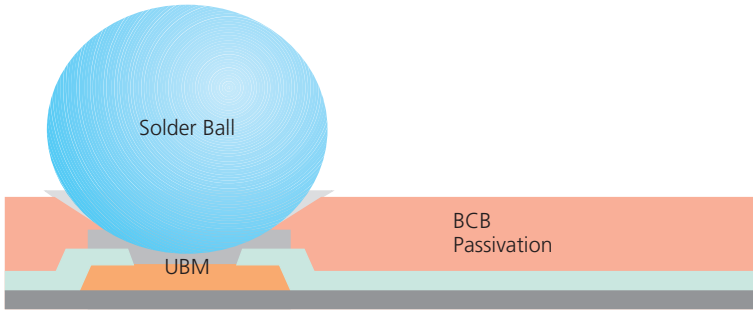


Figure 2:
Principle of wafer level Power Balling.

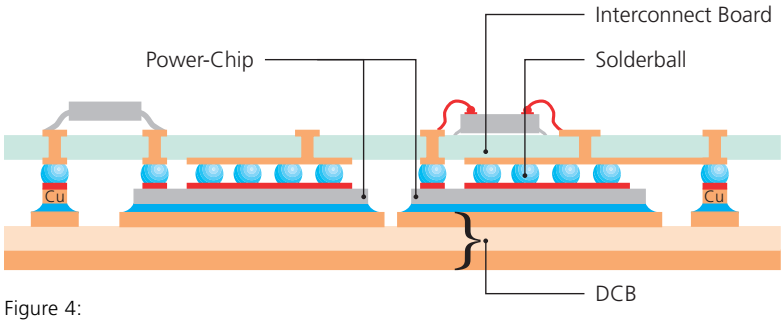
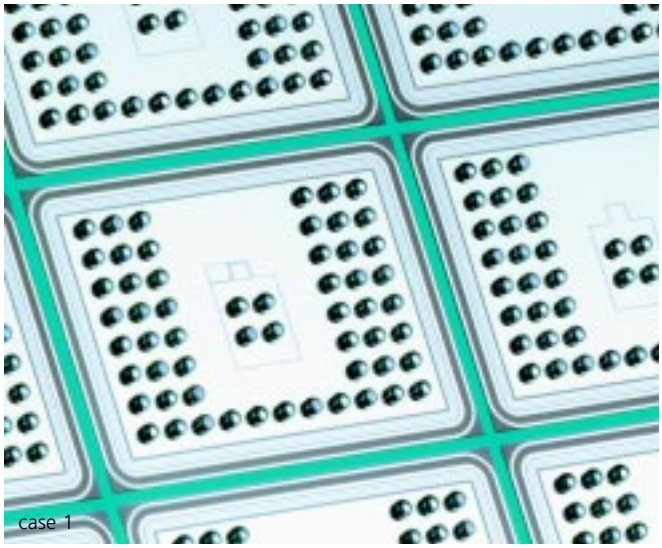
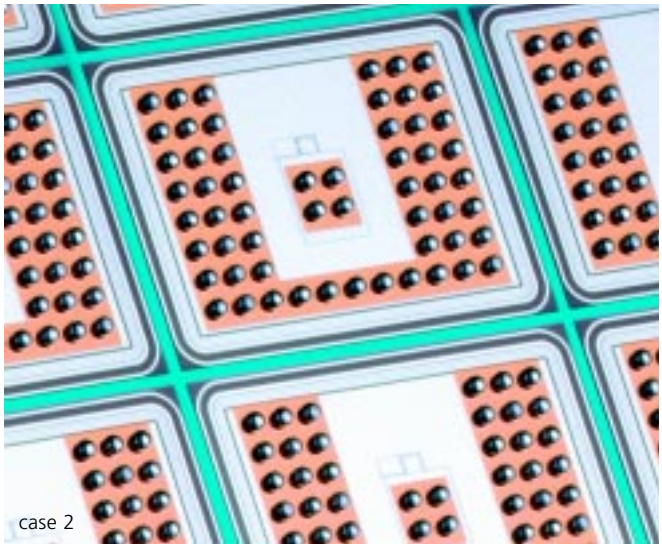


Figure 4:
Sandwich type module assembly for power devices with solder ball frontside.

Figure 3: Application of Power Balling on IGBT wafers. Case 1 with UBM underneath the solder balls only, case 2 with UBM covering the entire active IGBT area.





Wafer Level Chip Size Packaging Production at Itzehoe

Wafer Level Chip Size Packaging (WL-CSP) has become the most attractive packaging technique for many applications e.g. CSP for high density board assembly, high end IC-Packaging, RF- and power device assembly and further more.

In the past there was no commercial WL-CSP activity within Europe, instead industrial bumping suppliers were located in Far-East and the US only. In cooperation with SMI (Semiconductor Manufacturing Itzehoe) a joint project was started in 2003 to build up the first European center for WL-CSP production in Itzehoe. This decision was inspired by the idea to establish advanced packaging in Germany to compete with high volume production sites outside Europe. Therefore, competitive prices, short cycle times and a relevant process portfolio are mandatory.

Within the second half of 2003 lead content and lead free balling processes have been qualified. Since the beginning of 2004 SMI and ISIT started the production ramp up with a capacity of 50.000 6 inch wafers in the first year (figure 1 and figure 2). By equipment invest and process improvements the maximum line capacity in 2005 has reached 100.000 wafers per year.

The production is carried out in a state of the art class 100 back end cleanroom (figure 3).

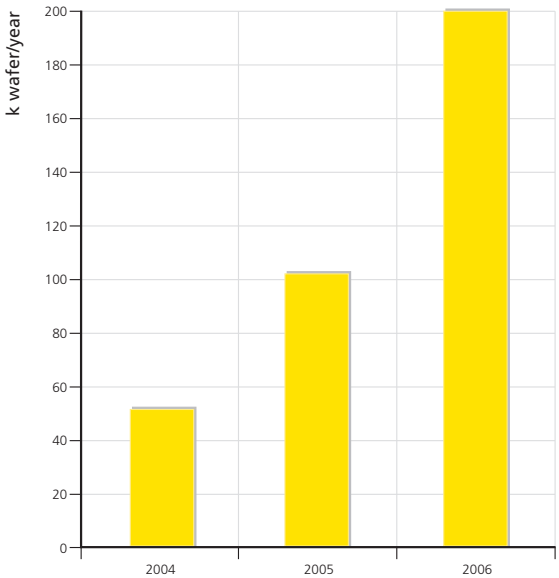


Figure 2:
Ramp up of production capacity.

Currently, the planning of an additional cleanroom for 8 inch wafers is in progress in order to offer WL-CSP for both wafer sizes (6 and 8 inch) in 2006.

Within this cooperation ISIT is responsible for the engineering and process development, mask design and layout as well as infrastructure and equipment sustaining. The operating of production, marketing and customer support is in the responsibility of SMI.

At this time a portfolio of 4 qualified CSP processes for lead content and lead free solder balls can be offered. Further processes for redistribution and fine pitch bumping based on solder paste printing are near to qualification and will be released for production in 2005 (figure 4). In a mid term view lead free solder plating for ultra fine pitch bumping is envisaged.

In conclusion it has to be highlighed that the production and R&D location Itzehoe brings together complementary knowledge, experience and abilities of different companies located at the Fraunhofer site:

1. the high volume IC-production capability of Vishay Semiconductor Itzehoe GmbH
2. the experience of SMI in operation of production, customer specific product development and marketing
3. the R&D excellence of the Fraunhofer Institute ISIT.

This mix of competences at the same location is an outstanding performance with high attractivity for customers. The availability of the entire value-added chain from development up to production is the main advantage which guarantees short cycles for time to market, competitive costs, easy cummunication and reduced effort for logistic.

Figure 1:
Time schedule for set up a WL-CSP production.

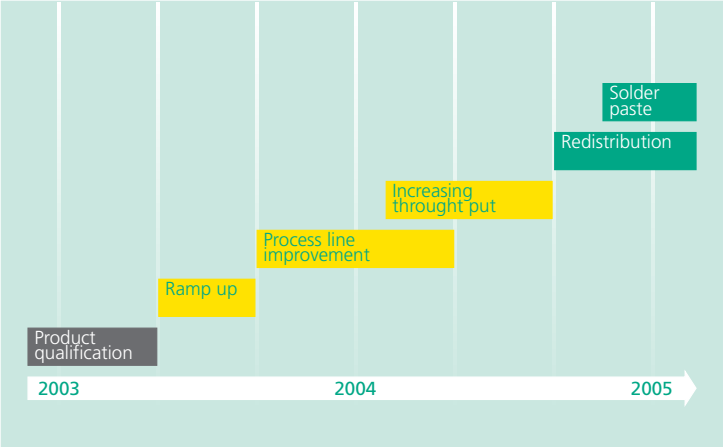


Figure 3:
State of the art production cleanroom for WL-CSP.

	Plated Bumps	Solder Paste	Solder Ball
I/O Count	3000	2000	200
Bump Pitch	60 µm	180 µm	500 µm
Bump Diameter	40 - 120 µm	80 - 220 µm	370 - 500 µm
Bump Height	20 µm	70 - 150 µm	200 - 400 µm
Package Height	0.3 - 0.6 mm	0.3 - 0.8 mm	0.6 - 1.1 mm
Under fill	Yes	Yes	Application dependent

Figure 4:
Overview on different bumping techniques.

MEMS Fabrication by Using CMP

Since its introduction in the beginning of the 90s, chemical-mechanical polishing (CMP) has developed into a key technology for the production of microelectronics devices. Starting with the planarization of inter level dielectrics (ILD), many new applications of CMP emerged over the years like CMP of tungsten for vias, CMP of copper as a replacement for aluminum metallisation, CMP for shallow trench isolation (STI), or CMP of poly-Si, to name a few. Further use of CMP includes polishing of Si-wafers or other substrates and of hard disk media. Since the mid-90s, CMP also found its way to the fabrication of MEMS devices.

Micro-Electro Mechanical Systems (MEMS) are microstructure products whose fabrication is enabled by microstructure technologies, which were mainly developed for microelectronics production. Other terms also used in this context are microsystems, micro system technology (MST) or micromechanics. Substrate materials can be silicon, but also glass, ceramics, metals, or others. Two MEMS-manufacturing techniques have been established: bulk micromachining and surface micromachining.

In bulk micromachining, the device is built in the bulk of the substrate by either wet etching (thinning) of the backside of the wafer or by deep reactive ion etching (DRIE) into the wafer. In surface micromachining, the device is built on the substrate as free-standing poly-silicon or metal structures by employing sacrificial layers.

Developed in the research laboratories over the last 15 years, microsystems and the accompanying fabrication techniques have recently begun

Parameters	MEMS		Microelectronics	Remarks
Typ. layer thickness	~ 1 - 10 µm	>>	< 1000 nm	
Required removal	~ 1 – 20 µm	>>	~ 200 – 1000 nm	
Required removal rates	> 0.5 µm/min	>	0.2 – 0.5 µm/min	alternative: grinding/polishing
Uniformity	< 5 %	=	< 5 %	
Throughput	< 10 wafers/h	<	20 – 60 wafers/h	
Starting topography	1 – 10 µm	>>	max. 1 µm	
Required planarity	> 100 nm	>	< 50 nm	opto: < λ10
Roughness R_a	10 nm	>	some nm	wafer bonding: 0.5 nm
Pattern width	µm - mm	>>	< 0.25 µm	
Dishing	> 100 nm	>	< 100 nm	large patterns
Erosion	> 100 nm	>	< 100 nm	large patterns
Critical particle	rel uncritical	>	< 0.1 µm	
Particle density	rel. uncritical	>	< 1/cm²	wafer bonding: < 1/cm²
Metal contamination	uncritical	>>	< 1 x 10^{12}/cm²	bonding: fresh surface
Wafer size	100 – max. 200 mm	>	200 – 300 mm	
Substrates	Si, metal, glass, ceramic		Si, III-V	
Layers	var. SiO_2, poly-Si, Si, var. metals, ceramics, polymers		var. SiO_2, Si, poly-Si, W, Cu	

Table 1:
Comparison of CMP requirements for MEMS fabrication vs. microelectronics manufacturing.

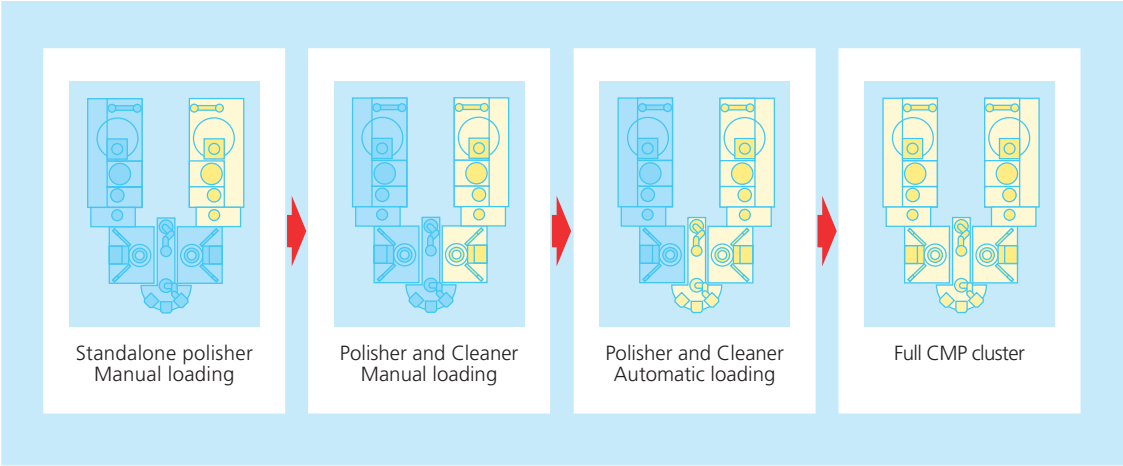


Figure 1:
From manually loaded lab polisher to fully automatic CMP cluster tool: The modular concept of the Peter Wolters PM 200 Gemini allows an upgrade of the CMP tool with growing production demands of the MEMS devices.

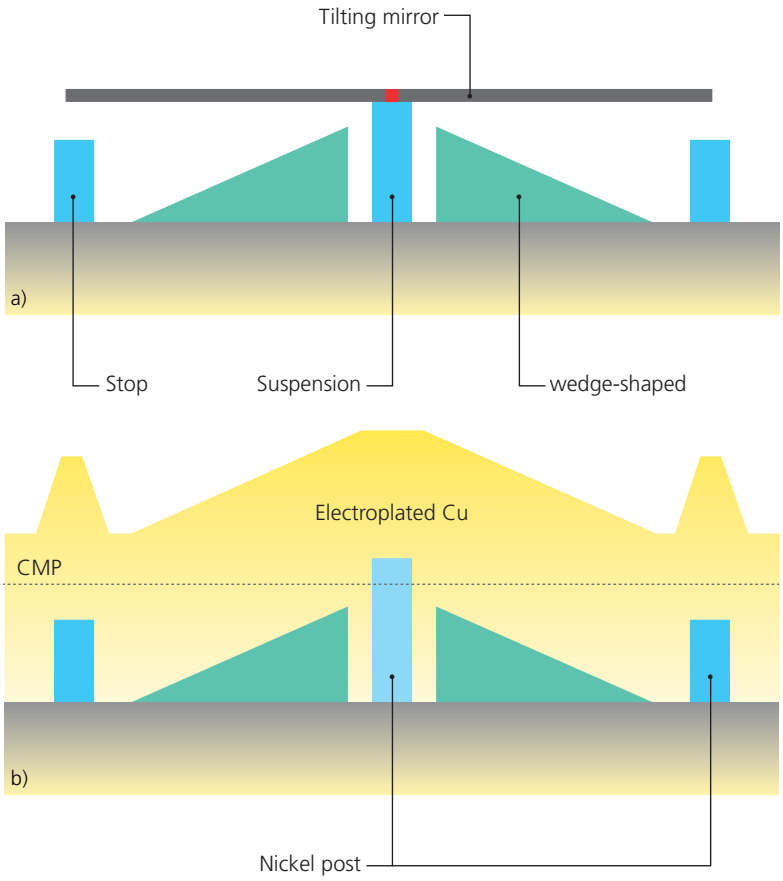
to move from the labs into the manufacturing floors. Typical MEMS products, which are already fabricated in large quantities, include acceleration sensors, gyroscopes and pressure sensors for the automotive industry. Optical switches for optical fibre networks and RF switches for tuneable capacitors, filters or antennas for cell phones are typical telecom applications. Printing heads for ink jet printers or R/W heads for hard disk drives are used in bulk quantities in office applications. Market forecasts predict annual growth rates for MEMS products of about 20 % for the next years, exceeding the predicted growth rates for microelectronic devices.

In MEMS fabrication, CMP is used for various purposes with an emphasis on surface micromachining. It is used to achieve flat, mirror-like surfaces for optical devices, it is used to planarize the topology from previous manufacturing steps and it is utilised to reduce film roughness for more precise lithography or for wafer bonding. While the critical dimensions of today's most advanced microelectronic devices fall below 100 nm, the structure dimensions of MEMS devices are usually larger and lay in the order of 1 – 100 µm or even in the millimetre range. The typical film thickness occurring in MEMS can be several µm, while in microelectronics, the future trend goes to ever decreasing values, sometimes only a few atomic layers.

In order to optimise a CMP cluster tool for MEMS applications, we have compared parameters of microelectronics manufacturing with typical requirements for MEMS devices, see table 1.

The comparison shows that MEMS-dedicated CMP tools have to fulfil demands that differ from CMP equipment developed for ULSI devices. Due to much thicker layers over larger structures with higher starting topography, the required material removal by polishing can be up to several ten micrometers. Since removal rates in microelectronics are typically below 0.5 µm/min, the CMP processes have to be accelerated in order to achieve reasonable throughputs of about 10 wafers/h, a goal which is relaxed by a factor of 2 – 5 to the requirements in IC manufacturing. For very high demands on material removal, using a combination of grinding and polishing might be an alternative.

Figure 2:
Crosscut through digital micro-mirror element. The tilting mirror is suspended by torsional hinges at the nickel posts and is deflected electrostatically by the wedge-shaped electrodes (a). For fabrication of the freely suspended mirror, a thick electro-plated copper layer, which has been planarized by CMP serves as a sacrificial layer (b).



Preston's law states that the removal rate of a polishing process depends linearly on the speed v between polishing pad and wafer and linearly on the pressure p with which the substrate is pressed against the pad:

$RR = k_P \, p \, v$

Properties of the slurry and pad used for the process are summarised in the Preston coefficient k_P.

Higher removal rates can therefore be achieved by increasing the table speed, which has a limitation due to the occurrence of high centri-fugal forces spinning-off the slurry and by increasing the pressure of the wafer against the pad. Higher pressures demand for very rigid polishing machines which can be realised e. g. by using a cast-iron frame. However, sometimes very high pressures can lead to delamination of the underlying layers.

Other means to achieve higher removal rates are utilising chemical aspects like increasing the slurry temperature or using accelerating additives in the slurry or utilising mechanical aspects like employing larger, harder and/or sharper abrasive particles or using tailored polishing pads. Since several years, CMP slurries optimised for MEMS applications are available from the slurry suppliers. Polishing pads with fixed abrasives, developed for microelectronics manufacturing applications, can also be used for MEMS fabrication.

Dishing or erosion of the structures during CMP, which are critical characteristics for ULSI manufacturing, are less critical in the MEMS world. However, due to the much larger structures, sometimes in the order of the planarization length of the process, planarity requirements are harder to fulfil. Especially in the case of opto-MEMS and the fabrication

of micro-mirror devices, surface qualities of λ /10 over larger distances have to be achieved. The requirements on surface roughness R_a after CMP are often less critical with the exception of surfaces prepared for wafer bonding, where R_a should be less than 0.5 nm.

A critical step in the CMP manufacturing sequence is post-CMP cleaning since slurry residues cannot be removed when once dried on the surface. The best equipment solution is a cluster set-up where the wafers are cleaned immediately after polishing. Otherwise the wafers have to be kept wet until cleaning and drying. While particle size and density has a direct impact on device yield for microelectronics manufacturing, it has a less pronounced impact on MEMS fabrication due to the larger feature sizes. Only wafer bonding requires clean surfaces comparable to microelectronics. Contamination by metal residues is of no concern in MEMS. In some cases metals like gold, silver, nickel, iron etc., which are lifetime killers for CMOS, are used as functional materials for MEMS.

While the mass production in microelectronics demands for large wafers with up to 300 mm diameter, the number of units of microsystems is smaller and can be produced on 100 or 150 mm wafers. Due to relaxed structure width requirements, older generation equipment, developed for 100 – 150 mm wafers, is often employed. Depending on the application, the wafers are made of silicon or other semiconducting materials, but also metal, glass or ceramics substrates are used.

In microelectronics manufacturing, polishing processes for various silicon oxides, mono- or polycrystalline silicon, conducting metals like tungsten or copper and barrier layers like titanium and tantalum and their nitrides have been

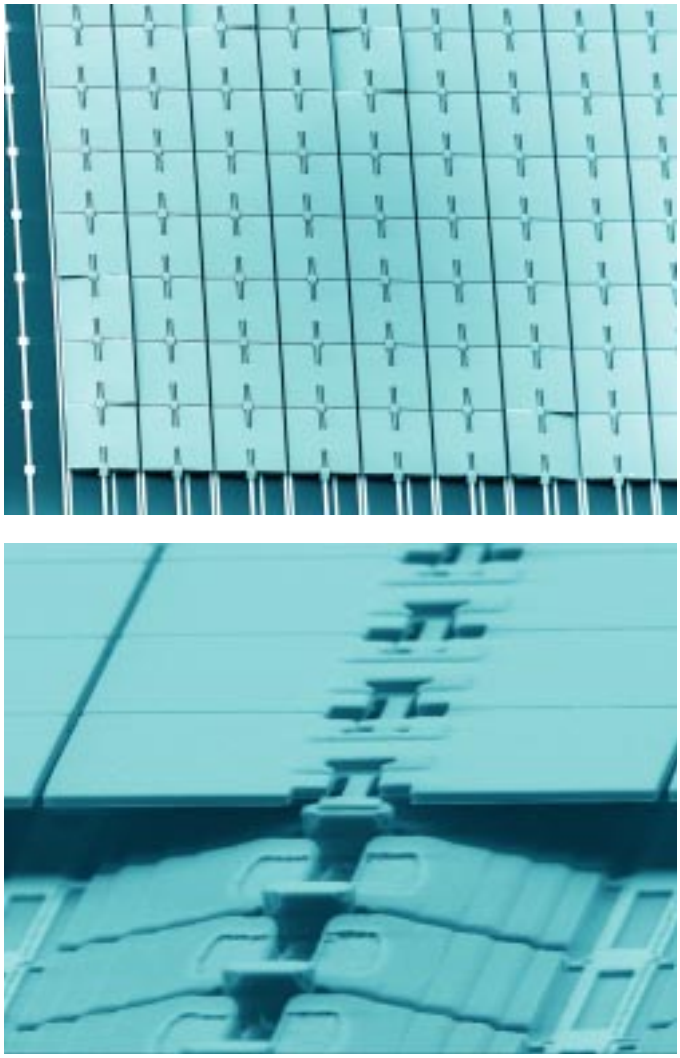


Figure 3:
Close-up of a digital mirror array (DMA) (a). Mirror elements with mirror and deflection electrodes (b). Only CMP allows the fabrication of planar tilting mirrors. For details see also figure 2a and b.

Figure 3a shows a part of the digital mirror array. In figure 3b details of the mirror elements like suspension posts, mirrors with torsional hinges and wedge-shaped deflection electrodes are clearly visible.

For the fabrication of a surface micromachining inertial sensor a poly-Si CMP process has been developed. The active sensing element consists of interdigital structures made of 10 µm thick poly-Si. The thick layer has been deposited using an epitaxy reactor with high deposition rates (EPI-poly). However, the surface of the poly-Si is comparatively rough and disturbs the lithography process. In order to get sharp structures, a smooth surface is needed which has been achieved by performing a poly-Si CMP process. The challenge is getting a polished surface without loosing the alignment marks for the next lithography steps. Two different products have been realised using this technology. Figure 4a shows the poly-Si moving comb structure of an angular rate sensor, while in figure 4b the inter-digital structures of an acceleration sensor is pictured.

These examples prove that a demand on CMP processes for the fabrication of MEMS devices exists and is increasing in the near future with growing production. Modular CMP cluster tools like the Peter Wolters PM 200 Gemini fulfil the typical process requirements from the develop-ment lab to the production floor. Materials suppliers have addressed this trend and have optimised several slurries for MEMS applications. Meanwhile a number of MEMS-specific CMP processes have been developed and are available for customers.

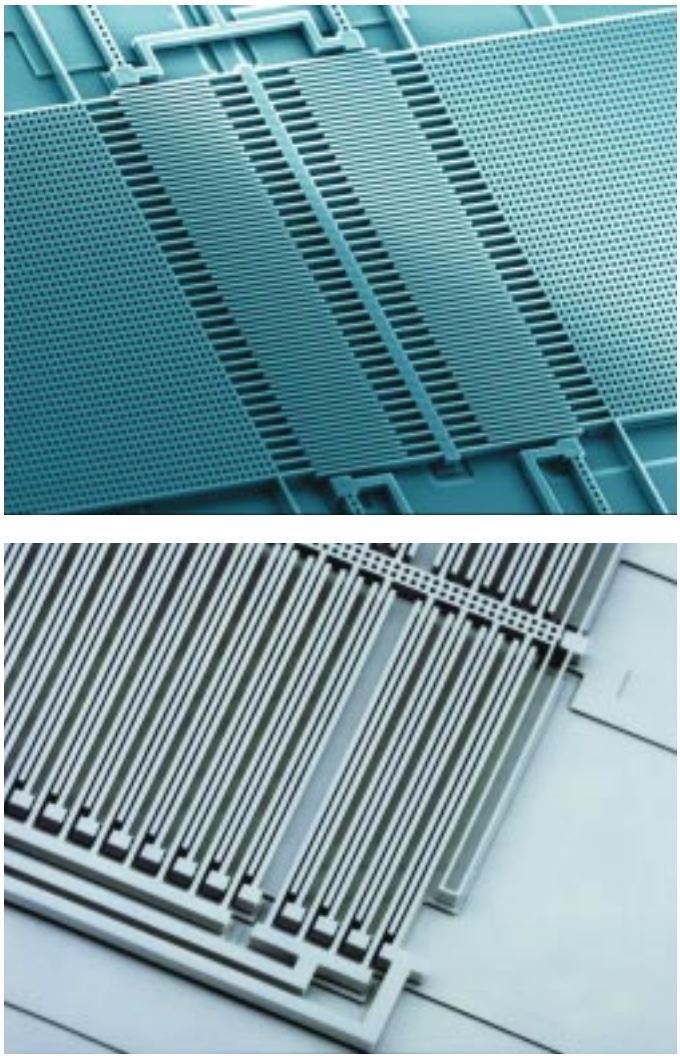


Figure 4:
Angular rate sensor (a) and acceleration sensor (b), both micromachined in poly-Si. The roughness of the 10 µm thick poly-Si has been eliminated by polishing before structuring.

Projection Mask-Less Lithography (PML2): MEMS-Technology for a Programmable Aperture Plate System (APS)

The fundamental technical performance challenge for direct write lithography is throughput. Whereas optical lithography (248 nm, 193 nm, 157 nm) and the successor EUV (13.5 nm) is expected to achieve 60 wafers per hour and more, present day e-beam lithography is typically two to four orders of magnitude slower. The limited throughput of e-beam lithography is caused by two factors, being the serial nature of the e-beam exposure process, and the limited, useable writing current. To overcome this limitation is the goal of the European MEDEA+ project T409 and the joint project "Abbildungs-methodiken für nanoelektrische Bauelemente – ABBILD" in Germany. The key is a massively parallel writing strategy with a few hundred thousand beams to meet the technical and economical requirements for fast prototyping and the fabrication of small and medium volume electronic devices with ≤45 nm minimum feature size. The primary innovations of this project will be the development of a 200 x reduction electron optical system equipped with a programmable aperture plate system (APS). A proof-of-concept tool will be built within the MEDEA+ project T409 by the key partners LEICA Microsystems Lithography GmbH (Jena), IMS Nanofabrication GmbH (Vienna) and the Fraunhofer Gesellschaft.

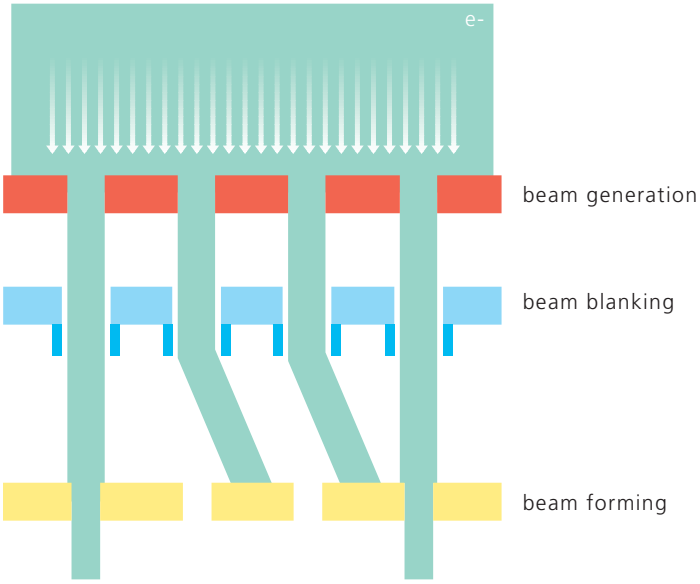


Figure 1:
Functionality of APS.

Concept of APS

The APS of the PML2 replaces the mask of a conventional lithography tool. Main component of the APS is the blanking plate, where electrical signals generate electrostatic fields according to the pixel data, in order to blank or unblank the individual electron beamlets. Other plates form the beamlets and correct the optical properties of the electron optical column (figure 1). A big number of apertures (about 300.000) generates a lot of single electron beams out of an expanded electron beam with about 1 inch diameter, which illuminates the complete aperture area of the first plate. The size of the beam forming apertures can be calculated to 5 µm x 5 µm taking into account a required pixel resolution of 25 nm on wafer level and a projection scale of 200:1 of the electron optical column. The Blanking Plate is driven by a stream of pixel data prepared off-line in advance and transmitted via a high speed optical data link from an outside storage equipment onto the plate. Using a specific driving electronics for each aperture every beam could be individually switched ON or OFF.

The project ML2-APS

The BMBF supported project ML2-APS (FKZ: 01M3154T) is part of the ABBILD-project. Within this project ISIT together with the Fraunhofer institutes IOF in Jena and HHI in Berlin have the goal to fabricate and assemble the single aperture plates including the optical data path and to finish at the end with a complete APS.

MEMS process

The Microsystem process development will focus on three key processes :

Figure 2:
General process flow
for a blanking plate.

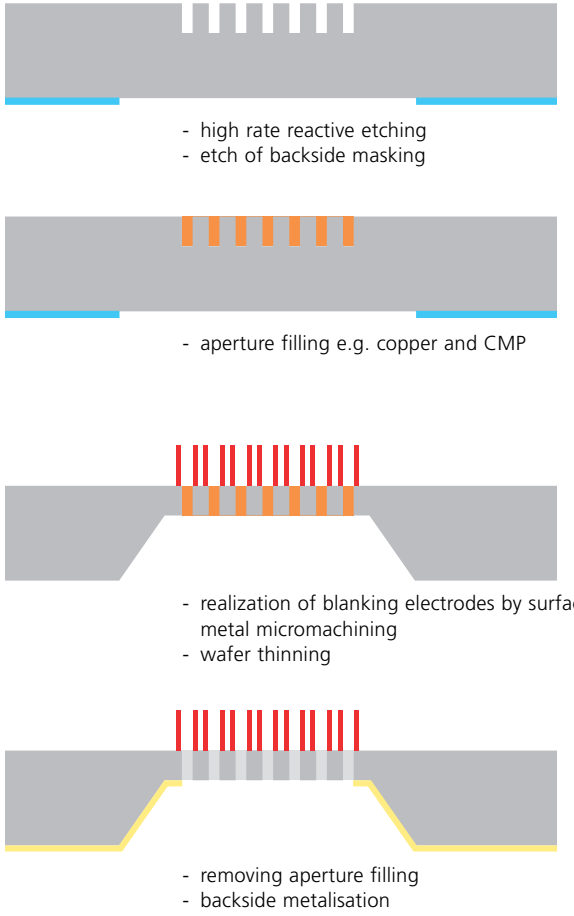


Figure 3:
Cross section of high rate reactive etched silicon apertures.

Figure 4:
Electroplated blanking electrodes 35 µm high.

- High rate silicon dry etching necessary for creating the apertures
- High aspect ratio electroplating for blanking electrodes
- Time controlled KOH silicon membrane etching for precise membrane thickness control

The fourth key point is the integration of these three single process modules into a complete process flow. Figure 2 shows the general process flow for preparing a blanking plate chip.

But before starting the whole process flow each single process step has to be optimized by its own. The requirements for good aperture performance are twofold. First having an aperture opening of 5 µm x 5 µm the egde radius has to be smaller than 100 nm. There standard widefield stepper with 0.8 µm resolution for MEMS application run into problems. This could only realized by OPC supported optical lithography or mix and match of optical lithography and e-beam lithography. Second requirement for aperture performance is the sidewall steepness over the 40 µm membrane thickness, which means an aspect ratio of better than 8. Therefore a high rate reactive etching process has been developed for the silicon apertures. Table 1 and figure 3 show the satisfying results.

The blanking is done by electrostatic forces. The available blanking voltage out of the monolithically integrated driving electronics is about a few volts. Together with a deflection angle of nearly 1 mrad the height of the blanking electrodes has been calculated to be in the range of 35 µm. Even the transparency of the aperture array (number of apertures per mm^2) should be improved because of its direct influence on the writing speed. Hence optical lithography in thick resist layers and electroplating of the blanking electrodes has to go to the limit. Based on an AZ type resist a process has been developed with 40 µm resist thickness, resolution of 8 µm and a resulting electrode height of 35 µm after gold electroplating. Figure 4 shows gold electrodes after resist removal.

Table 1:
Results of process development for high aspect ratio apertures in silicon

Aperture Ø Top [µm]	Aperture Ø Bottom [µm]	Depth of aperture [µm]	Sidewall angle [°]
10,0	9,1	94	89,7
5,0	3,9	73	89,5

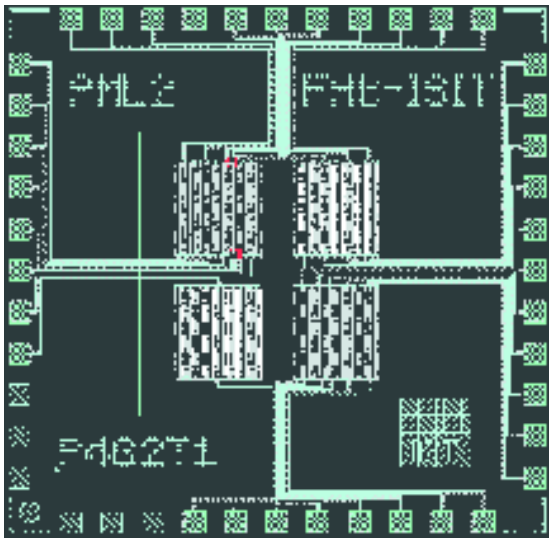


Figure 5:
APS Demonstrator:
Complete chip
design 8 x 8 mm²
in size.

Based on the result of the single process development the demonstrator mask design was carried out. Figure 5 shows a complete APS demonstrator chip design. The chip size is 8 mm x 8 mm and contains four aperture areas with 1000 apertures respectively.

After mask fabrication the complete flow for the blanking chip demonstrator was processed. The SEMs in figure 6 and 7 show good quality of the demonstrator process also when looking in details. First tests in the IMS teststand in Vienna result in good switching properties of the electrodes with an deflection angle of 0.25 mrad/V.

Design and layout of the monolithically integrated driving electronics

The very large amount of electrodes on the APS cannot be controlled by outside electronics which is connected to the MST-chip by bond wires or by flip-chip because it is impossible to directly connect more than several hundred electrical contacts. The precision for the switching of the beamlets must be very precise, i.e. in the range of nano seconds. The exposure concept foresees that the APS is able to switch about 300.000 electron beams at the same time while the wafer moves continuously. The amount of data to handle is in the range of several Tbit per second. Therefore only a monolithically integrated driving electronics next to the blankers is able to fulfil this challenge. The necessary memory, logic and driver for each aperture has only minimum space. To keep the mechanical precision the allowed bowing of the electronics as well as of the APS-plate due to heating has to be very small, resulting in an advanced electronic technology with low power dissipation. This means the electronic focus is on 180 nm CMOS technology which could only be dealed by an external provider which allows a supply voltage down to 1.25 V. In addition to the APS demonstrator an electronic demonstrator has been designed for testing memory, logic and driving electronics for the APS application (figure 8). It shows the dense layout of one aperture cell, designed on a 0.01 µm grid with the area for the aperture in the center of the upper part.

Assembly

The integration technology for the APS plates covers the assembly and interconnection of the electronics and microsystem components on the base plate (compare figure 9). According to the modular plate concept several components such as the aperture chips and the hybrid electronic chip have to be mounted and electrically connected to the base plate. The assembly of the aperture plate system consists of three independent tasks:

- Wafer bonding of support frame and base plate wafer
- High precision chip stacking with less than 1 µm positioning error
- Assembly of the electrical and micromechanical components on the base plate wafer

Figure 6:
Detail of a complete
demosntrator
chip with apertures and
blanking electrodes.

Figure 7:
Top view of figure 6.

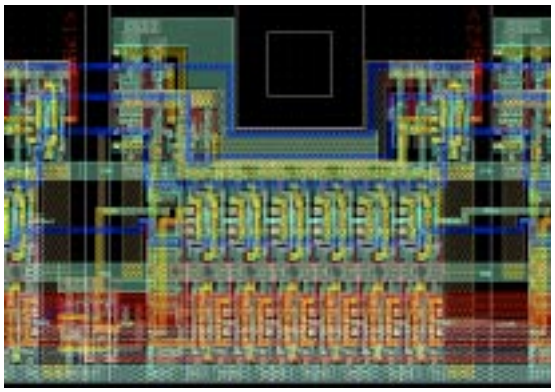


Figure 8:
Electronic layout for one aperture cell.

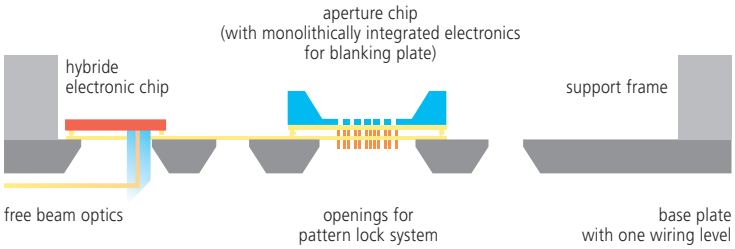


Figure 9:
Modular plate concept for the APS, base plate with hybride electronics and monolithically integrated blanking chip.

A key issue of the aperture plate system is the geometrical stability of the stack. Therefore a 5 mm thick support frame is used as stiffener for the base plate wafers. To minimize the effect of inhomogeneous temperature loads a very good thermal conductivity combined with a low coefficient of thermal expansion (CTE) is required. No adhesives can be used since the vacuum compatibility cannot be guaranteed under heavy electron exposure. The prefered solution is AuSi eutectic bonding which fulfils all requirements with regard to electrical and thermal conductivity, vacuum compatibility, and easy process integration.

The design of the APS plate systems contains stacked dies with a relative placement accuracy of better than 1 µm. This precision exceeds the requirements for common high precision bonding of optical fiber components. Some equipment manufacturers specify an application dependent accuracy between 0.5 µm and 1 µm. Furthermore a solder connection with a high melting point has to be used since the whole stack has to withstand a reflow process during the assembly of the base plate wafer. Possible solders are eutectic or intermetallic AuSn alloys.

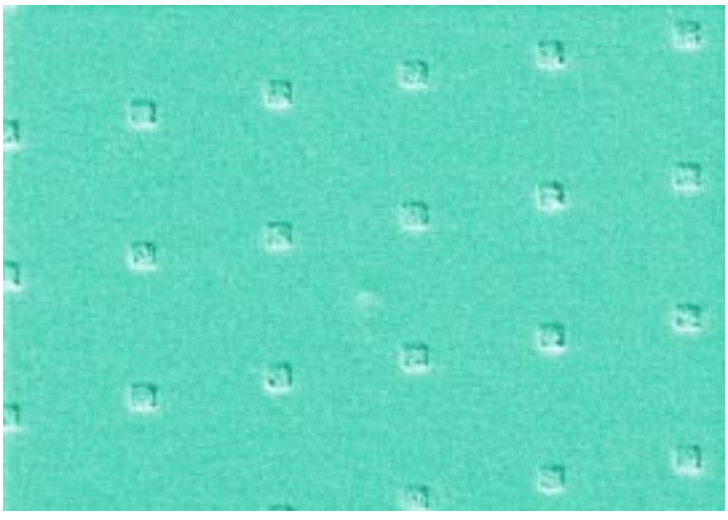
Exposure experiments

First aperture arrays have been used for exposure experiments in an Ion Projector System to inspect completeness of all produced apertures and their quadratic shape. This could be done because ions travel in electrostatic fields on the same paths as electrons because they are at the same energy much slower so that the mass effect is compensated. The exposure with 9 x demagnification showed undistorted images of the square holes in the resist as demonstrated in figure 10.

Next steps

For each of the above described working fields, the MEMS process, the monolithically integration of the driving electronics and the assembly of all components for the modular plate concept, demonstrators have been defined and realized. The actual status of evaluation of the available results from the defined demonstrators show good performance. This fact makes the realisation of a fullsize APS in the next step very promising.

Figure 10:
Ion exposed resist using an aperture array as a mask.



Microscanners for Mobile Laser Projection Displays

For several years already there is a steady tendency to more and more scale down the size of mobile phones. But at the same time the demand for larger image size and higher resolution of the mobile displays increases. A clever solution to meet these two colliding requirements is to integrate a tiny laser scanning projection display into the mobile phone. The size of the projected image then only depends on the projection distance and thus can be several times larger than the mobile phone itself. Based on more than ten years of experience in design and fabrication of optical MEMS Fraunhofer ISIT has developed a miniature two-axes microscanner chip that deflects a laser beam in a fast raster scan for image projection.

The microscanner consists of a movable silicon mirror plate that is suspended by thin torsional beams in a frame that itself is movably suspended in a fixed chip frame. Boths axes of the scanner are actuated by electrostatic forces. While the mirror plate is driven in resonant mode at 4kHz the surrounding flexible frame typically is driven quasistatically at a frequency of 30Hz. Using continueous bidirectional scanning 8000 image lines are projected per second. A high sophisticated electronics measures within a few nanoseconds the instantaneous 2D-deflection of the scanner and reads out the corresponding pixel intensity from the image memory for correct intensity modulation of a small laser diode. With that kind of configuration the laser modulation is synchro-

Figure 1:
An integrated tiny laser projection display will be able to produce images that are several times larger than the mobil phone.

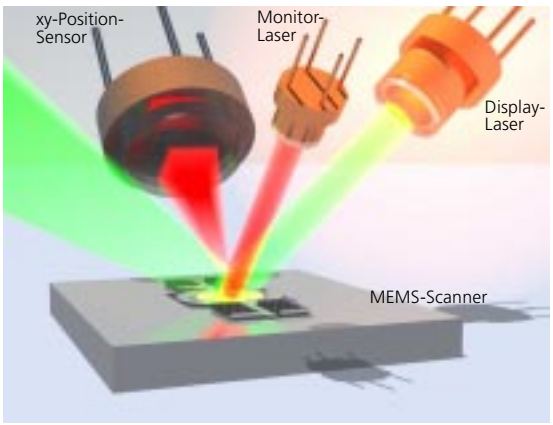


Figure 2:
a) The core components of the miniature laser beamer: A two-axes microscanner chip and a laser diode.
b) Using a second laser beam and a position sensitive diode the xy-position of the mirror gives a high resolution position feedback.

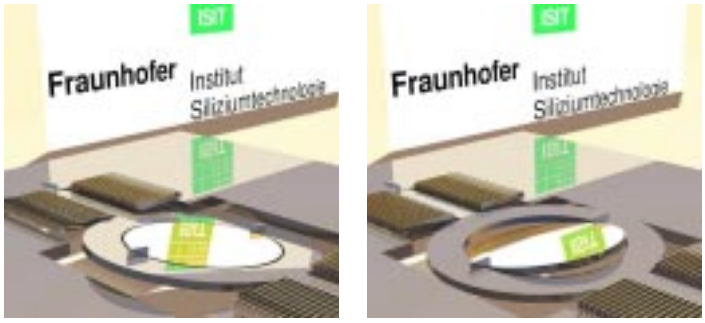


Figure 3:
a) Applying a voltage to the vertical comb electrodes leads to a quasistatic deflection of the slow axis.
b) Applying an AC-voltage to the vertical comb electrodes of the mirror leads to mirror oscillation.

nised to the mirror movement at any time and unpredictable impacts, vibrations or temperature drifts are easily compensated without image distortion. But in addition that control electronics also offers the capability to use a lissajous scan instead of a raster scan which can have several advantages, e.g. larger image size, higher scan frequencies and less jitter. In order to demonstrate the imaging capabilities of that microscanner a microprojector with a resolution of 512 x 256 pixels was set up.

The microscanner chip has a size of only five by five millimeters which allows the dimensions of such a miniature laser beamer to be reduced down to sugar cube scale. Each processed silicon wafer consists of 500 scanners therefore the fabrication process enables cheap mass production of these microscanners which is important for consumer applications. Other than that mentioned application in mobile phones such a miniature laser projector becomes of interest also for the automotive industry for use in head-up-displays.

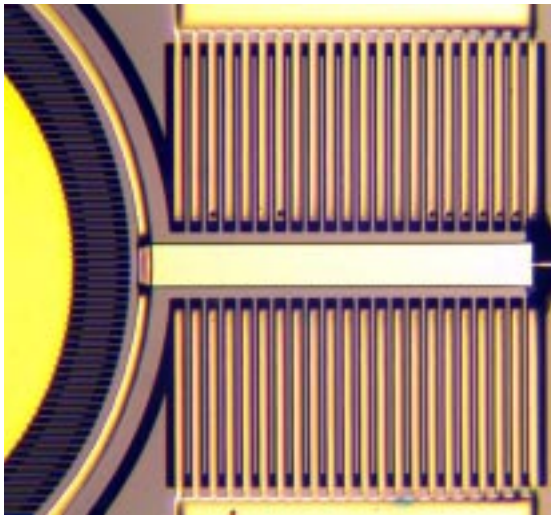


Figure 4:
Detail view of the two axes mirror chip that shows the tiny comb electrodes of the mirror and larger electrode structures of the second axis.

Specifications of the 2D-Scanner-Chip:

chip dimensions:	5 mm x 5 mm x 0.5 mm
mirror size:	1.5 mm ∅
mirror scan frequency:	> 4 kHz
gimbal scan frequency:	0..500 Hz
mirror scan range:	+/- 12°
gimbal scan range:	+/- 8° (quasistatic) .. +/-20° (resonant)
actuation voltage:	< 80 V

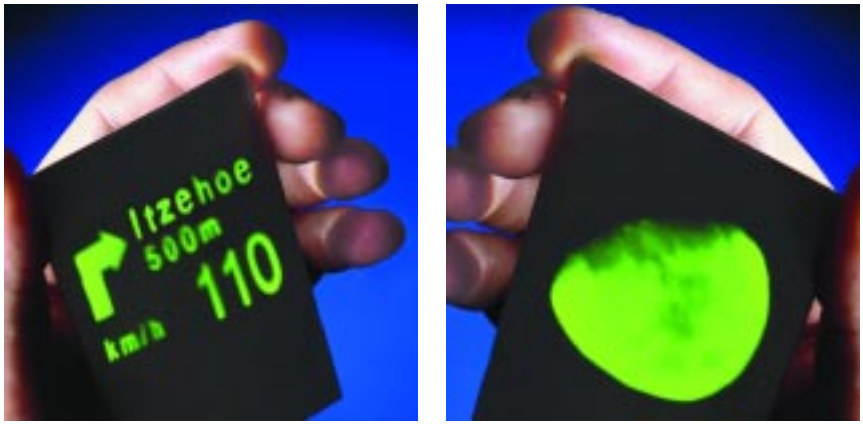


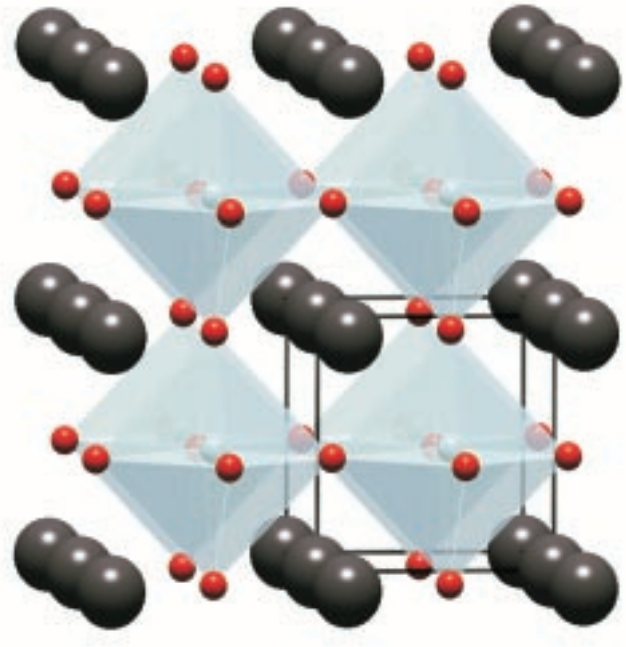
Figure 5:
Two examples of projected images (graphical test image and the moon). For a better visibility a green laser source was used.

Development of a New Sputter Process for the Deposition of Piezoelectric Layers for MEMS-Actuators

Despite the fact that the fabrication of thin film PZT $Pb(Zr_x Ti_{1-x})O_3$ is a field of intensive research activities, the fabrication of thin films made of PZT is still a big challenge. Methods like screen printing or even bonding and grinding of bulk PZT plates are very limited. Screen printing requires a very high firing temperature to achieve a void free film and due to chemical reactions of the evaporated lead of the PZT the silicon substrate is damaged. Bonding and grinding allows the manufacturing of approx. 20 µm thick PZT but it is a very expensive way for the integration of the PZT material and due to thermal mismatch of the PZT to silicon very often cracks occurred.

Commonly used thin film deposition techniques like MOCVD (metal organic chemical vapour deposition) magnetron sputtering or sol-gel suffers all from the low deposition rates. For magnetron sputtering a max. sputter rate of 5 – 15 nm/min are reported while the published results for MOCVD are in comparable ranges. On the other hand sol-gel techniques are offering at the first sight a very attractive way for the deposition of PZT since these techniques can be applied without the use of expensive tools, however a more detailed consideration shows some severe drawbacks. First single sol-gel layers must be very thin (typical 50 nm – 200 nm) to avoid the development of cracks during the followed thermal annealing. To achieve thicker layers it is necessary to repeat the spin-on of the gel layer and the annealing at approx. 700° C each time. Secondly the resulting layers have nevertheless very often cracks and defects due to the continuous handling of the soft gel layer prior to annealing. Beside the difficulties to avoid defects in the fabricated PZT layer, the sol-gel deviated PZT layer showed very often a gradient in their chemical composition caused by the evaporation of lead during the various annealing steps. So in fact industrial applications of thin film PZT material used in an actuator are very rare and limited. However PZT as actuator material has an enormous potential for use in MEMS devices. Microactuators like valves, relays, ink-jet print-heads, micromirrors, filters etc. driven by the piezoelectric effect of PZT are only a small fraction of possible applications.
The piezoelectric drive allows the realisation of actuators with large forces at high frequencies and low energy consumption.

Figure 1:
This figure shows the lattice of a Perovskite Type material. The dark atoms are Pb, red is oxygen and in the middle of the common used unit cell is Zr or Ti.



To overcome these limitations Fraunhofer ISIT started a close co-operation with Fraunhofer IST to develop a high rate sputter process for PZT based on the Gas Flow Sputtering technique invented by Fraunhofer IST. The Project is funded by Ministerium für Wirtschaft, Arbeit und Verkehr des Landes Schleswig-Holstein.
The Gas Flow Sputter technique uses a specific cathode arrangement to produce a high density plasma (figure 2). An argon gas flow transports the material towards the substrate.

A reactive gas can be added outside the cathode if required. Due to the separation of the discharge from the reactive gas a chemical reaction of the target surfaces with the reactive gas can be avoided.

Compared to the conventional magnetron sputter process the gas flow sputter technique enables very high deposition rates especially for oxides and nitrides. The sputter cathodes for the deposition of a complex material can be realised by a set of segments made of the different elements.

A target consisting of the three metals (Pb, Zr, Ti) was used in the experiments to deposit PZT (figure 3). The oxygen was added as reactive gas beyond the cathode. Since the cathode arrangement delivers a non-homogeneous plasma density resulting in a non-uniform film thickness the substrate is moved perpendicular to the plasma jet during the sputter process.

Characteristics of the GFS process:

- hollow cathode discharge
- sputtering of the inner surfaces of the cathode
- transport of material by an Argon flow
- inlet of a reactive gas beyond the hollow cathode

Using an extremely low power level of about 600 W sputter rates of 200 nm/min were observed allowing the deposition of PZT films with a thickness up to 6 µm within 30 min (figure 5). Even much higher sputter rates seems possible

Figure 2:
Scheme of the GFS process.

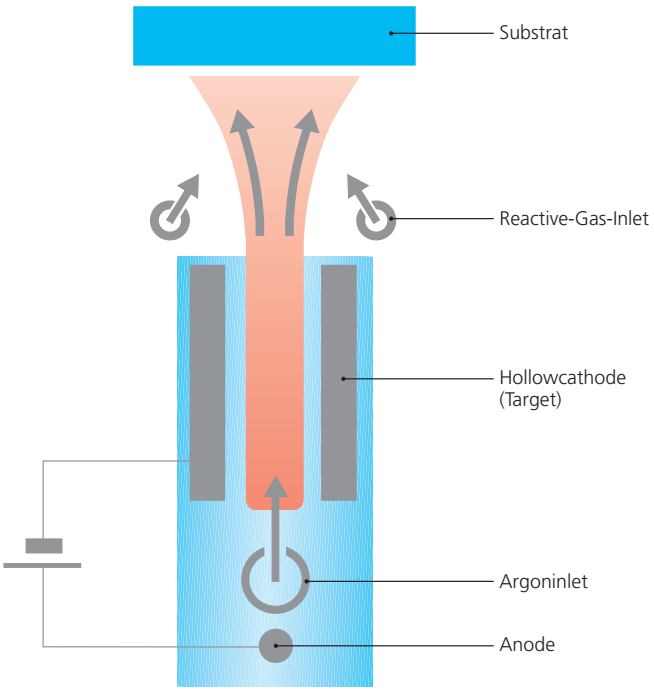
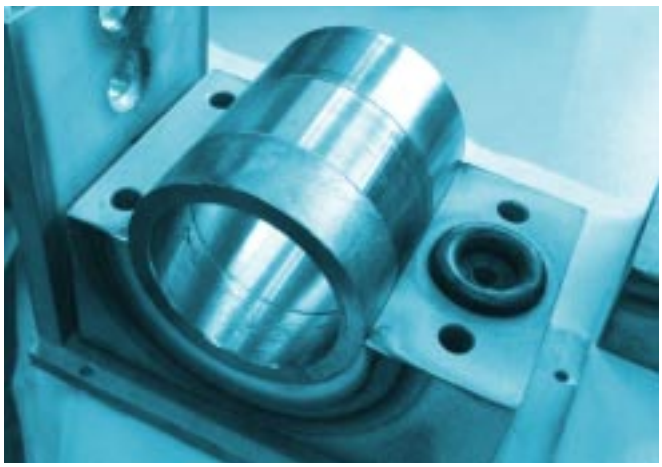


Figure 3:
Composite target existing of three element rings (Pb, Zr, Ti).



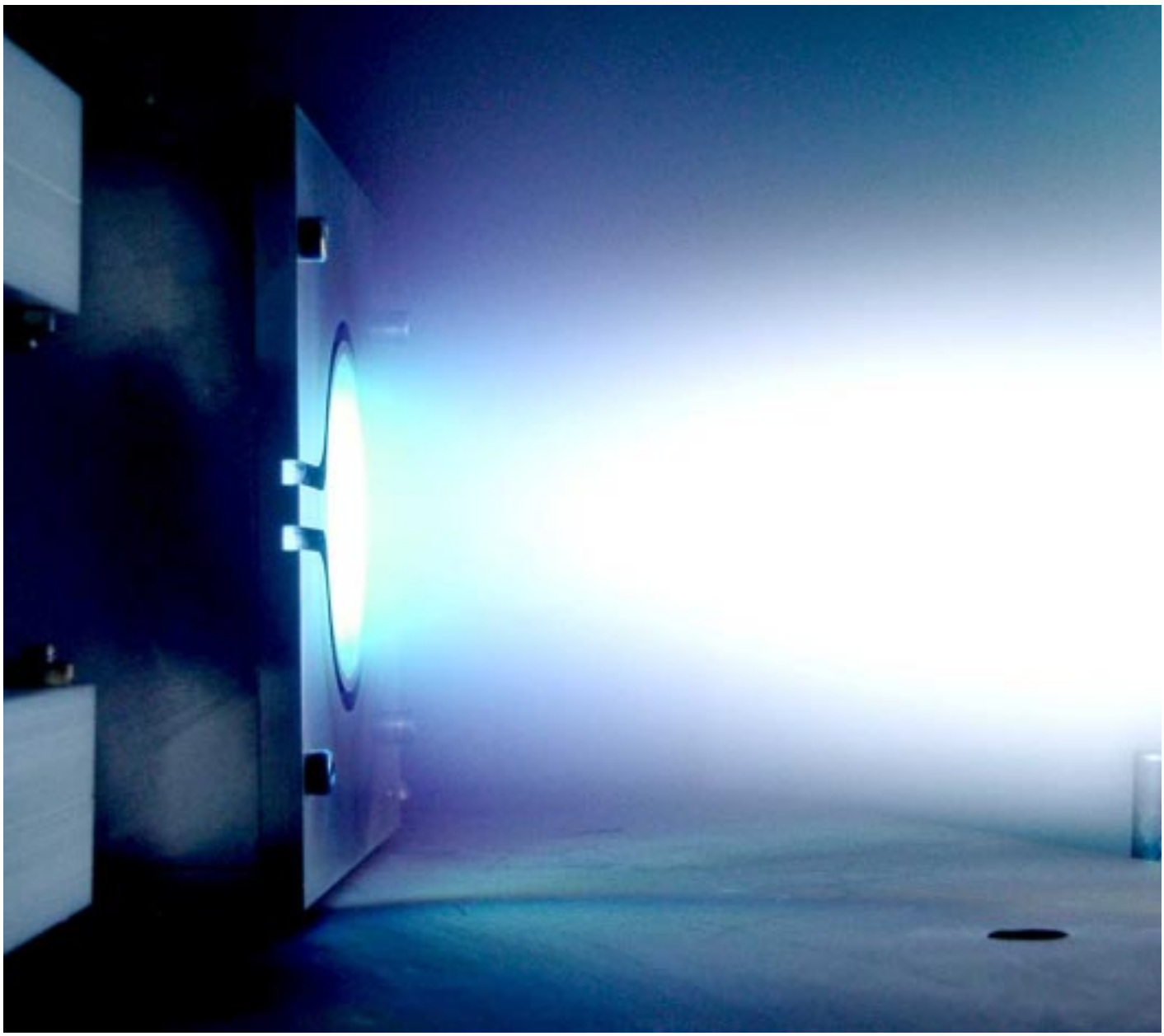


Figure 4:
GFS Source in
operation.

since only a small fraction of the available power level is operated. The deposited PZT films were crackfree up to a thickness of 7 – 8 µm.
The produced PZT layers were characterised with a variety of analytical methods including SEM (Scanning Electron Microscope), EDX (Energy Dispersive X-ray), EPMA (Electron Probe Micro Analysis), SIMS (Secondary Ion Mass Spectroscopy), XRD (X-ray Diffraction) and TEM (Transmission Electron Microscope). High piezo-electric coupling coefficients require an optimum ratio of Zr/Ti = 0.52/0.48 (morphotropic phase boundary). Many parameters like length and arrangement of the targets, flow of the argon and oxygen and the used power level have shown an influence on the composition of PZT films. Final results from EPMA measurements on deposited PZT samples demonstrated a stoichiometry near to the target composition (figure 6).

Measurements using XRD showed that the PZT film consists of small crystals (figure 7). Furthermore more detailed experiments resulted that heating the substrate increases the level of the crystallinity of the deposited film as well as an additional post sputter annealing step. Beside the tests on the chemical composition or the crystallinity electrical tests especially for determining the piezoelectric coupling coefficients d_{15}, d_{31} and d_{33} are still on going. First measuring results of the dielectric constant ε_r of the thin film was found to be over 500. Only perovskite type materials have got such high values. Despite the preliminary stage of the work it could be noticed that the studied new PZT sputter process based on the gas flow sputtering is very promising and will probably lead to a broad range of new application in MEMS.

Figure 6:
EPMA measurements.
The stoichiometry would be perfect, if the ratios of $Pb/Zr/Ti/O_2$ would be 20/10,4/9,6/60.

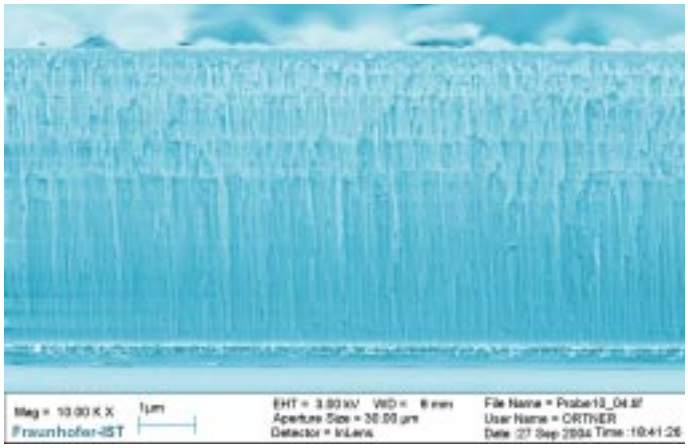
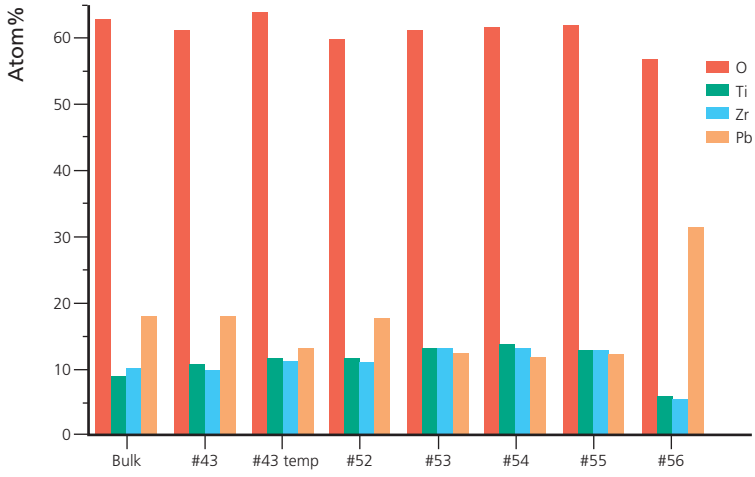


Figure 5:
Cross section of a PZT layer.



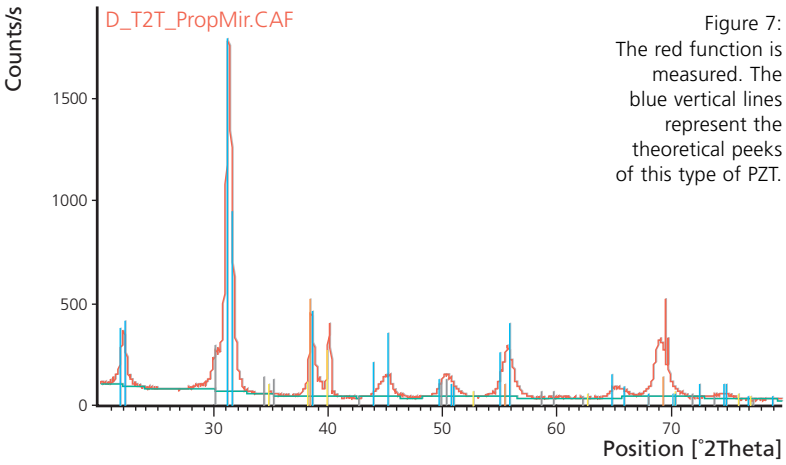


Figure 7:
The red function is measured. The blue vertical lines represent the theoretical peeks of this type of PZT.

MIMOSA: Microsystems Platform for Mobile Services and Applications

MIMOSA is an European Commision funded Integrated Project in the frame of the Information Society Technologies Programme, contract number IST-2002-507045, in the Sub-programme Micro and Nanosystems. The key figures are

- 15 partners from 7 countries
- co-ordinator: ST Microelectronics , France
- total budget: 23.2 Mio €; EC funding: 10.0 Mio €
- duration: January 2004 - June 2006
- http://www.mimosa-fp6.com

The MIMOSA objective is to create a new open system platform for context-aware mobile services and applications. MIMOSA extends the area of telecommunication business to Ambient Intelligence, i.e. a functional environment in the background surrounding and supporting the user. Ambient Intelligence includes a multitude of interconnected sensors and smart tags providing information that can be utilised in mobile applications as such or as an index to Internet or local services. The MIMOSA approach is mobile phone based and strongly human-centred, providing the users with a smooth transition from current mobile services to Ambient Intelligence services.

End users and application developers participate in designing and evaluating how Ambient Intelligence and short-range communication

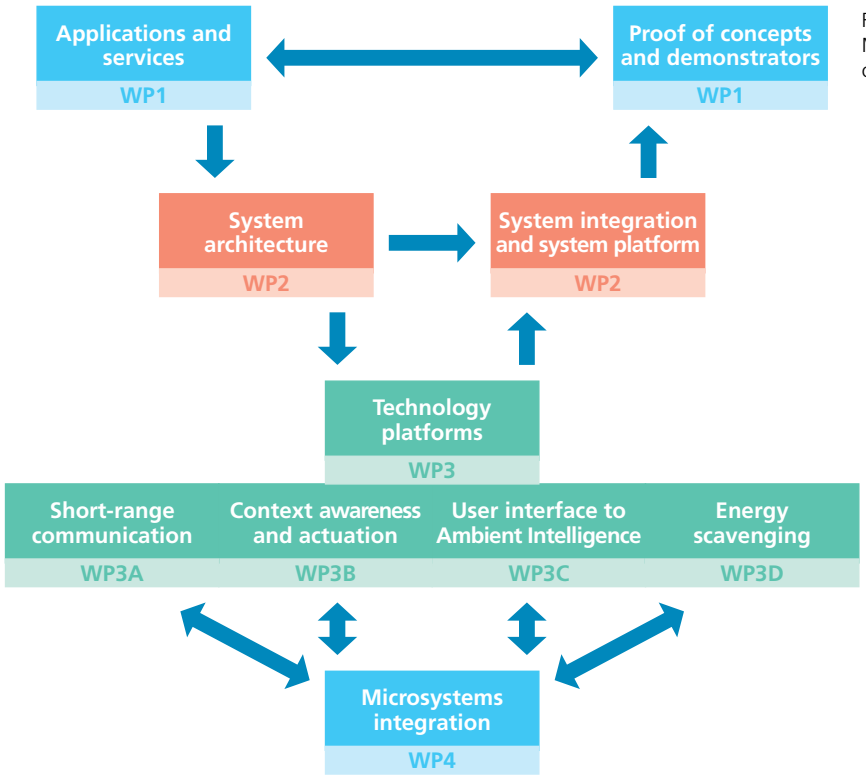


Figure 1:
MIMOSA project organisation.

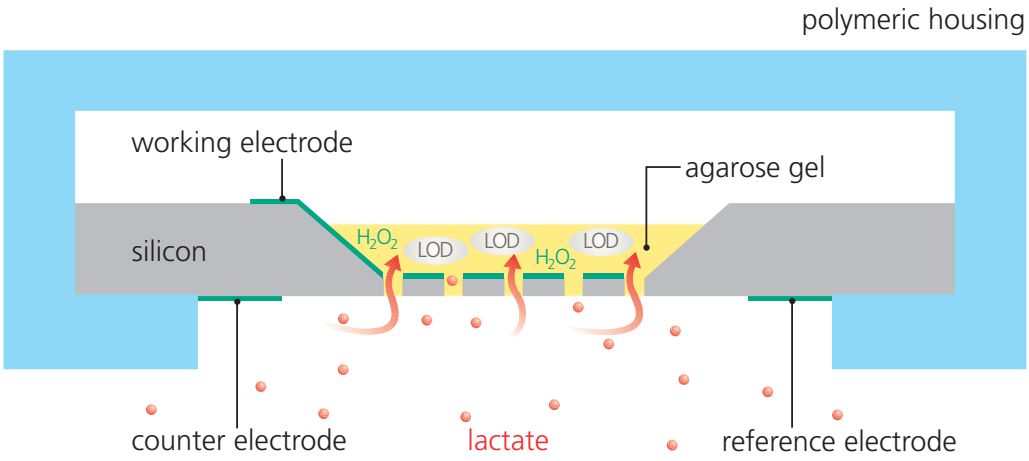


Figure 2:
Priciple of the lactate sensor.

with environment could be best utilised in the everyday life. To demonstrate the generic characteristics of the platform, MIMOSA develops specific applications with particular emphasis on physical browsing, health monitoring, intelligent housing, fitness/sports, context awareness for Ambient Intelligence and intuitive user interfaces.

In the area of short-range connectivity, MIMOSA positions itself to low-cost, low-bit rate territory that can be set up with relatively modest investments in the infrastructure. A focus of MIMOSA is the development of novel low-power microsystems, in particular wireless sensors exploiting the RFID technology, highly integrated readers/writers for RFID tags and sensors, low-power MEMS-based RF-components and modules and low-power short-range radios.

Ultraminiaturized low-power sensors and novel intuitive user interfaces to Ambient Intelligence are crucial for usability. The contribution of Fraunhofer ISIT focuses on these workpackages. For the fitness and sports application a continuous lactate sensing device is being developed. The MIMOSA vision is to integrate this sensor in a smart plaster system including a wireless communication link to the mobile phone. The amperometric silicon-based lactate sensor contains the lactate oxidase as a catalyst (figure 2). To achieve a painless transfer of interstitial fluid through the skin, a polymer microneedle array, investigated by AMIC AB from Uppsala, will be integrated in the sensor module.

A second sensing task is on low-cost inertial measuring units (IMU). These units, measuring accelerations and angular rates in three dimensions are able to serve as inertial user interfaces or as motion monitoring devices in sports and fitness. The underlying MEMS technology of the IMU has been described elsewhere in this annual report (see page 54). The work in MIMOSA focuses on new sensor designs and low-power sensor interfaces for the mobile application.

The work on new user interfaces to Ambient Intelligence divides in optical, acoustical and inertial UIs. Fraunhofer ISIT contributes mainly in the optical section with the development of an micromirror-based laserscanning micro-projector which is described in a separate chapter of this report (see page 46).

Representative Results of Work Microsystems Technology and IC-Design

Surface Micromachining Process Platform for the Development of Inertial Measurement Units (IMU) in Automotive Application

The detection of inertial motion like acceleration and rotation is widely used in automotive industries for the control and stabilization of vehicle dynamics like Airbags, Electronic Stabilization Program (ESP) or car navigation systems. At present each functional subsystem has its own integrated sensor system. Providing an all-in-one sensor solution for the concurrent measurement of all 6 degree of freedom of inertial motion in a single Inertial Meassurement Unit System (IMU) is the ambitioned mid-term objective on the automotive technology roadmap (figure 1). This central IMU will then be providing all relevant motion data to a multitude of automotive subsystems.

For single or dual axis sensors the MEMS technology has already a broad market share due to the inherent superior performance in measurement accuracy, costs and reliability. Next to continuous perfomance improvements by design and technology optimisation common future trends for MEMS inertial sensors will be cost and size reduction by more complex technology integration like the implementation of a sensor packaging process on wafer level.

At Fraunhhofer ISIT the surface micromachining process PSM-X2 has been established, which allows the production of MEMS devices such as vibratory gyrometers or accelerometers whereas

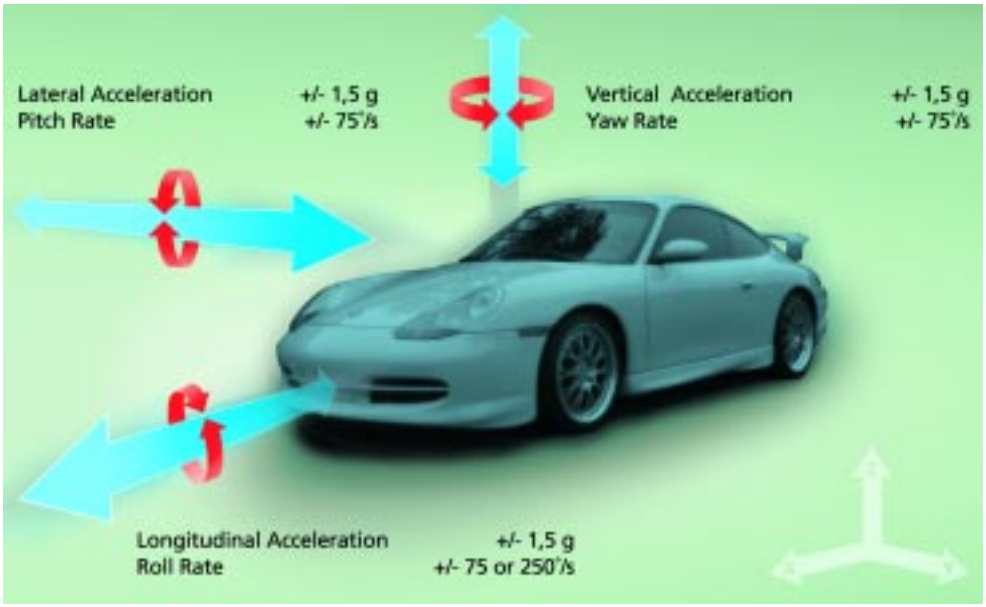


Figure 1:
Degrees of freedom for inertial motion and measurement range for automotive application.

Active Layer Thickness	e.g. 11 µm
Min. Feature Size	2 µm
Electrode Spacing	1,5 µm
Operating Pressure Range	1 µBar < p < 1 Bar
Total Device Thickness	1,2 mm

Table 1:
PSM-X2 key figures.

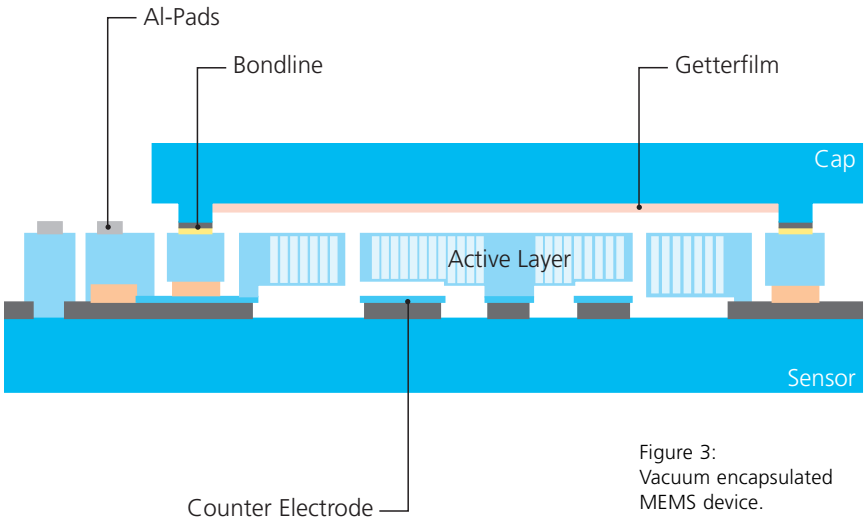


Figure 3:
Vacuum encapsulated MEMS device.

the mechanical active structure is formed by e.g. an eleven micron thick poly silicon layer (figure 2). An in-plane motion can for example be achieved by electrostatic actuation of electrode finger structures. For the detection of out-of-plane deflection an underneath conducting layer is used as counter electrode. To maintain a defined operating pressure condition and to protect the poly silicon microstructures from mechanical damage and particel defects a wafer-level packaging process is performed by using eutectic gold-silicon bonding. In this step a cap wafer with anisotropic etched cavities is aligned and bonded to a sensor device wafer.

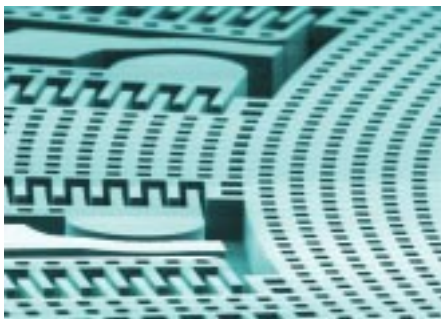


Figure 2:
MEMS active layer:
11 µm thick
polycrystalline Silicon.

The gold-silicon bonding line shows excellent gas hermeticity and leakage rates below 10-13 mBar xl/s. Superior vacuum conditions are achieved by the integration of a thin getter film in the cap wafer cavity above the sensor structure. A cross section of a final chip device is seen in figure 3.
The sensor package is robust enough to fulfill the high quality standards of automotive industry. Applying the process PSM-X2 gyrometers and accelerometers with appropriate sensor performance have been demonstrated (figure 4).

In the PSM-X2 process a broad geometry flexibility of the MEMS structure together with a high operation pressure bandwith is combined. Since the IMU requires different sensor designs and concepts this process platform is uniquely suited for their common production. Future work will incorporate the integration of 3D accelerometers and 3D gyrometers in a one chip solution.

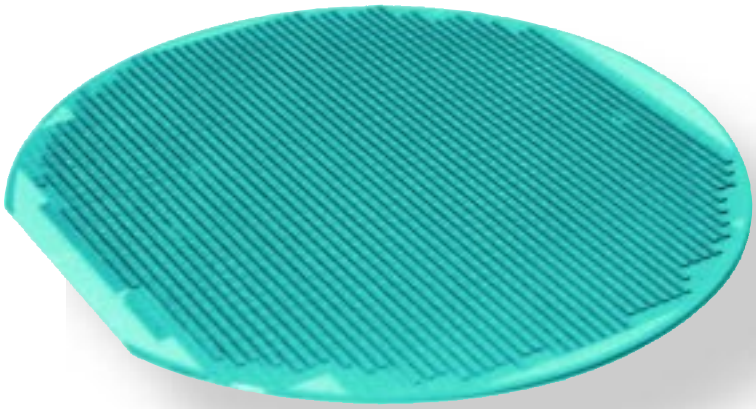


Figure 4:
Wafer level packaged MEMS wafer with gyrometer devices, manufactured with PSM-X2

Representative Results of Work
Microsystems Technology and IC-Design

Training Course for MEMS Design

ISIT has a long history of developing various processes, technologies and products of microelectronic mechanical systems, MEMS. The institute contributes to the dissemination of advanced MEMS technologies by scientific publications, conference articles, presentations – at exhibitions and at direct contacts to enterprises. Especially the transfer of MEMS technologies to companies and first time users was supported during several years by the European Union within the EUROPRACTICE programme. One result of the good visibility of ISIT as a MEMS technology provider was an increase in the number of requests from countries outside of Europe. One such request came from the Malaysian institute for microelectronics MIMOS, Kuala Lumpur. This institute has in the past already cooperated with institutes from the Fraunhofer network microelectronics on CMOS technologies. Now MIMOS wants to investigate and build up competencies in microsensor and MEMS technologies. To prepare such technology transfer the idea was born that MIMOS engineers should become experienced with surface micromachining by preparing designs for several devices that are later produced within ISIT. A training course for that was set up and organised within ISIT and office space and working places were prepared for MIMOS employees in Itzehoe. Four MIMOS engineers with design experience in microelectronic circuits have visited ISIT from September to December 2004. They were instructed to use ISIT design tools to design several acceleration sensors with readout circuitry making use of the ISIT polysilicon surface micromachining process. The design process included mathematical calculations and

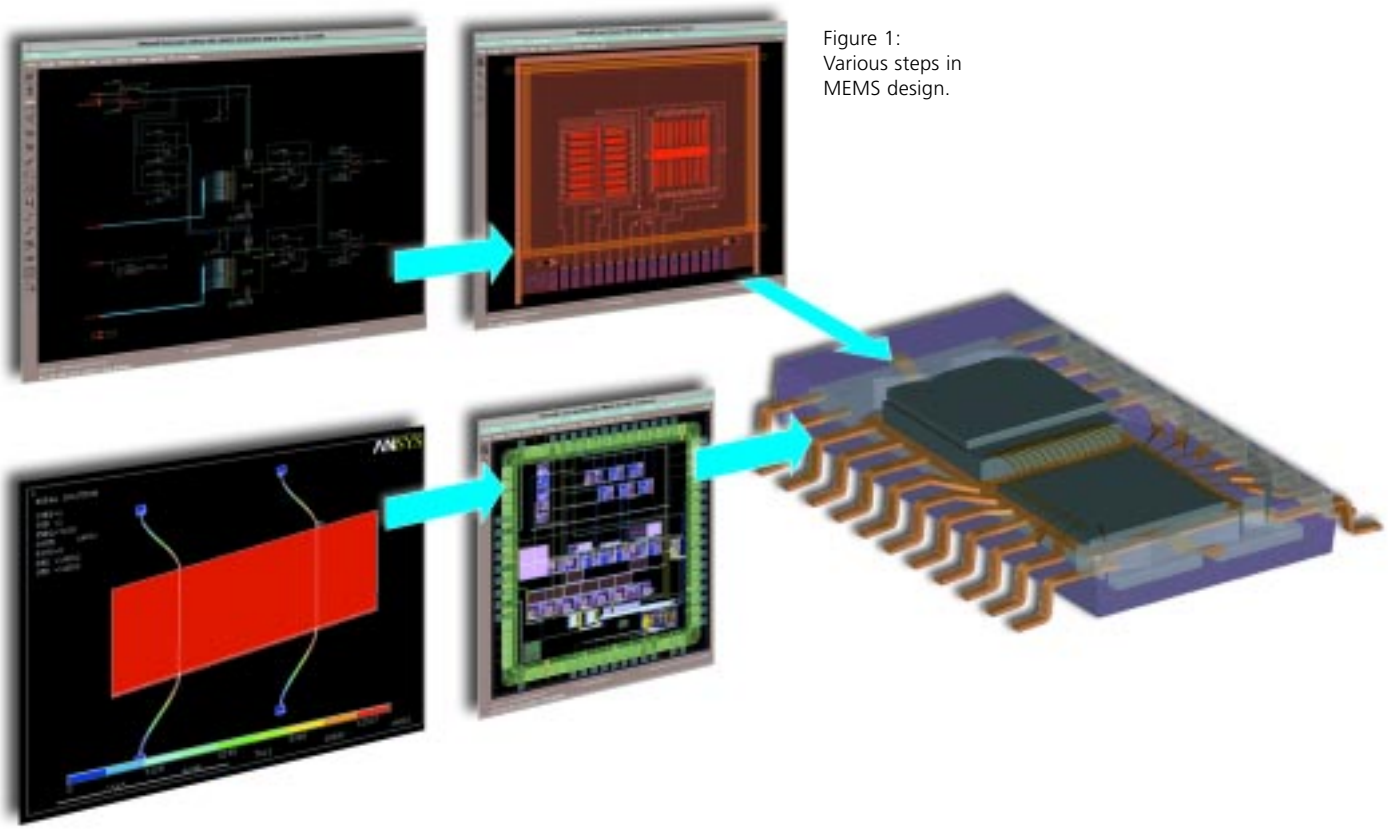


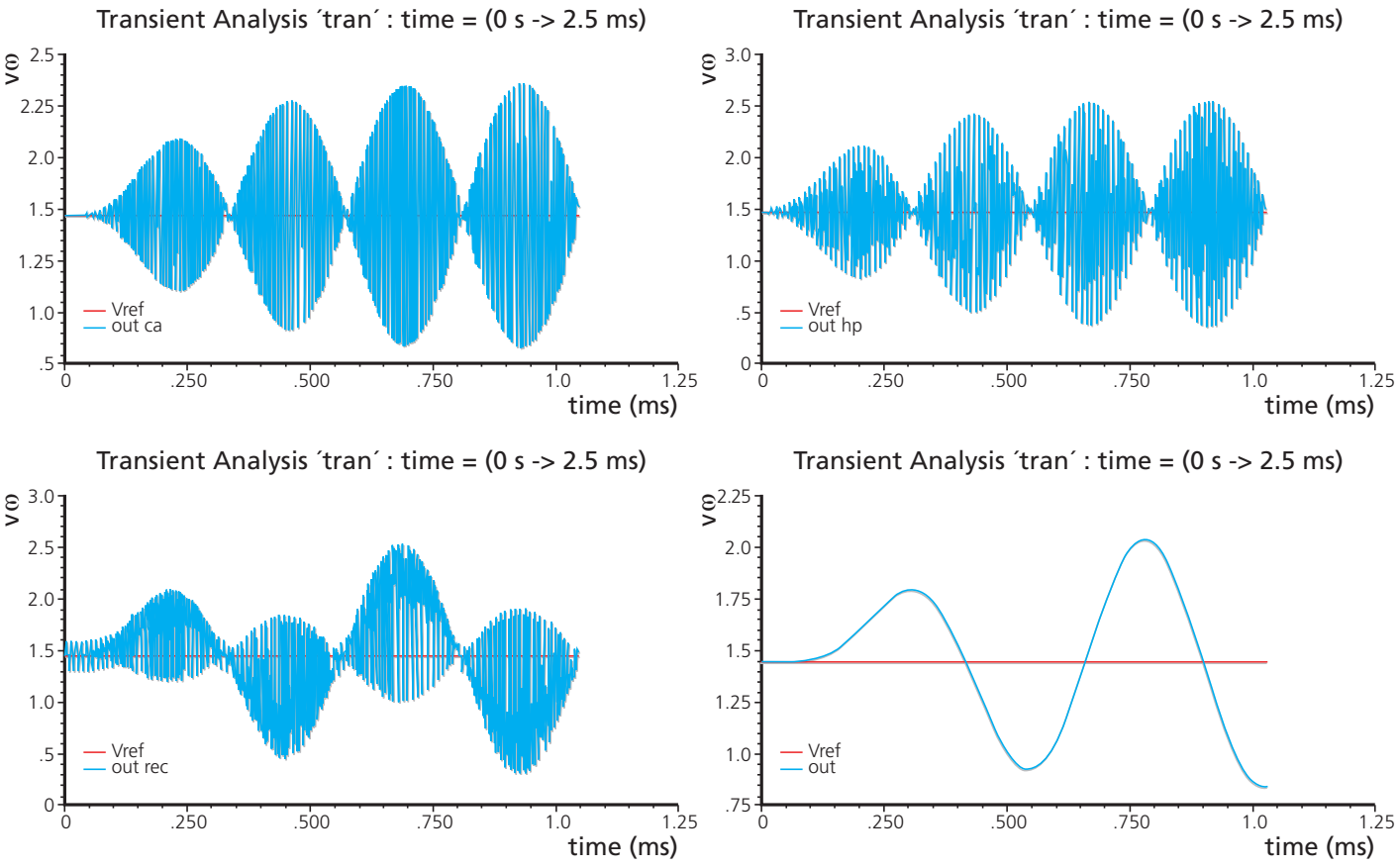
Figure 1:
Various steps in
MEMS design.

FEM simulations to achieve given specifications, the translation of this information into a CAD layout as well as into a behavioral model to be able to simulate the sensor with an electrical simulator. With the aid of this model it was possible to design and simulate a well-suited read-out circuitry.

The sensor designs are now being manufactured by the ISIT MEMS technology. With finished samples of their own designs MIMOS will build up test set-ups to measure and characterise the final devices. With this specialised training programme MIMOS engineers have gained first hand experience in MEMS technologies and can come to a more precise decision which directions of technology development are best suited for the demands of the Malaysian industry. Transfer of MEMS technologies from Itzehoe to Kuala Lumpur that are finally identified by MIMOS will be the central point of future project ideas and negotiations.

The successfully executed training course for MIMOS engineers is a new working field for ISIT. This experience will help to decide whether such an enlargement of the ISIT training offers is a reasonable extension of the training programmes already offered for companies in the field of packaging and interconnection of integrated circuits. Increasing demand for MEMS design technologies is an indication of the broadening application and market acceptance of MEMS technologies.

Figure 2:
Simulation of
MEMS devices.



Pathogen Detection on Electrochemical Microarrays

The detection of pathogens is today as important as it has been in the past. One top issue is the threat of bioweapon attacks by terrorist organisations with microorganisms like anthrax (*Bacillus anthracis*). Another topic are new evolving pathogens, causing severe diseases, like SARS and bird flu epidemics and also antibiotic-resistant microorganisms. Bacteria strains, like methicillin resistant *Staphylococcus aureus* (MRSA), can cause life-threatening surgical wound infections and can become a serious problem within the healthcare system. Methods for routine identification of microorganisms take at least several hours, a day or even more and are therefore of little use in giving fast needed answers (figure 1).

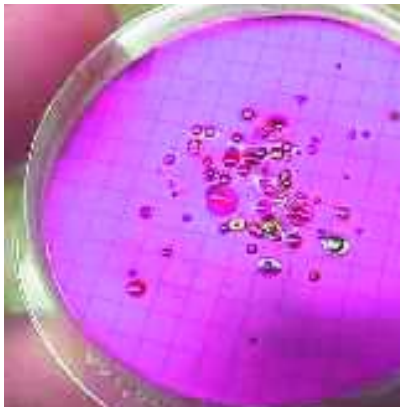


Figure 1:
Escherichia coli and cultiviation plate.

That is where modern analytical techniques, combined with molecular biology, offer substantial benefits. The development of electrochemical microarrays with ISIT's high-end silicon technology together with portable instruments for on-site analysis in our group are the basic tools for this purpose. Offering easy handling and fast results, we adapted the established biochip platform to two different strategies as examples for highly sensitive, nucleic acid based pathogen detection.

All nucleic acid based applications start with the immobilisation of target specific capture oligonucleotides to individual interdigitating gold ultramicroelectrodes on the biochip. Specific recognition on a certain position occurs through hybridisation with a directly or indirectly biotin-labelled target, present in a given sample. The biotin-label mediates the affinity binding of the enzyme conjugate ExtrAvidin®-alkaline phosphatase. The enzyme itself initiates a site-specific, electrochemical reaction on the electrode with the substrate p-amino phenyl phosphate, called redox-recycling. On electrode positions with enzyme a characteristic current profile is monitored and used for detection with a 16-channel potentiostat. Starting after the isolation of the nucleic acid material, the typical analysis program takes around 30 minutes.

The first strategy targets ribosomal 16S RNA from bacteria responsible for different widespread urinal tract infections. The 16S rRNA is present in bacteria cells at a high copy number around 20.000 per cell (E. coli), leading to a detection limit of 10.000 cells/mL.

The method is most straightforward in applications where enough nucleic acid can be isolated. The total RNA is directly extracted from the cells and bacteria specific analysed on the electrodes after a few steps. 16 of such microelectrodes are arranged into a precisely fabricated microarray on a silicon based biochip, that is coated with target specific capture oligonucleotides. In a set-up for 5 different bacteria species, 3 positions each or a total of 15 are used for pathogen

identification, the last position is an internal positive control. The sample scheme and an example for the positive detection of 16S rRNA of *Staphylococcus aureus* is illustrated in figure 3.

The second nucleic acid based strategy includes a very important tool in molecular biology, called PCR (polymerase chain reaction). It is used for exponentially amplifying target DNA of pathogens. In a cell, DNA is present only in very low amounts, usually just as a single copy per cell. But using the material from only a few cells, specific regions of the DNA can be selected and copied millionfold with PCR in a process that takes usually 1-2 hours.

We recently established a special PCR variant, that amplifies DNA in a form that can be directly analysed on our microarrays and developed automated programs for the technical platform for the applications. The next step underway is the design and testing of microarrays that can be used for the detection of DNA from pathogens, like Bacillus anthracis or ortho pox viruses.

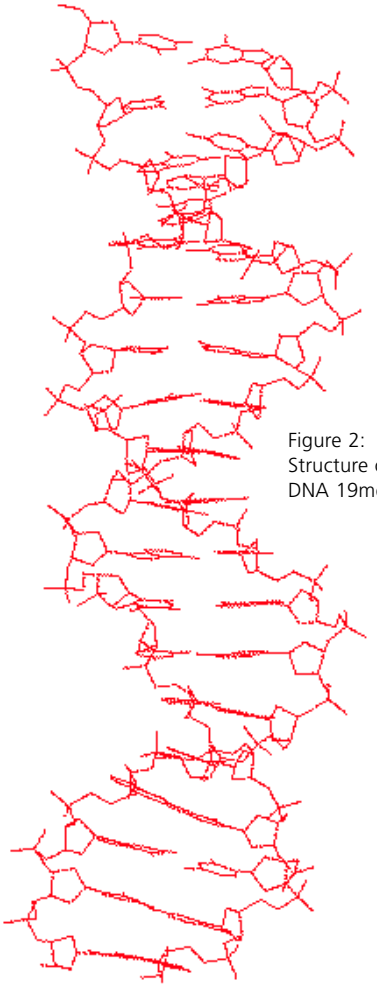
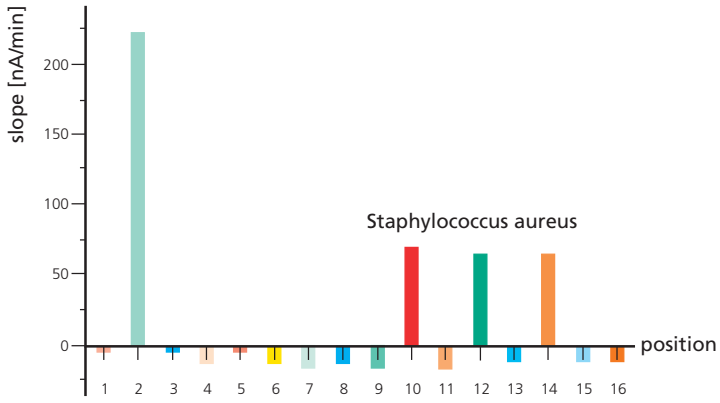


Figure 2:
Structure of a DNA 19mer.



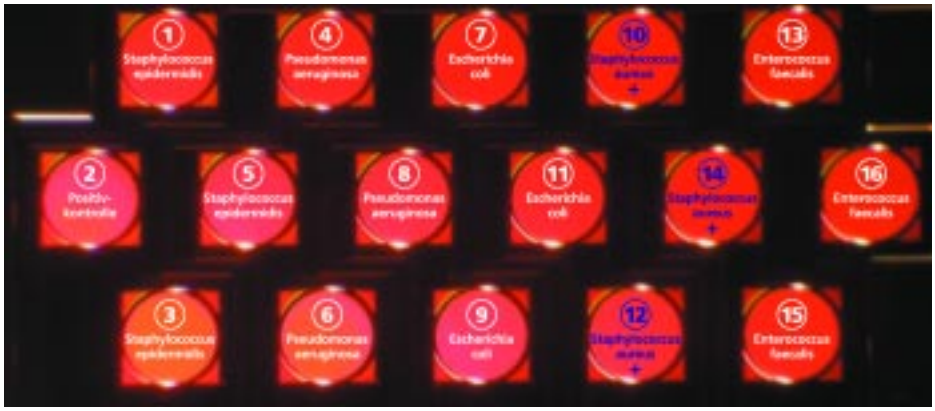


Figure 3:
Microarray for detection of 5 bacteria species, scheme of capture sequences and an example for the positive detection of RNA from Staphylococcus aureus (slope value analysis).

Representative Results of Work Module Integration

High Vacuum Wafer Bonding Technology AuSi Eutectic Wafer Bonding with Integrated Getter Thin Film for Long Term Stable High Vacuum

MEMS operation requirements

Microsensor packaging is one of the most important and challenging, technology areas. In particular, hermetic packaging on wafer level is a key technology of many microelectro-mechanical systems (MEMS). The hermetic sealing protects them from harmful environmental influences, significantly increasing their reliability and lifetime. In addition some MEMS need a specific gas or pressure environment within the package to function as specified, see table 1. This article intends to give an overview on the relevant technological topics to produce hermetic sealed, micromachined devices on wafer level with controlled cavity pressures ranging from 10^{-4} mbar to 1000 mbar.

Wafer-level processes are particularly interesting for the MEMS packaging since they can reduce the fabrication costs and open up possibilities for batch processing. Various wafer level sealing technologies may be used, including wafer bonding, cavity sealing by thin-film deposition, and reactive sealing.

Fraunhofer ISIT develops together with the project partners Saes Getters, ST Microelectronics, Thales Avionics, EV Group, and University Pavia within the european project VABOND a process on eutectic AuSi wafer bonding to produce low-cost and long-term reliable hermetic MEMS packages. Figure 1 shows the main functional elements of a surface micromachined MEMS device with integrated getter film in the cap.

Beside maintaining vacuum, encapsulation on wafer level solves the problem of device protection during the wafer dicing operation. The improved robustness of capped devices allows MEMS devices to be handled in existing standard semiconductor backend processes.

sensor/device type	vacuum level
accelerometer, switch	300 – 700 mbar
absolute pressure sensor	1 – 10 mbar
resonator	10^{-1} – 10^{-4} mbar
bolometer	< 10^{-4} mbar

Table 1: Required vacuum level for different MEMS.

AuSi eutectic bonding

AuSi eutectic bonding is a technology using eutectic formation at 363° C between a silicon wafer and gold deposited on another silicon substrate. The bond temperature used is in the range of 380 – 400° C. This is compatible with Al device metallisations. Due to the liquid melt formed, this technology tolerates wafer topography coming from previous processing operations. The technology is also compatible with extended outgassing cycles and the activation requirements in case a deposited getter layer is present in the device cavity. Compared to glass frit bonding, AuSi eutectic bonding does not outgas during the wafer bonding cycle, and requires only very small bondframe widths, typically in the range of 60 – 100 µm. This increases the throughput which is a major parameter for low-cost production.

Getter technology

The use of Non Evaporable Getter (NEG) material (Zr based alloy) is required to ensure suitable vacuum (total pressure under 1 x 10^{-3} mbar) and long-term stability in MEMS devices. NEG can chemically sorb all active gases, including H_2O, CO, CO_2, O_2, N_2 and H_2. The main constraints imposed by the device design and process are the compatibility of the getter with the fabrication process, the thickness of the getter film and an activation temperature compatible with the bonding process. Besides this, SAES Getters laboratories offers a patterned deposition of the getter material on the cap wafer by a proprietary technology: PaGeWafer®,.

The thick getter film can be selectively placed into the cavities without affecting the lateral regions of the wafer where the hermetic sealing is to be performed. The typical pattern lateral dimensions are in the range of the millimeter, while the getter film can be placed in the cavities

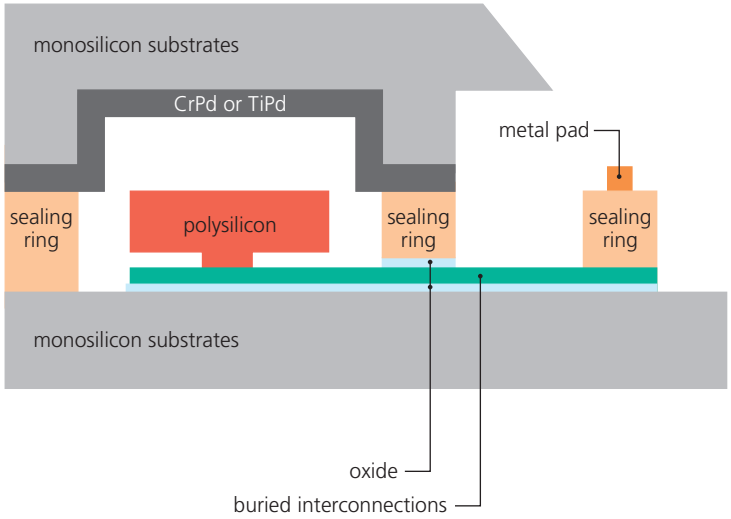


Figure 1:
MEMS construction with getter.

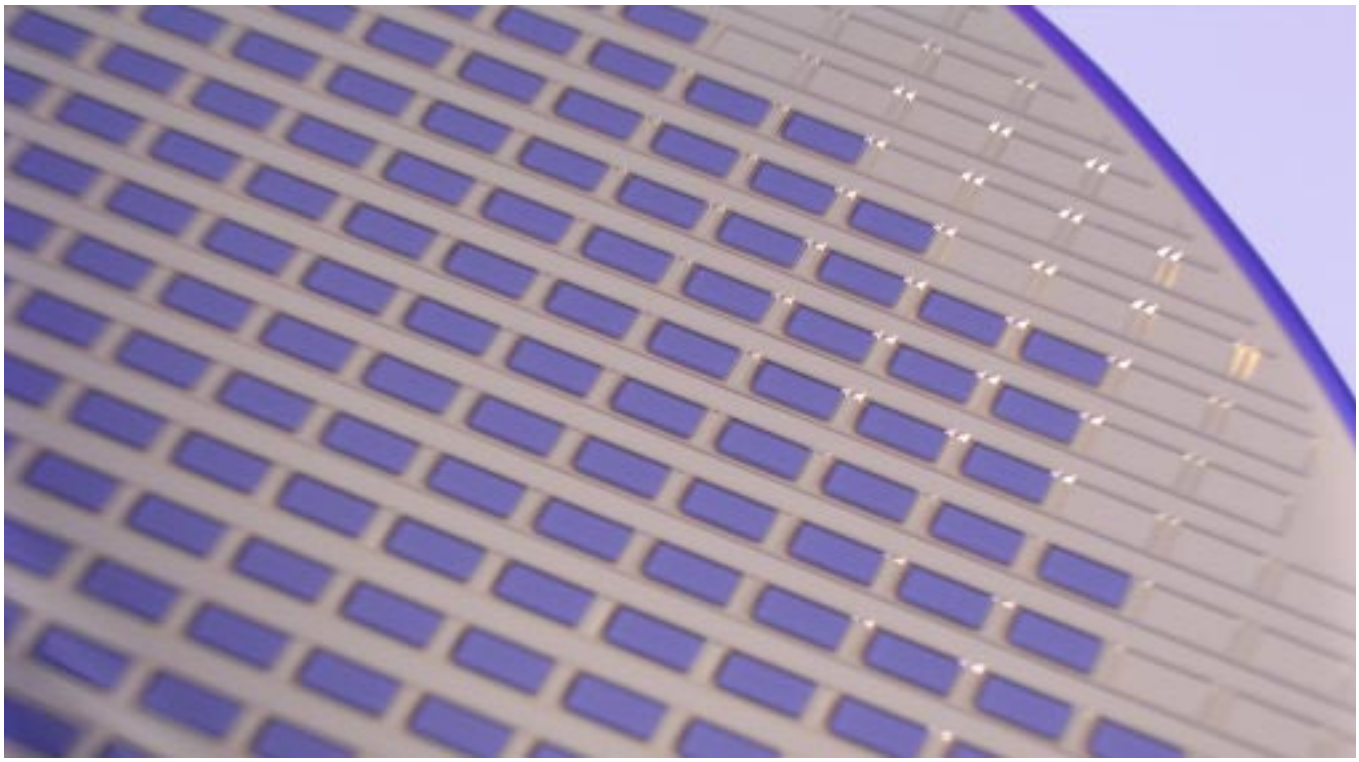
with any depths, ranging from few microns up to hundreds of microns. Figure 2 shows the precise deposition of the getter material inside the cavities.

The getter film consists of a special Zr alloy whose composition is optimized to maximize sorption performance or to maximize performance in specific sealing or bonding processes.

Cap wafer cleaning

Wafer cleaning of the cap wafer is usually required before bonding to remove organics from the gold bond frames. The getter layer must tolerate the cleaning chemistries. It has been discovered that a caustic chemical treatment of the getter film both cleans the film and enhances its performance without measurable degradation of its structural integrity. For example, caustic chemical treatment SC1 with $NH_4OH/H_2O_2/H_2O$ and SC2 with $HCl/H_2O_2/H_2O$ did not affect the morphology and the sorption capacities of the getter film and significantly increased the sorption capacity, measured after ASTM standard F 798-82.
The getter film at wafer level can withstand

Figure 2:
Cap wafer with deposited getter layers.



Representative Results of Work Module Integration

also treatment with a highly aggressive HNO_3 process up to 65 % @120 °C. The full compatibility of the getter film towards both temperature and chemical treatment with regards to the activation and capacity of the getter film is demonstrated. Typical absorption speed and absorption capacity of the patterned getter film per unit area at room temperature for hydrogen and carbon monoxide are reported in figure 3.

Getter activation

The getter film is supplied in a stable, passivated form to protect the getter and to ensure that it performs as specified. The PaGeWafer, can be safely handled in clean room air. Once the getter film is in a vacuum or noble gas environment, it needs to be activated. Activation is achieved by applying thermal energy to the getter to diffuse the passivation layer into the bulk, rendering the surface of the grains chemically active and ready to pump contaminants out of the MEMS package.

The getter film activation can be achieved through three main scenarios:

1. the classic scenario is activation of the getter as part of the wafer bonding process. The temperatures under vacuum reached in the bonding process will simultaneous activate the getter as well as bond the device and cap wafers. In this case, the getter film will also improve the process conditions, by achieving a higher vacuum between the two wafers in the cavity.
2. The second scenario is to apply heat to the cap wafer after bonding
3. The third scenario is first to heat the cap wafer under vacuum and then align the wafers and bond them.

Backfilling

To realize a defined gas damping for resonating sensors, a gas-filling procedure has to be established. Only inert gases or gases that do not consume the getter or alter the getter sorption performance may be backfilled in the device cavities. Most often Argon is selected because of good damping characteristics and low out diffusion. The backfill operation is typically one step in the wafer bond cycle. Figure 4 shows the dependency of the device Q-factor from cavity pressure for a typical BOSCH type yaw rate sensor.
The cavity pressure can be tuned to any value between 10^{-4} mbar and 1000 mbar, even overpressure is possible depending on the wafer bonder infrastructure.

Hermeticity testing

The pressure inside of the vacuum encapsulated devices depends on the outgassing of the inner surfaces, the leakage rate through fine leaks and permeation through the walls, see figure 5. The outgassing depends mainly on the fabrication process of cap and device wafer, which has to be optimized.
Fine leaks arise from imperfect bonding or crack initiation. The pressure change per unit time in a device can be expressed as
$dP/dt \approx L / V$
where L is the leak rate and V the cavity volume of the device. Typical cavity volumes range from 0.1 mm^3 to around 5 mm^3.

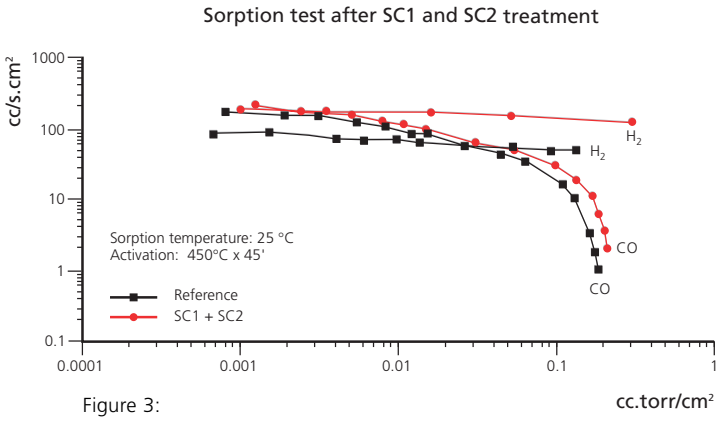


Figure 3:
Sorption characteristics for H_2 and CO per cm^2 of getter film after a SC-1 and SC-2 treatments.

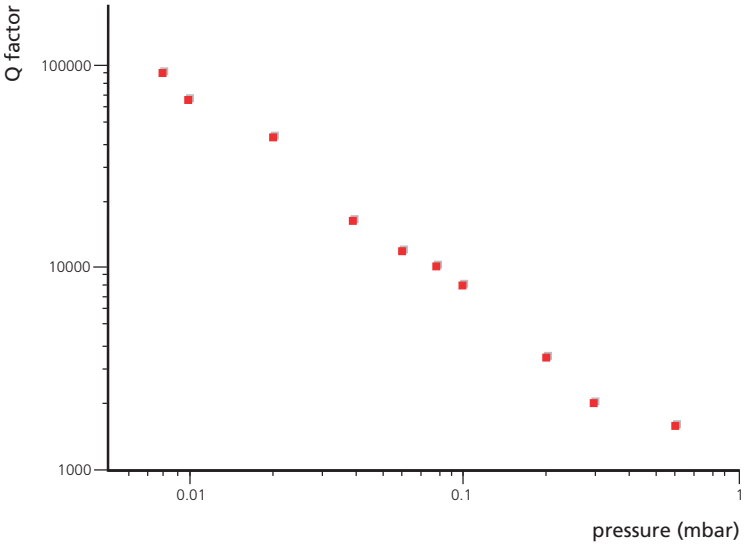


Figure 4:
Dependency of the Q-factor vrs. cavity pressure [N_2] for a typical surface micromachined resonator.

Since fine leaks may always be present a leak test is necessary to guarantee a leakage rate which is small enough to be compensated by the getter. This leak rate may be called the critical leak rate, as it defines the devices within the statistical cavity pressure distribution that fail the first after the guarantied lifetime is fulfilled. As an example: for a device with a life time demand of 15 years and internal vacuum requirement better than 0,1 mbar and a getter capacity of approximately 1.7 x 10^{-5} mbar·l per cavity the maximum tolerable leakage rate for a cavity volume of 0.26 mm^3 is 3.6 x 10^{-14} mbar·l/s. Due to the high Helium permeation in Si and silica a long-term stable, high vacuum better than 10^{-4} mbar is very difficult to achieve. Fraunhofer ISIT has developed a in-line, ultra-fine leak test on wafer level to determine the leak rate of every single resonating device before shipping out. This ultra-fine leak test overcomes the limitations of He and Kr^{85} fine leak test and is compatible with integrated getter and unaffected by the typically very small cavity volumes. Critical leak rates down to 10^{-16} mbar·l/s can be determined without interference between neighboring devices.

Conclusions

In respect to process yield, a eutectic wafer bonding technology with a liquid phase of > 1 µm thickness will considerably improve the tolerance of the bonding process in respect to surface topography and bondframe imperfections (scratches, particles). A cap wafer cleaning procedure with SC1 and SC2 has found to be very effective to achieve a good bond homogeneity, and at the same time even improves the getter sorption capacity. It is not recommended to apply Ar ion milling or backsputtering on any of the used wafers. PaGeWafer, can assure high performance MEMS sensors, considerably increasing the device life time by maintaining the Q-factor of the device, at the same time relaxing the stringent requirements for minimum leak rates.

Acknowledgements

ISIT greatfully acknowledge the project funding by the European Commission (IST-2001-34224).

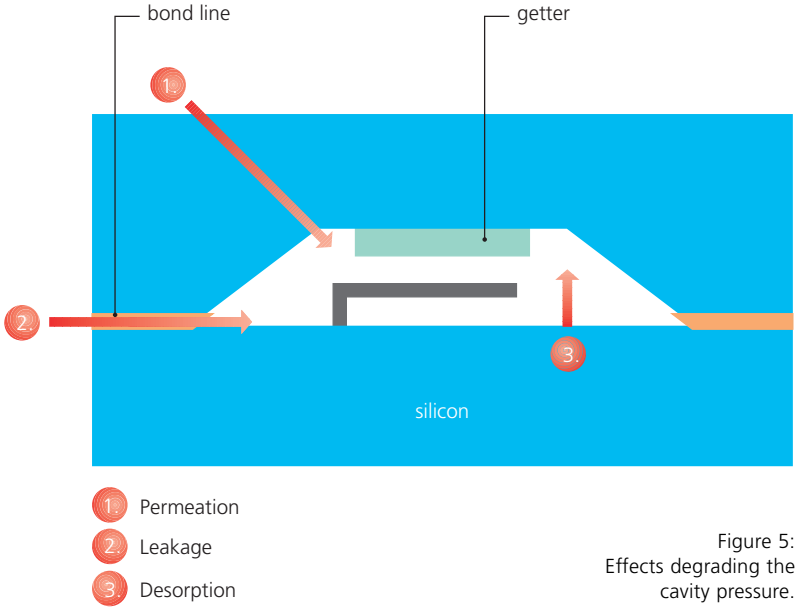


Figure 5:
Effects degrading the cavity pressure.

Representative Results of Work Module Integration

Studies on Underfilling Components With Area Array Solder Terminals in Surface Mount Technology

Introduction

Chip-Scale-Packages (CSP) have area array terminals placed on the components bottom side made of small balls of solder. Up to now, the use of underfill (UF) for them is not established in conventional manufacturing routes. As a result of a thermomechanical mismatch between the CSP-component (Si-chip) and the PCB, thermal cycling will initiate fatigue cracks in the solder balls. The result is that CSP-components are often the reliability-limiting components in electronic assemblies.
For Ball-Grid-Arrays (BGA), component underfilling is conceivable if the application requires high reliability at simultaneously high stress. It makes sense to underfill large-area, non thermally matched systems. Underfilling is even being proposed for the larger SMD-types, the BGA, when the relevant components are exposed to harsh environmental conditions, e.g. electronics for automotive applications.
The potential of underfilled CSP and BGA components to increase product reliability has up to now not been fully utilised. One reason for this has been the lack of fundamental studies on the requirements of the special underfill materials and on process reliability.

Figure 1:
Layout of the test PCB.

Objective

The main objective of the project was to qualify underfill materials which are suitable for underfilling CSP and BGA components and which can withstand 2000 temperature cycles (–40° C°/ +125° C) with a dwell time of 30 minutes on each temperature level.
The underfilling of CSP and BGA components with area array lead free and lead containing solder terminals in surface mount technology has been systematically studied and evaluated. One of the goals of the research was to define the particular requirements that have to be put on CSP/BGA underfill materials and to estimate what level of process reliability for underfilling can be achieved. The knowledge and experience with flip chip underfilling could not be directly transferred to CSP and BGA assemblies due to the differences in material combinations and geometry of the joint gap as well as the differences in the nature and magnitude of the stress. Ageing and stress tests on test assemblies with commercially available and alternative underfill materials highlighted the specific advantages of underfilling CSPs and BGAs.

The studies had been realized in cooperation with the „Fraunhofer-Institut fuer Fertigungstechnik und Angewandte Materialforschung“ (IFAM), the „Institut fuer Aufbau- und Verbindungstechnik der Elektronik“, Technische Universitaet Dresden and the Fraunhofer-Institut fuer Siliziumtechnologie (ISIT). The authors would like to acknowledge the financial support for this work by the German Federal Ministry of Economics and Labour (AiF-project 13.138B).

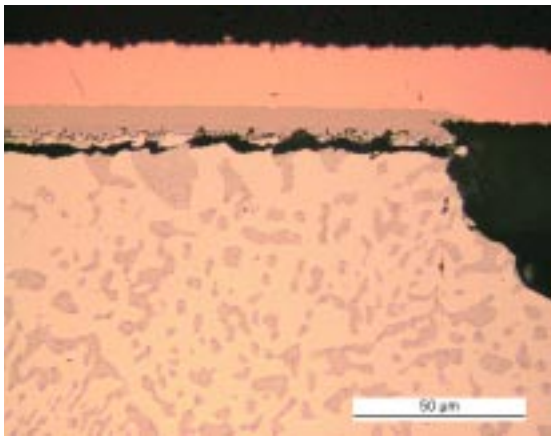


Figure 2:
FFBGA1152/WUF
after 1250 cycles TS
-40/+125° C.

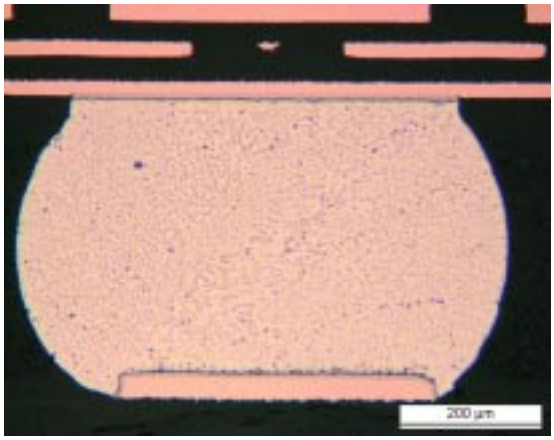


Figure 3:
FFBGA1152/UF
after 2000 cycles TS
-40/+125° C.

Results

Simulations to specify underfill material properties

First of all a simulation was carried out. The objective of this simulation was to characterise an ideal underfill material and to derive thermomechanical requirements as an aid to preselecting suitable alternative polymers for underfilling. The finite element method was used for the calculations. Prediction of the lifetime was carried out using the relationship of Coffin-Manson.
The simulation results showed that stiff underfills increase the lifetime and equalise the stress on the solder joints. On the other hand, there is an increased risk of cracks forming in the Si-chip and other defects (e.g. delamination). It is hence recommended to select an underfill with a modulus of elasticity E not larger than necessary to guarantee the required lifetime of the solder joints.
The effect of the coefficient of thermal expansion of the underfill is considerably greater for stiff underfills than it is for soft underfills. The optimum value depends on the stiffness of the underfill. In order to avoid additional tensile and compressive stress on the solder joints between the chip and PCB, it is recommended to have a soft material such that the coefficients of thermal expansion α of the underfill and solder are approximately the same: $\alpha_{UF} \approx \alpha_{sol}$.
For a very stiff underfill it is recommended that the coefficients of thermal expansion CTE and the modulus of elasticity E of the underfill and PCB are approximately the same: $\alpha_{UF} \approx \alpha_{PCB}$ and simultaneously $E_{UF} \approx E_{PCB}$.
In this situation the underfill and PCB form a homogenous clamp around the solder terminal which reduces the undesired stresses in the solder joint and thus increases its lifetime.

Screening for suitable materials

A search was carried out to screen alternative materials that were commercially available. Four alternative materials matching the requirements from the simulation were chosen. These materials, along with the other underfills, were subjected to a screening procedure in order to make a preselection. The objective of this screening was to qualify a limited number of the numerous underfills and alternative materials for underfilling original components.
After all results came in, an evaluation matrix was drawn up in order to define 8 materials for further testing on the test assemblies. The four criteria "CTE value", "reworkable", "flow behaviour at 70° C" and "alternative material" were identified as key differentiating and selection criteria for this project. A low CTE value is important for the automotive sector (temperature shock test load). For the consumer product sector, a high CTE value (mechanical shock load) and a reworkable underfill are advantageous.
The underfill materials that were used to build the assemblies had key properties in the following ranges:

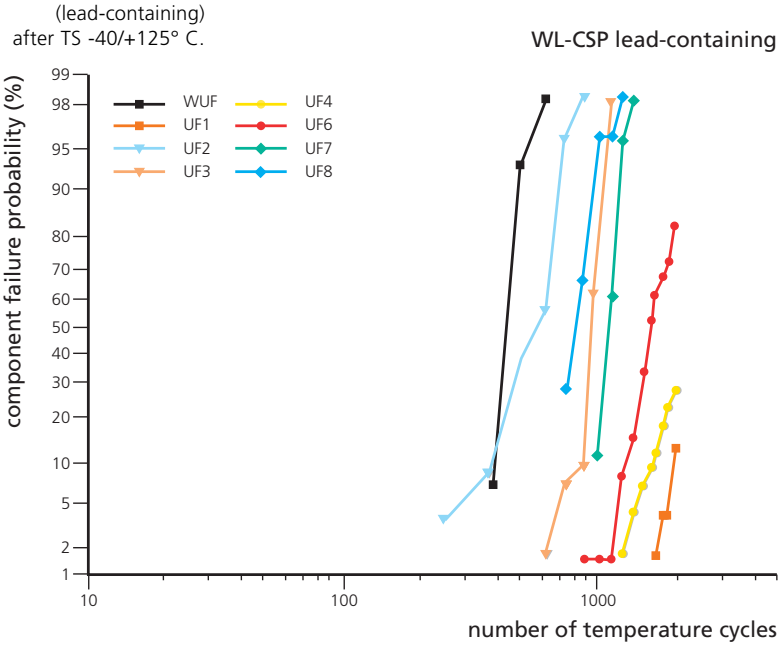
- CTE value: 27 ppm/K below T_g up to 229 ppm/K above T_g
- Glass transition temperature: 9° C to 144° C
- Reworkable underfill materials: two underfills.

Representative Results of Work Module Integration

Test assembly manufacturing and testing procedure

µSMD, CSP and BGA assemblies were selected in order to have maximum variation of the components. The respective components can however be viewed here as each being representative of a type of component. The assemblies were soldered with lead-free solder and also lead-containing solder (figure 1). They were underfilled and the initial state was characterised. After exposure to temperature shock cycles (TS, -40° C / +125° C, with 30 minutes dwell time on both levels) all the components were electrically tested at room temperature after 30, 60, and 125 hours and then every succeeding 125 hours. Metallographic cross sections have been prepared and analysed for selected samples.

Figure 4:
Fatigue life: WL-CSP (lead-containing) after TS -40/+125° C.



Reliability investigation by temperature shock test cycling

The properties of the underfill materials have a significant influence on the very complex load conditions of the solder contacts. Materials with a high stiffness lead to a significant increase of lifetime due to a more uniform stress acting on the contacts. On the other hand there is an increased risk of cracks in the silicon chip and other defects (e.g. delaminations etc.). Therefore, the E-modulus of the underfill materials should be chosen not higher than it is really needed for the guarantee of the required lifetime of the solder contacts. The influence of the coefficient of thermal expansion (CTE) is much more significant when underfill materials with high stiffness are in use compared to applications with lower stiffness materials.
One underfill was shown to be the most suitable for most of the components that were studied. The defined target to withstand 2000 temperature shock test cycles (TS) was essentially fulfilled (figure 3). The reference samples of the same component type without underfill (WUF) failed after just 1250 cycles (figure 2). A lower CTE in combination with a high Tg makes them very suitable for the application under study.
For the underfilled assemblies there was a clear difference between the reliability of WL-CSP soldered with lead-containing and lead-free solder (figure 4 and figure 5). Temperature shock lifetime of the lead-free soldered components was much shorter. This may be due to differences in the composition of the solder paste and to the differing residues (contaminated PCB surfaces) as well as to the observed failure mechanisms. The electrical tests on lead free WL-CSP components without underfill and with several underfills showed that there were very early failures (< 100 cycles). In addition to the already known causes of failure such as crack formation in the solder and detachment of the underfill from the component and PCB a new cause of failure was observed. Some materials cause damage to the overall system on the PCB. Tensile stresses occur in the solder at high temperatures which are larger than when lead-containing solder is used. Lead-free solders are

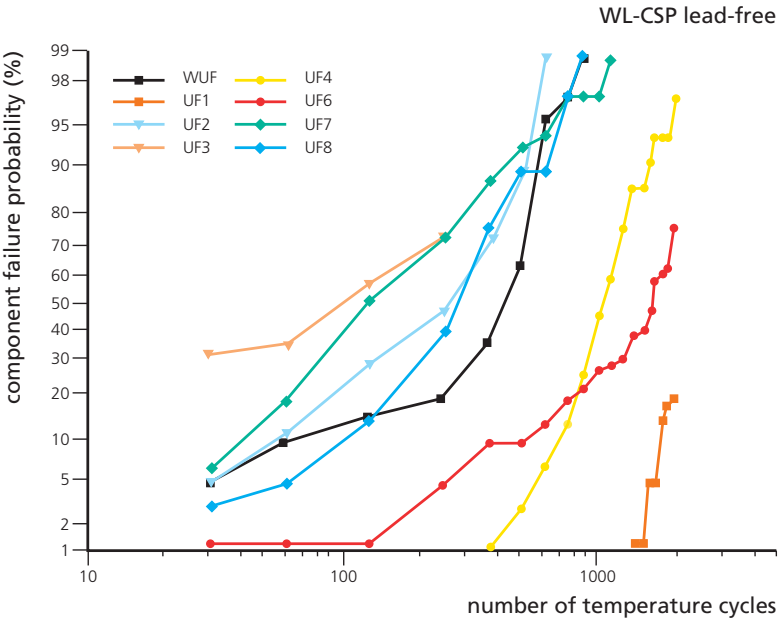
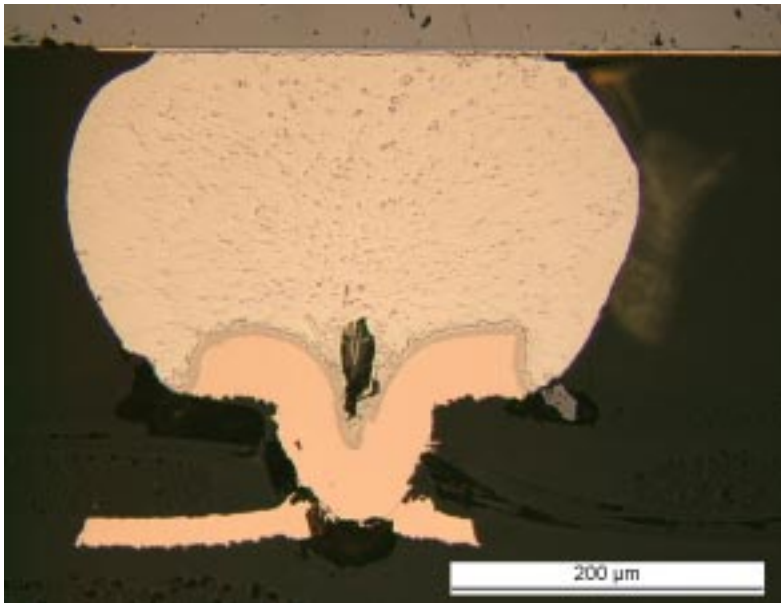


Figure 5:
Fatigue life: WL-CSP (lead-free) after TS -40/+125° C.

more creep resistant and hence less compliant. The tensile stress within the solder joint deforms the copper traces in Z-direction, obviously caused by the high CTE of the underfill. Cracks form at the periphery to the microvia due to high deformation of the pad in the Z-direction, additionally, delamination is observed beneath the pads due to Z-axis expansion and detachment of the underfill from the solder resist (figure 6). The solder joints' strength to the copper pad via the intermetallic phases is larger than the adhesion of copper to the FR4; therefore, the copper pad is necessarily deformed during temperature shock load while delaminating from the FR4.
Due to the cyclic tension and compression of the solder joint, the periphery of the microvia is stressed by cyclic bending; thus, fatigue fracture is caused after a short time.
As a measure of the underfill performance, a ranking of the underfill materials has been set up with respect to the component type.
The underfill that was chosen from the favourably-priced alternative materials is in the lower middle of the ranking. This material may be taken as an economic alternative, provided the requirements on reliability are of less importance.
However, not every underfill is equally suitable for all types of components. An underfill for one component type may be in the top group, for another at the end of the ranking.
The repairable underfill materials are at the bottom of the ranking. The ability to be repaired and increased reliability after temperature shock test cycles cannot be combined in the materials under test.
It must however be emphasised that the main concern of this project was the reliability in temperature shock test cycles. This is a key requirement for automotive applications. For "hand-held" applications with the main requirement to withstand mechanical shock, the ranking of the underfill materials may be totally different.

Selected underfills were applied to industrial electronic control assemblies. These systems were subjected to temperature shock test cycles as part of the internal qualification programme by the industrial partners. Intermediate results after 1000 cycles showed similar results to the test assemblies used in this project. Underfill materials that proved suitable on the test assemblies also showed no failures on the industrial demonstration systems. Underfill materials that showed unsatisfactory reliability on the test assemblies showed the same failure behaviour (such as cracks in the laminate and in the soldered joints). Therefore, transfer of the results to industrial applications is possible and application in series production can be expected soon.

Figure 6:
Fatigue life: WL-CSP/UF (lead-free), microvia removed after 1000 cycles TS -40/+125° C.



Representative Results of Work Module Integration

Lead-Free Soldering for RoHS Compliance – Challenge, Task and Chance

Imposition of change in electronics production

When people think of their most popular electronics goods used on day to day basis, they may not understand the environmental impacts and externalities of these products' life cycle. For example, computers and their components – semiconductor chips, circuit boards, and disk drives – are made from more than 1,000 materials. Many of these materials – such as solvents, gases, acids, brominated flame retardants, plastics, lead, cadmium, and mercury – are extremely toxic. Similar hazardous materials and substances are used in production of popular mass market products such as telephone, radio, TV, fax machines, video players, CD players, mobile phones etc.

Decades of irresponsible use of hazardous chemicals and substances used in manufacturing of electronics goods resulted in highly contaminated groundwater and community health problems in a number of countries, including EU member states. Further, electronics production, seen over the entire life cycle of the products, contributes to a number of environmental problems, including ozone depletion, global warming, acidification, human toxicity, fauna and flora toxicity, resource depletion (materials and energy carriers), and smog.

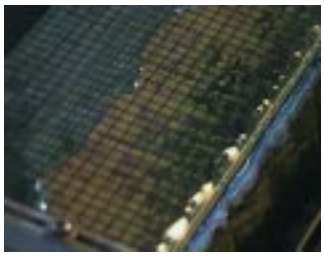
On the example of computers, it is estimated that more than 60 million new PCs enter the market and 12 million are disposed of each year in the European Union. Add the unknown numbers of old computer products hidden in basements or garages, and the result is a staggering mass of plastic, metal, chemical, and glass "junk". The waste will contain more than 4 billion pounds of plastic, 1 billion pounds of lead, 1.9 million pounds of cadmium, 1.2 million pounds of chromium, and nearly 400,000 pounds of mercury. Amazingly, less than 10 % of outdated computer products are refurbished or recycled. E-waste has become one of the world's fastest growing and most toxic waste streams. The industry depends on unimaginative solutions such as land filling and incineration as disposal methods. This leads to even more pollution and greater threats to human health.

Scientists and health professionals have long understood that lead causes serious health problems, including brain damage as well as blood and neurological disorders. Specifically neurological development of unborn babies and young children are at risk when exposed to lead in food chain. It is widely used in manufactured products, however, because of its strength and low melting temperature. Lead is imbedded into the glass of CRT monitors as a radiation shield,

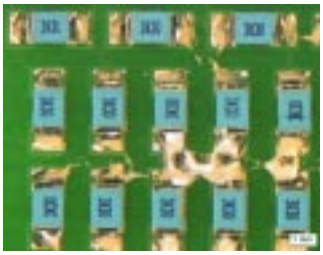
Figure 1:
Lead-free wave soldering; transport direction (from right to left).

a) chip wave in standby mode.

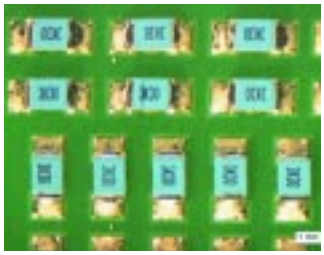
b) glass plate over chip wave showing flux activity.



c) on laminar second wave, no more flux avtivity.



d) wave soldering R0805, air: solder bridging (left).



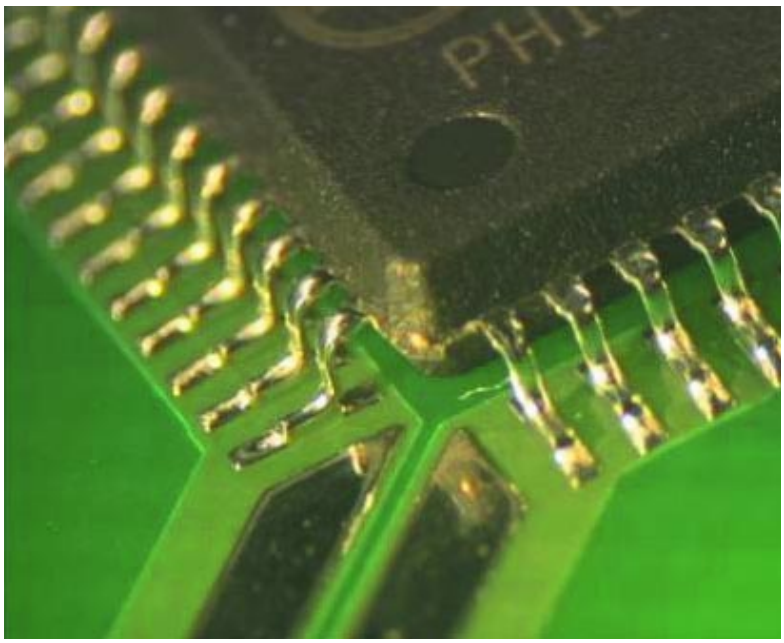
e) wave soldering R0805, nitrogen inert gas: no bridging, few solder balls (right).

used as solder on circuit boards, and incorporated into computer parts.

Thus, it is high time that the EU acts. The policy formations of the Integrated Product Policy based on life cycle analysis, such as the WEEE and RoHS directives, are a step in the right direction to address the environmental issues in electronics products lifecycle from cradle to grave. By cradle to grave is meant the life cycle spanning from raw material extraction all the way to end of life recycling, recovery, disposal. Since February 13, 2003, when two european guidelines were set into action, a new era started for electronics production: The new EU legislation on electronic waste stream and restriction of hazardous substances presents consequences for all parties involved in the electronics products supply chain: OEM manufacturer, contract assembly houses, equipment manufacturer, solder and flux manufacturer, PCB manufacturer, component manufacturer and distributor, and other consumables (gas/nitrogen, tooling) manufacturer, and, last not least, recycling companies and communal waste management.

However, the environmental problems will be solved the quickest and in the most expedient manner if the industry is not only imposed a set of more stringent norms but is actively supported in the transition process. The problems arising of the enforced laws are especially harsh for SME assembly houses:

- Substantial cost factor due to necessary investments in new equipment
- Incomplete availability of RoHS and process compliant components
- Lack of compatibility of lead-free processing at higher temperature with existing device specifications
- Lack of experience with lead-free-specific inspection and repair routines
- strong deficits of personnel skills regarding lead-free soldering
- disruption of running commercial production during experimental introduction, feasibilty tests and in-house training lead-free technologies not only in RoHS relevant, but also RoHS exempted applications.



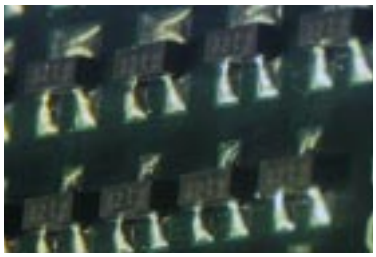


Figure 2:
wave solder applications under inert gas.
a) SnAg3.5.
b) SnCu0.8Ni.1.

Joint research for lead-free soldering with ISIT

Together with a group of companies from the Hamburger Lötzirkel, experiments were performed on industrial line wave solder systems at the sites of equipment manufacturers. It was found that under air the solder on the second wave oxidized so quickly, that passive SMDs (Surface Mounted Devices) on the solder side formed frequent bridges between adjacent solder joints (figure 1d), although the pad layout was in accord with current recommendations. The reason was that the flux layer was consumed completely on the first wave (figures 1b to 1d). Under nitrogen, there was no bridging, because there was no oxidation on the second wave (figure 1e).

More wave solder experiments under inert gas conditions were performed with different alloys, also in comparison with tin-lead. Systematic tests with over 200 boards showed that for SMD, no new defects appeared for lead-free when the design recommendations as known for tin-lead wave soldering were used. Indeed, design aids like solder thieves in the wake of the solder wave

prevent bridging for lead-free alloys just as well as for tin-lead, as shown on a QFP44 with 0.8 mm pitch (figure 2a). Even design tolerances could be shown: Where pad design intended for reflow soldering was placed on the wave solder side next to the dedicated wave solder design, there were no missed pads found (figure 2b): wave design/top row vs. reflow design/bottom row). This is not to be misunderstood as a recommendation for small pads and narrow spacing in lead-free wave soldering, however when process verification is done, there is some tolerance left with regard to the original recommendation, e. g. from Philips Guidelines for Pad Design.

However, design is crucial at THT (Through-Hole-Technology) with high thermal demand. This is shown in figures 3a and 3b. The contact time was rather short, only ca. 1.5 s. The massive copper rail conducts the solder heat away from the joint area, and the vertical fill is insufficient (figure 3a). A modified rail however, with saw cuts to increase thermal resistance, keeps the heat closer within the joining area. The result is thus an acceptable vertical fill (figure 3b).

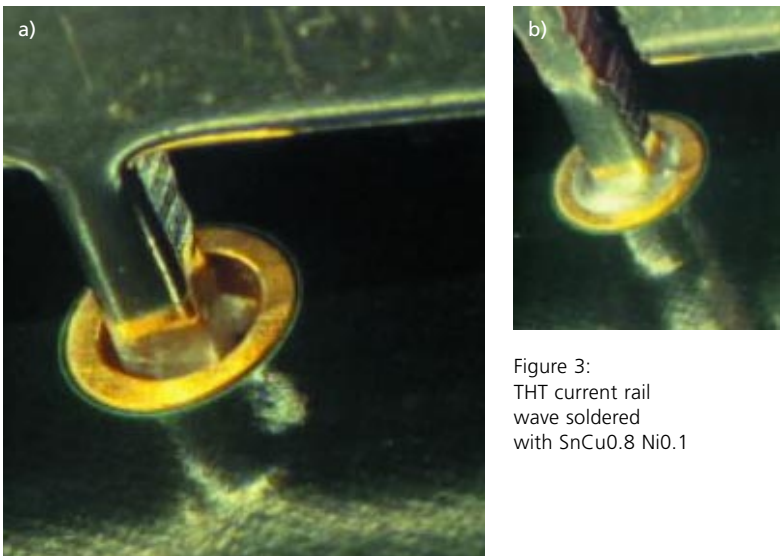


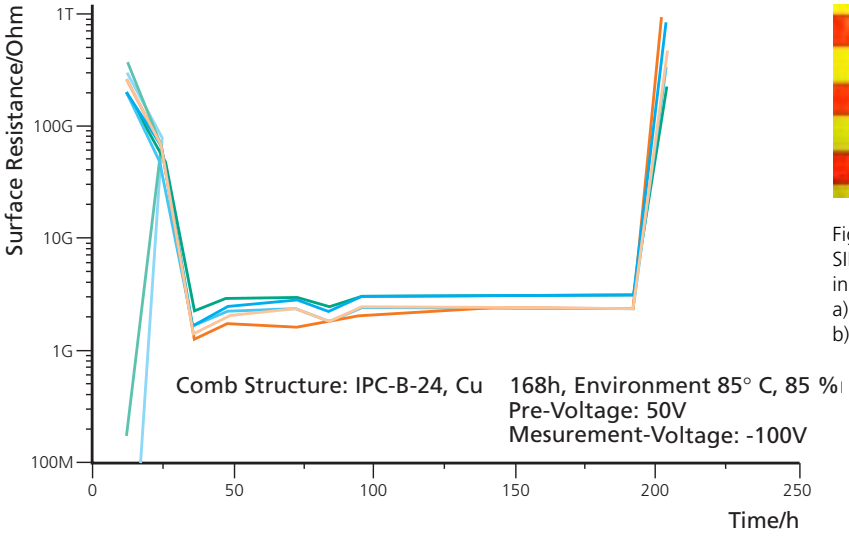
Figure 3:
THT current rail
wave soldered
with SnCu0.8 Ni0.1

As to reduce green house effect gases, alcohol based solvents are also to be reduced in accord with Council Directive 1999/13/EC of 11 March 1999 on the limitation of emissions of volatile organic compounds (VOC) due to the use of organic solvents in certain activities and installations. Although up to now this directive does not apply to electronic assembly, there is a tendency towards low-VOC or VOC-free soldering flux. For once, to make advantage of the higher activity when soldering with lead-free alloys at higher temperatures, secondly to reduce hazardous (flammable) chemicals in the production environment, and of course to reduce green house effect emissions altogether.

For selected flux formulations, ISIT has investigated long term corrosion effects from flux residues by means of a standardized SIR (Surface Insulation Resistance) test in accord with IPC-TM 650, using the IPC-B24 comb structure test coupon, humid heat at 85° C/85 %rH, 50 V dc continuous voltage and 100 V for the resistance measurement. Figure 4a shows the resistance vs. time diagram after 168 h, figure 4b the comb structure as inspected after the test, with no indication of dendrites or other harmful residues. During the one week test period, the resistance never dropped below 1 GΩ for all test coupons run over the spray fluxer, regardless if they were turned to point upwards with the fluxed structure, or if they were left with the structure downwards over the solder wave. This means that all tested formulations passed the requirements for no clean flux in accord with IPC-J-STD-001 and -004.

Assistance for electronics manufacturers

The process step of lead-free soldering in itself is already a manageable task, though to be mastered with narrow process tolerances. Assistance for this step in electronics production is given e. g. by equipment manufacturers for individual users. However, there is such great short term demand by industry for help and assistance in making the transition for conformity with the IPP (Integrated Product Policy) and specifically WEEE (Waste Electrical and Electronical



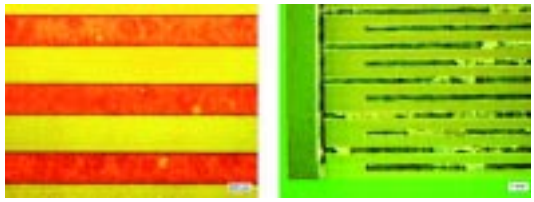


Figure 4:
SIR test result – copper comb after 168 h
in environmental chamber at 85° C/85 %rel.H.
a) Resistance vs. time diagram.
b) Inspection after test shows clean surface.

Equipment) and RoHS (Restriction of the Use of certain Hazardous Substances) legislations, that LEADFREE will not be able to satisfy the entire huge demand across Europe alone. A 2004 study from Technikum Wien says that over 40 % of electronics manufacturing companies in Austria and Germany are only starting their RoHS transformation activities in 2005 or even later. These companies are in grave danger for disrupted production and last minute failures which can threaten their existence. Fraunhofer ISIT has contributed to over 30 regional and international networking events to give information on technology and discuss transformation issues.

These events provided efficient feedback from design, production and logistics departments out of the rows of participants. They showed the need for external practice. Thus the ISIT Quality and Reliability group opted to broaden its spectrum of services and started activities to implement a full scale production line for training industrial personnell. This line will make use of the in-depth ISIT know-how in temperature measurement and solder process simulation, and of the experience gained with test board design and handling. The production environment will further incorporate the since long available ISIT rework center, so that e.g. component fitness for the increased thermal load in lead-free soldering can be tested from storage via double sided reflow to wave or selective soldering, all the way to multiple rework in one facility, and then tested for integrity.

Life Environment LEADFREE: Implementation of a "lead-free training line" in ISIT

The solution proposed is a non-for-profit, pre-competitive European competence centre for demonstration, training and exercises to be used by European electronics manufacturers, who bring their own materials and test vehicles to practice with state-of-the-art lead-free soldering equipment, assisted by scientific engineering supervision and analysis including hands-on training.

An innovation lies in the approach to mediate this environmental and product friendly approach also to single clients, thus presenting the possibility for SME to practice on their own discretion without the need to prior investment. The aim is to assist in evolution of sustaining technology in economically weak regions. In this way, the acceptance of environmental goals will be further increased, when it is demonstrated that environmental and economic goals do not exclude each other.

With the assistance of IZET, the aspect of reproduction and dissemination is covered by this partner experienced in marketing of technological infrastructure and possibilities on a european scale. Furthermore, IZET will focus on the project management which will be a difficult task with the view on the shear number of anticipated 300 SME clients taking part in the training and exercise actions. Thus, ISIT can focus on the aspects of skills and technology transfer.

For this goal, ISIT has applied for funding by the LIFE ENVIRONMENT programme to establish a fully functional industrial scale production line, which is to be set up in the well controlled environment based under the wafer fab facility. Complemented by the analytical and qualifying test methods provided by ISIT, this line will assist assembly producers as well as component manufacturers in qualification of materials and processes for environmental friendly products.

Representative Results of Work
Integrated Power Systems

Installation and Ramping-up of a Lithium-Polymer Rechargeable Battery Production Line

Re-chargeable batteries enter more and more fields of every-day life. Portable electronic devices, such as mobile telephones, notebooks, walkmen etc., rely on accumulators for their power supply. Other applications with a heavily growing market potential are smart tags or smart labels that are self-sufficient in power. New accumulator developments are also expected for all kinds of vehicles from automobile to electrically assisted bicycles and wearable electronics. Lead accumulators, nickel-cadmium (NiCd), nickel metal hydride (NiMH), re-chargeable alkali-manganese cells and lithium systems offer a wide spectrum as regards the range of performance, the quality and the prices.

It is the lithium ion accumulators in particular on which developments are focused since they provide the highest energy density of all available systems. However, this advantage is dearly "paid for". The liquid electrolytes used in the currently available lithium ion accumulators are sensitive to hydrolysis and require a high technological input. A rigid metal housing e.g. is therefore essential for this type of accumulator.

Not only does the hermetic metal encasement of the lithium ion accumulators, which can take up to 30 % of such an accumulator's weight, reduce the effective gravimetric energy density.

Apart from its disadvantageous weight, the rigid encasement also considerably reduces the freedom to adapt its shape to the small size of modern and optimized systems into which it would have to be fitted. Some potential applications ask for mechically flexible accumulators which cannot be realized by utilizing a rigid housing.

Great efforts have therefore been made at international level, to lessen the problem of the liquid electrolyte by housing it in a sponge-like matrix which acts as a carrier or by gelifying. Apart from increasing the safety level, the electro-chemically active layers as well as the housing can thus be made as foils. Work has been going on the relevant systems for several years now, but only now first product are brought into market.
The reason is that the problems arising when transferring the lab-scale production to industrial level has been underestimated.

The new development in lithium polymer technology carried out by *Sollith Batteries/Fraunhofer-ISiT* was driven by the above mentioned market demands:

- Reduction of weight
- Improved safety for the end user
- Increased flexibility in dimensions and capacity

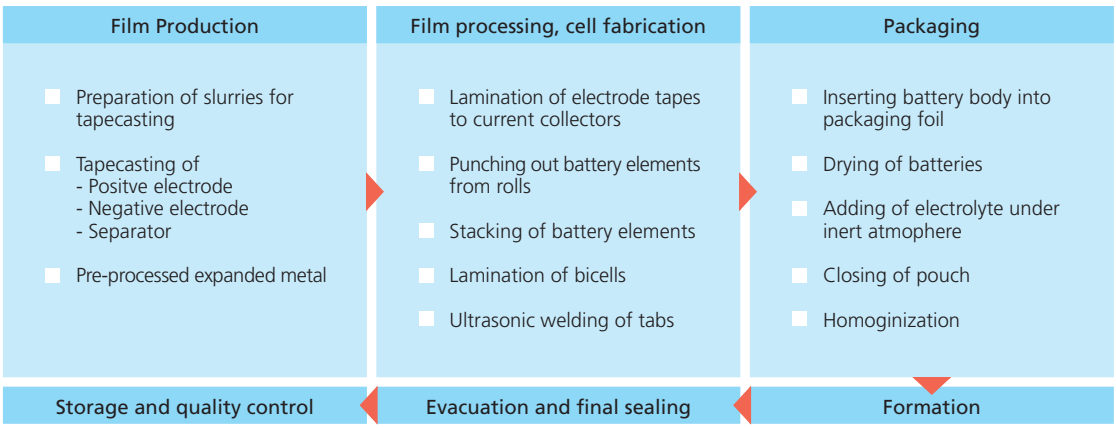


Figure 1:
Process flow of Sollith Batteries' Lithium polymer rechargeable batteries production line.

- Reduction of production costs even at moderate numbers of customer specific accumulators
- Opening of new fields of application by production of thin, large-area accumulators

Reduction of weight and improved safety are achieved by the specific set-up of *Sollith Batteries cells*. The abandonment of the rigid metal housing leads to an improved gravimetric energy density. Additional safety is coming from the immobilization of the liquid electrolyte in a polymer matrix and in particular from the set-up of the separator. It contains a solid state ionic conductor as ceramic filler that leads in combination with the immobilized electrolyte to a mechanically stable separator layer with high ionic conductivity. The mechanical stability of the separator is under safety aspects of great importance because it protects against internal short circuits in the battery due to e.g. dendrite growth from lithium metal deposition at the anode in case of overcharging. The use of a foil based housing additionally leads to improved safety because in case of overheating of the battery, leading to gas development, explosions are avoided. The polymer battery simply opens along the seal. In case of rigid metal housings an expensive relief valve or a burst protection has to be provided.

The improvements in flexibility in dimensions as well as in capacity is a problem associated with production set-up. This is accounted for by *Sollith Batteries* by a new production concept in which almost all components of the accumulator are stamped out in the required size from pre-processed foils. The thus obtained components are then joined together to so-called bicells by lamination. For given lateral dimensions the capacity of a cell can then be achieved by stacking of the neccessary numbers of bicells. The housing is realized in foil technology as it is known from packaging of pharmaceuticals or food.

Sollith Batteries GmbH (Itzehoe) and *Bullith Batteries AG* (Munich), its partner company, are

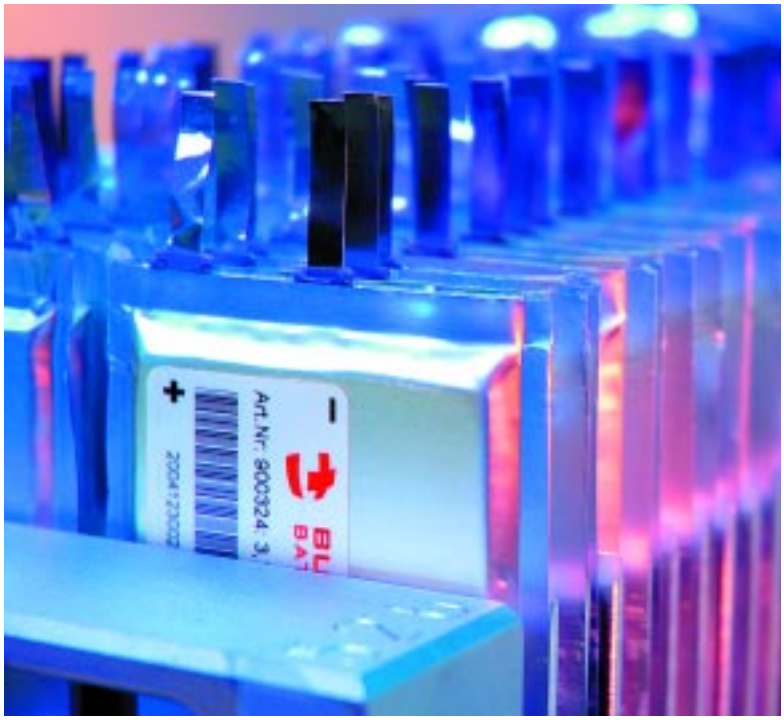


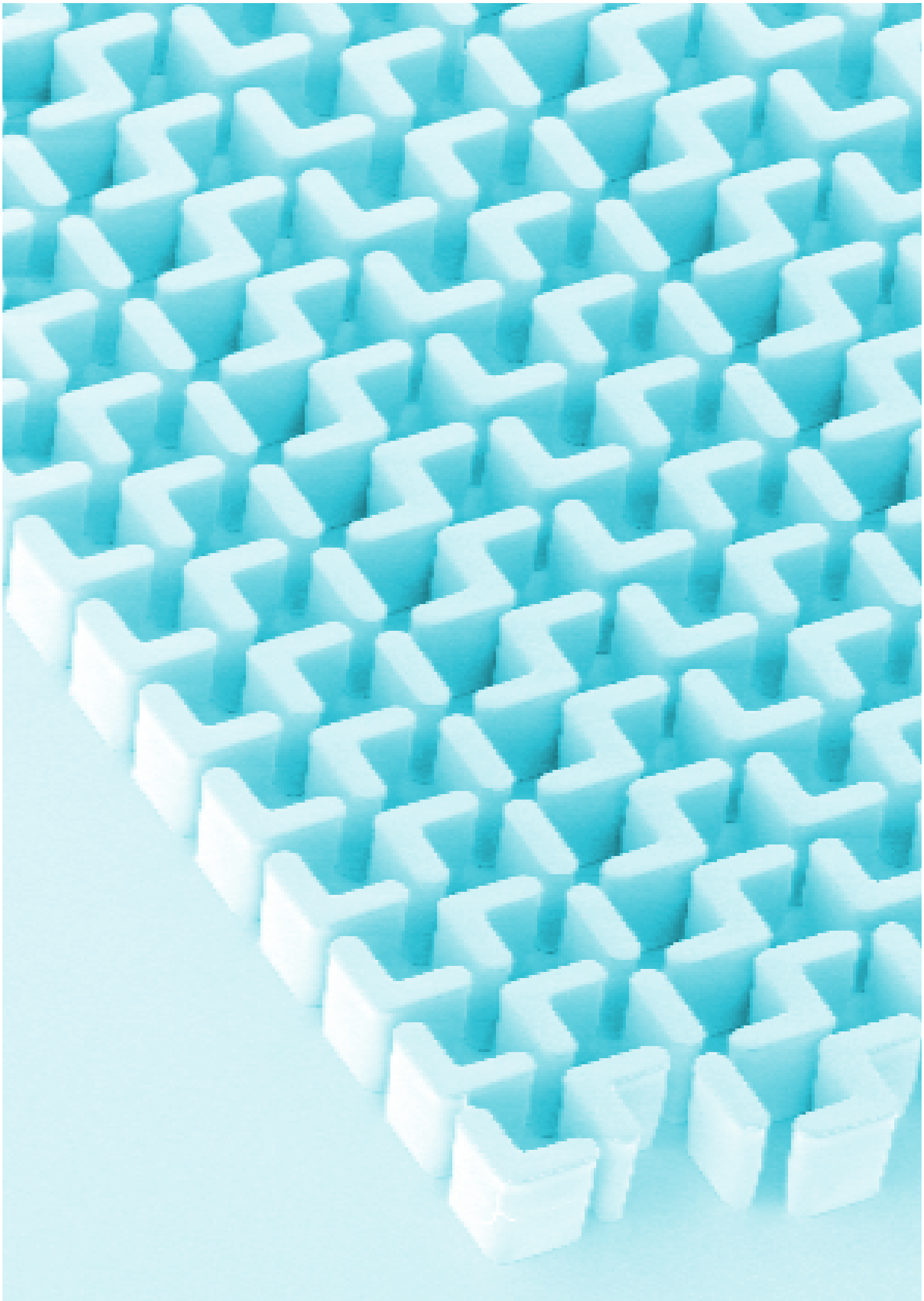
Figure 2:
Production of Sollith Batteries lithium polymer rechargeable batteries.

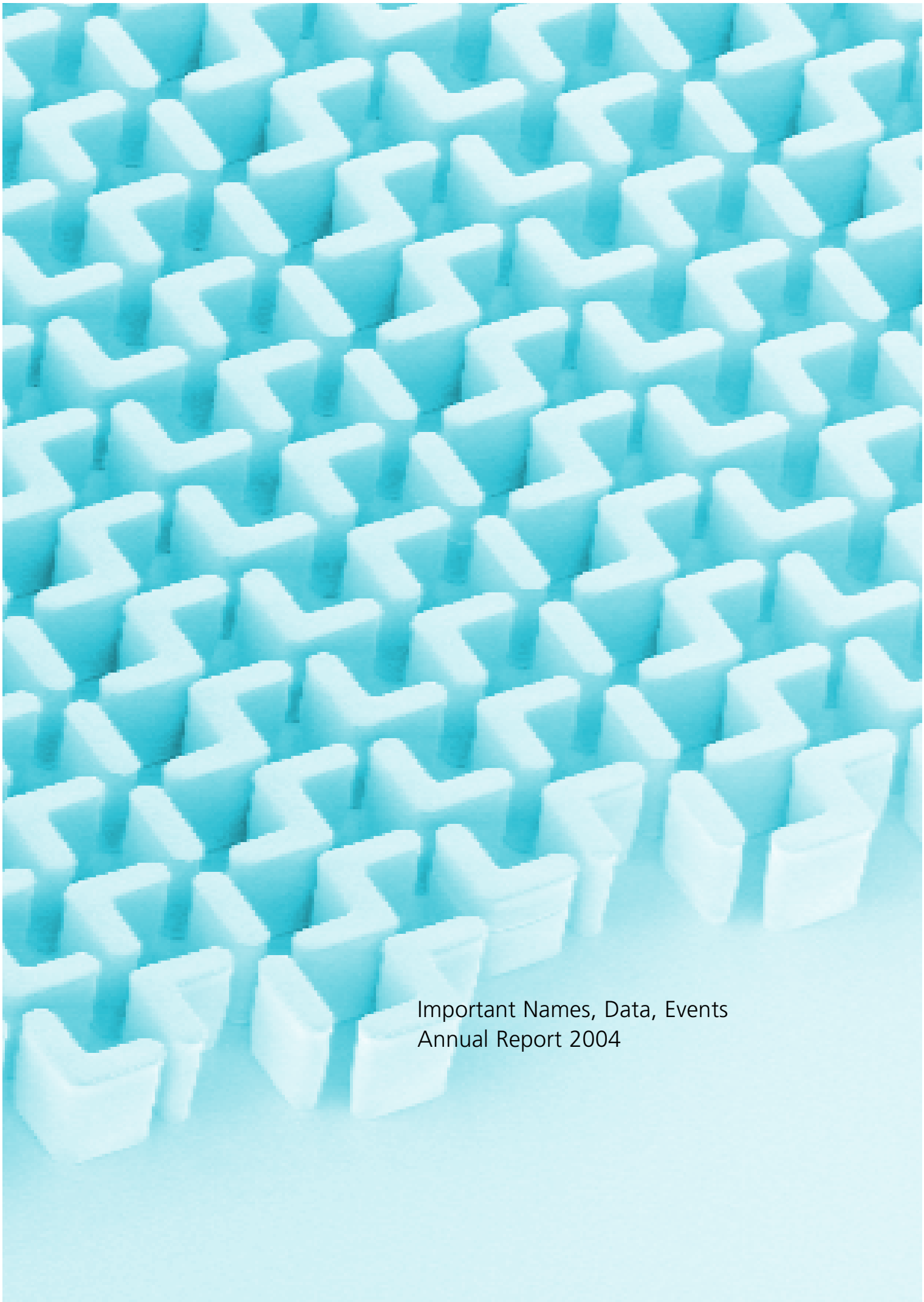
both spin-off companies out of ISiT with *Sollith Batteries* located in the direct neighbourhood of the Fraunhofer-ISiT. The ISiT is research partner and licenser for both companies. Within the year 2004 *Sollith Batteries* GmbH has carried out the final equipment installation and the ramping-up of a lithium-polymer rechargeable battery production line. For the first time a completely new production concept addressing to flexibility in customized design of rechargeable batteries has been realized.

This line allows for the production of prismatic cells in the range of:

(mm)	Minimum	Maximum
Cell width	40	105
Cell length	55	140
Thickness	2	6

The basic process flow for the production Lithium polymer rechargeable batteries realized by Sollith Batteries is shown in figure 1.





Important Names, Data, Events
Annual Report 2004

Lecturing Assignments at Universities

H. Bernt:
Halbleitertechnologie I und II, Technische Fakultät der Christian-Albrechts-Universität, Kiel

A. Heuberger:
Lehrstuhl für Halbleitertechnologie, Christian-Albrechts-Universität, Kiel

Memberships in Coordination Boards and Committees

T. Ahrens:
Member of ELF NET (European Leadfree Network)

T. Ahrens:
Coordinator of AOI-Anwenderkreis (Automated Optical Inspection)

T. Ahrens:
Member of DVS Fachausschuss Löten

T. Ahrens:
Member of DVS Fachausschuss Mikroverbindungstechnik

T. Ahrens:
Member of Hamburger Lötzirkel

W. H. Brünger:
Member of Steering Committee: Electron, Ion and Photon Beams and Nanofabrication, EIPBN, USA

W. H. Brünger:
Member of VDI Fachausschuss: Maskentechnik, VDI, Düsseldorf

W. H. Brünger:
Section Head: Micro and Nano Engineering, MNE 04, Rotterdam

J. Eichholz:
Member of MEMSTAND Workshop International Steering Committee

A. Heuberger:
Advisory Editor of International Journal of Semiconductor Manufacturing Technology; Microelectronic Engineering

A. Heuberger:
2. Chairman of an International Conference on Micro Electro, Opto, Mechanic Systems and Components

K. Pape:
Member of VDI Fachausschuss Assembly Test, VDI, Frankfurt

K. Pape:
Member of BVS, Bonn

K. Pape:
Member of FED

W. Reinert:
Speaker of working group „Wafer level packaging" in ZVEI

W. Reinert
Member of Arbeitskreis A 2.4 Drahtbondtechnik, DVS

M. Reiter:
Member of Gf Korr "Arbeitskreis Korrosionsschutz in der Elektronik"

M Reiter:
Member of "Arbeitskreis Lotpasten"

M Reiter:
Member of "Arbeitskreis Bleifreie Verbindungstechnik in der Elektronik"

M Reiter:
Member of "Industrie-Arbeitskreis Know-How-Transfer mikrotechnischer Produktion"

G. Zwicker:
Head of Fachgruppe Planarisierung/ Fachausschuss Verfahren/ Fachbereich Halbleitertechnologie und –fertigung der GMM des VDE/VDI

Distinctions

Rainer Hintsche (ISIT), Walter Gumbrecht (Siemens), Roland Thewes (Infineon)
Deutscher Zukunftspreis 2004, Preis des Bundespräsidenten für Technik und Innovation: Labor auf dem Chip – elektrische Biochiptechnologie, Berlin, November 11, 2004

Peter Merz
MAZ level one Award: Glass Flow-Process for Custom-sized microlenses, Hamburg, June 17, 2004

Cooperation with Institutes and Universities

Universität Autonoma de Barcelona, Spain

Hahn-Meitner-Institut, Berlin

Robert-Koch-Institut, Berlin

Rijksinstituut voor Volksgezondheid en Milieu, Bilthoven, Netherlands

Technische Universität Braunschweig, Institut für medizinische Informatik

Veterinary and Agrochemical Research Centre, Brüssel, Belgium

Cambridge University, UK

Organisatie voor Toegepast Natuurwetenschappelijk, Delft, Netherlands

Rutherford Appleton Laboratories, Didicot, UK

Technische Universität Dresden, Institut für Halbleiter- und Mikrosystemtechnik

VTT, Espoo, Finland

Fachhochschule Flensburg

University of Gdansk, Poland

University of Greenwich, UK

Ernst-Moritz-Arndt-Universität (EMAU), Greifswald

CEA Leti, Grenoble, France

Universitätskrankenhaus Eppendorf, Hamburg

Universität Hamburg, Abteilung für Biochemie und Molekularbiologie

Universität der Bundeswehr, Hamburg

BAE SYSTEMS Advanced Technology Centre, Hamshire, UK

Fachhochschule Westküste, Heide

Technical University of Budapest, Department of Electronic Technology, Hungary

Technische Universität, Ilmenau

Joint Research Centre Ispra, Italy

Institut für Fügetechnik und Werkstoffprüfung (IFW), Jena

Christian-Albrechts-Universität, Technische Fakultät, Kiel

Fachhochschule Kiel

MIMOS, Kuala Lumpur, Malaysia

École Polytechnique Fédérale de Lausanne, Switzerland

IMEC, Leuven, Belgium

University of Linkoeping, Sweden

CNRS-Université Claude Benard, Lyon, France

Consejo superior de Investigaciones Cientificas, Madrid, Spain

Universität, Madrid, Spain

Max Planck Institut für Polymerforschung, Mainz

Institut für Diabetesforschung, München

Wehrwissenschaftliches Institut, Munster

CSEM, Neuchâtel, Switzerland

Safety Equipment Development AB, Ösköldsvik, Sweden

SINTEF, Oslo, Norway

Universität Oulu, Finland

Centre National de la Recherche Scientifique, Pa laiseau, France

Universtity of Pavia, Italy

National Inst. for NBC Protection, Pribram, Czech Republic

Royal Institute of Technology (KTH), Stockholm, Sweden

Swedish Defence Research Agency, Stockholm, Sweden

VTT, Technical Research Center of Finland, Tampere, Finland

VDI/VDE-Technologenzentrum Informationstechnik, Teltow

LAAS-CNRS, Toulouse, France

Centre d'Etude le Bouchet, Vert le Petit, France

Fachhochschule Wedel

Technische Universität, Wien, Austria

Trade Fairs and Exhibitions

SMT Hybrid Packaging 2004.
System Integration in Micro Electronics, Exhibition and Conference,
June 15 – June 17, 2004, Nürnberg

Optatec 2004.
7. International Trade Fair for Future Optical Technologies, Components, Systems and Manufacturing,
June 22 – June 25, 2004, Frankfurt/Main

Electronica 2004.
21. International Trade Fair for Components and Assemblies in Electronics,
November 9 – November 12, 2004, München

Miscellaneous Events

"Aspekte moderner Siliziumtechnologie"
Public lectures. Monthly presentations, ISIT, Itzehoe

ISIT presentation at BMBF Kick-off conference
"Mikrowelten – Zukunftswelten", February 4 – February 5, 2004, Berlin

Der Lötprozess in der Fertigung elektronischer Baugruppen
Seminar: March 1 – March 3 and October 18 – October 20, 2004, ISIT, Itzehoe

SMT-Rework-Praktikum auch mit bleifreien Loten
Seminar: April 20 – April 22 and November 2 – November 4, 2004, ISIT Itzehoe

Manuelles Löten von SMT-Bauelementen auch mit bleifreien Loten
Seminar: April 20 – April 22 and November 2 – November 4, 2004, ISIT, Itzehoe

12. CMP Users Meeting
April 23, 2004, Forum am Deutschen Museum, München

Bleifreie Löttechnik
Seminar: May 5 – May 6, 2004, ISIT, Itzehoe

Regular Europractice Workshop
"Microsystem Production in Europe", May 25 – May 26, 2004, Hamburg/Itzehoe

ISIT presentation for Heide Simonis and an international delegation of ambassadors.
Speaker: Prof. Anton Heuberger, June 24, 2004, ISIT, Itzehoe

Day of open house
together with Vishay, SMI, Sollith Batteries, Condias and IZET, August 21, 2004, Itzehoe

13. CMP Users Meeting
October 15, 2004, TU-Dresden

Press conference "Hohe Investitionen in Zukunftstechnologien am High-Tech-Standort Itzehoe".
Speakers: Dr. Bernd Rohwer (Wirtschaftsminister des Landes Schleswig-Holstein), Dr. Gerald Paul (President and COO of Vishay Intertechnology) and Prof. Anton Heuberger, October 27, 2004, ISIT, Itzehoe

MEMS workshop: Vacuum Wafer Bonden.
ZVEI – Seminar,
December 17, 2004, Stuttgart

Scientific Publications

Journal Papers and Contributions to Conference

H. Etzel, H. Oertel, R. Dudde, P. Staudt:
Analysis of Wafer Process Duration for ab initio Calculation of Capacity, Throughput and Bottleneck Equipments in a Wafer Fab. Proceedings Annual, IEEE/SEMI ASMC, 2004

M. Gabig-Ciminska, H. Andresen, J. Albers, R. Hintsche, S. -O. Enfors:
Identification of Pathogenic Microbiol Cells and Spores by Electrochemical Detection on a Biochip. Microbiol Cell Factories, 3:2, April 16, 2004

M. Gabig-Ciminska, A. Holmgren, J. Albers, R. Hintsche, M. Los, A. Czyz, G. Wegrzyn, S. -O. Enfors:
Detection of Bacteriophage Infection and Prophage Induction in Bacterial Cultures by Means of Electric DNA Chips. Anal Biochem., January, 324(1), p. 84 – 91, January 1, 2004

M. Gabig-Ciminska, A. Holmgren, H. Andresen, K. Bundvig Barken, M. Wümpelmann, J. Albers, R. Hintsche, A. Breitenstein, P. Neubauer, M. Los, A. Czyz, G. Wegrzyn, G. Silfversparre, B. Jürgen, S. Schweder, S.-O. Enfors:
Electric Chips for Rapid Detection and Quantification of Nucleic Acids. Biosens Bioelectron., January, 19(6), p. 536 – 46, January 15, 2004

H. Jacobsen, E. Stachowiak, G. Zwicker, W. Lortz, R. Brandes:
Metrological Assessment of the Coefficient of Friction of Various Types of Silica Using the Motor Current During ILD-CMP. Advances in Chemical-Mechanical Polishing, MRS Symp. Proc. 816, K3.3.1, Warrendale, PA, 2004

T. Lisec, C. Huth, B. Wagner:
Dielectric Material Impact on Capacitive RF MEMS Reliability. Proc. 34. European Microwave Conference, p. 73 – 76, Amsterdam, 2004

T. Lisec, C. Huth, M. Shakhray, B. Wagner, C. Combi:
Surface-Micromachined Capacitive RF Switches with High Thermal Stability and Low Drift using Ni as Structural Material. Proc. 5th Workshop on MEMS for Millimeter-wave Communications, MEMSWAVE 2004, C33 – C36, Uppsala, 2004

G. Mörsch, G. Zwicker:
Planarization with CMP for MEMS Fabrication. Semiconductor Manufacturing, p. 48 – 50, November, 2004

E. Nebling, T. Grunwald, J. Albers, P. Schäfer, R. Hintsche:
Electrical Detection of Viral DNA Using Ultramicroelectrode Arrays. Anal Chem., February, 76(3): p. 689 – 696, February 1, 2004

M. H. Poech:
Schädigungsmechanismen in bleifreien und bleihaltigen Lötverbindungen bei erhöhter Temperatur. GMM Fachbericht 44, „Elektronische Baugruppen", DVS/GMM 2004, p. 273 – 278, VDE Verlag GmbH, Berlin Offenbach, 2004

M. H. Poech:
Modelling of Thermal Aspects of Power Electronic Assemblies. Proceedings IMAPS Nordic Annual Conference, p. 120 – 125, Helsingor, Denmark, September 26 – September 28, 2004

W. Reinert:
Vacuum Wafer Bonding Technology. Proceedings IMAPS Nordic Annual Conference, Helsingor, Denmark, September 28, 2004

H. Schimanski, Thomas Harder:
Laserlöten von Silizium/Pyrex mittels Glaslot zur Kapselung von Mikrosensoren auf Waferebene. Plus-VTE Produktion von Leiterplatten und Systemen, Eugen G. Leuze Verlag, p. 1010, June, 2004

H. Schimanski, M. H. Poech:
Untersuchungen zur Unterfüllung von Bauteilen mit flächig verteilten Lötanschlüssen in der Oberflächenmontagetechnik. Plus-VTE Produktion von Leiterplatten und Systemen, Eugen G. Leuze Verlag, p. 2118, December, 2004

L. v. Trotha, G. Mörsch, G. Zwicker:
Advanced MEMS Fabrication Using CMP. Semiconductor International, p. 54 – 56, August, 2004

X. Xie, D. Stüben, Z. Berner, J. Albers, R. Hintsche, E. Jantzen:
Development of an Ultramicro-electrode Arrays (UMEAs) sensor for Trace Heavy Metal Measurement in Water. Sensor and Actuators, Band 97, p. 168 – 173, 2004

G. Zwicker:
Advanced CMP Technology and Applications. ECS Proc., Vol. 2004-11, p. 235 – 243, 2004

G. Zwicker, H. Jacobsen, W. Lortz, E. Stachowiak, R. Brandes:
Characterisation of Oxide-CMP Slurries with Fumed-Silica Abrasive Particles Modified by Wet-Jet Milling. Proc. 9. CMP-MIC, p. 216 – 223, Marina del Rey, February, 2004

Talks and Poster Presentations

T. Ahrens:
Lötqualität. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, March 1 and October 18, 2004

T. Ahrens:
Baugruppen- und Fehlerbewertung. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, March 2 and October 19, 2004

T. Ahrens:
Was wird anders durch bleifreies Löten. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, March 3 and October 20, 2004

T. Ahrens:
Bleifreies Löten: Nicht nur eine Prozess-, sondern auch eine Managementaufgabe. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, March 3, 2004

T. Ahrens:
Betriebszuverlässigkeit elektronischer Baugruppen. 7. Europäisches Elektroniktechnologie-Kolleg, Technologien für die elektronische Baugruppe, Mallorca, March 19, 2004

T. Ahrens:
Bleifrei Reparaturlöten. Seminar: Manuelles Löten von SMT-Bauelementen auch mit bleifreien Loten, ISIT, Itzehoe, April 20 and November 2, 2004

T. Ahrens:
Rework-Qualifikationen vor dem Serienprozess. Seminar: Forum Bleifreie Löttechnik, ISIT, Itzehoe, May 5, 2004

T. Ahrens:
Reliability of Lead-Free Solder Joints. Conference: Status in Lead-free Electronics Assembly Copenhagen, June 14 – June 15, 2004

H. Schimanski:
Reparatur komplexer SMT-Baugruppen. Seminar: Manuelles Löten von SMT-Bauelementen, ISIT, Itzehoe, April 20 and November 2, 2004

H. Schimanski:
Einführung in die bleifreie Reparatur. Finetech Workshop "Grüne Reparatur", Berlin, May 13, 2004

H. Schimanski:
Beurteilung von bleifreien Lötergebnissen mittel AOI und AXI. Finetech Workshop "Grüne Reparatur", Berlin, May 13, 2004

H. Schimanski:
Rework-Strategien für bleifreies Löten – Sichere Prozessführung durch Optimierung und Festlegung der Arbeitsschritte. OTTI-Profiforum, Produktion elektronischer Baugruppen, Regensburg, May 24 – May 25, 2004

H. Schimanski:
Unterfüllung von Bauteilen mit flächig verteilten Pb-haltigen und Pb-freien Lötanschlüssen in der SMD-Technik. 12. FED-Konferenz: Elektronik-Design Leiterplatten Baugruppen 2004, Neu-Ulm, September 18, 2004

H. Schimanski, T. Ahrens, J. Pontow, D. Prochota:
Rework an bleifreien Elektronik-Baugruppen. Hilpert electronics Fachseminar: "Lead-Free", Baden-Dättwil, Switzerland, April 29, 2004

H. Schimanski, M.-H. Poech:
Vom Wärmefluss in der Lötanlage zum optimierten Lötprofil. Bleifrei Forum der Peter Jordan GmbH, Offenbach, April 28, 2004

B. Wagner:
Sensor Technologies and User Interfaces for Ambient Intelligence. European Micro- and Nanosystems EMN04, MIMOSA Satellite Workshop, Paris, October 19, 2004

G. Zwicker:
Wet-Jet Milling of Slurries. 12. CMP Users Meeting, Munich, April 23, 2004

G. Zwicker, W. Schreiber-Prillwitz:
Backside CMP for the Fabrication of Integrated Sensors. 13. CMP Users Meeting, Dresden, October 15, 2004

G. Zwicker:
Anwendung von CMP für die MEMS-Fabrikation. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, November 3, 2004

G. Zwicker:
Advanced CMP Technology and Applications. 3. International Conference on Semiconductor Technology (ISTC 2004), Shanghai, 2004

G. Zwicker, H. Jacobsen, W. Lortz, E. Stachowiak, R. Brandes:
Characterisation of Oxide-CMP Slurries with Fumed-Silica Abrasive Particles Modified by Wet-Jet Milling. 9. CMP-MIC, Marina del Rey, February 24 – February 26, 2004

Diploma Theses

A. Hanisch:
Entwicklung von ELISA's auf Mikroelektrodenchips zum Nachweis von Proteinen und Haptenen.
Fachhochschule Wedel, February, 2004

S. Kreutzer:
Konstruktion und Aufbau eines rechnergestützten Messplatzes zur Bestimmung der Schockfestigkeit von MEMS-Bauteilen und Aufnahme einer Messreihe.
Fachhochschule Lübeck, December, 2004

M. Kröner:
Extraktion von Materialparametern aus Resonanzmessungen.
Fachhochschule Münster, October, 2004

S. Kurnaz:
Manuelles Reparaturlöten von THT (Through hole Technology) – Bauteilen mit bleifreiem Lot.
Fachhochschule Wedel, February, 2004

A. Nerowski:
Entwicklung eines Herstellungsverfahrens von elektrischen Durchführungen aus Silizium und Glas auf Waferebene.
Fachhochschule Lübeck, October, 2004

M. Oldsen:
Entwicklung eines eutektischen Au-Si Verbindungsprozesses auf Waferebene.
Fachhochschule Wedel, September, 2004

C. Wulf:
Aufbau eines vollautomatisierten Vakuumprobermessplatzes zur Charakterisierung von mikromechanischen Drehratensensoren.
Fachhochschule Lübeck, September, 2004

General View on Projects

- Prozesse/ Verfahren für die Herstellung ultradünner Trench-IGBTs auf sub-100µm Silizium-Substraten
- Entwicklung einer UBM/BCB Technologie für Wafer Level Packaging
- Fabrication of Si-Microstructures based on SOI-Wafers
- Prozessentwicklung und Unterstützung bei der Produktion von Philips-Wafern
- Prozessierung von Wafern mittels Silizium-Trockenätzen zur Erzeugung spezieller Si-Strukturen
- Fabrication of Capacitor Structures
- Entwicklung von Post-CMP-Reinigungsprozessen für die Fertigung von zukünftigen integrierten Schaltkreisen in der Si-Technologie
- Evaluierung von Slurries zum chemisch-mechanischen Polieren von SiO_2
- Schleifen und Rückseiten-polieren von Wafern für MEMS-Anwendungen
- Entwicklung von Platinwiderständen auf Keramiksubstraten

- Untersuchung an mikromechanischen Drehraten-Sensoren
- Herstellung und Replikation von großflächigen 3D-Nano- und Mikrostrukturen
- Entwicklung von kapazitiven HF-Schaltern
- Fertigung eines Spiegelarrays mit elektrischem Anschluss und Beurteilung der Mikrospiegeltechnologie
- Entwicklung von piezoelektrischen Schichten für Si-Mikroaktuatoren
- Design schaltbarer optischer Netze
- Fabrication, Assembly and Testing of a Miniature Two-Axis Laser Scanner and a High Voltage Amplifier
- Kostengünstige Herstellung von Mikrosystemen: Verbundtechnik von Kunststoff und Silizium
- Herstellung mikrooptischer Linsenarrays aus Glas
- Herstellung mikrooptischer Linserarrays in Polycarbonat
- Entwicklung eines Wasserstoffsensors

- Microsystems platform for Mobile Service and Applications – MIMOSA
- AMICOM: Advanced MEMS for RF and Millimeter Wave Communications, Network of Excellence
- P-ML 2, Projection Maskless Lithography; Development of an Aperture Plate System

- Microsystem Manufacturing Cluster, EUROPRACTICE AMICUS
- Customer Support and Design Centre for Physical Measurement Systems, EUROPRACTICE CCMeSys
- Microactuator Competence Centre, EUROPRACTICE CCMicro
- MIMOS Training programm MEMS Design European Access to Manufacturing Service for MEMS on SOI Micromachining Technologies

- Electric DNA Chips for Bioprocess Control
- Nanoskalige elektrische Messverfahren für portable Analysesyteme niedermolekularer Verbindungen
- Aufbau einer technologischen Plattform zur Erregerdiagnostik mit Elektrischen Biochips (TTZ Kiel)
- Intelligent Controll Assistent for Diabetes, INCA

- Chipkartenbestückung mit Grautonblenden
- Ultra-Thin Packaging Solutions using Thin Silicon
- Flip Chip Die Bonder for Ultra-Thin Silicon
- Untersuchung zur Unterfüllung von Bauteilen mit flächig verteilten Lötanschlüssen in der Oberflächenmontagetechnik, CSP Underfill
- Long-Term Stability of Vacuum-Encapsulated MEMS Devices Using Eutectic Wafer Bonding, VABOND
- Stressarme Montage von Sensoren und Mikrooptik – Komponenten mittels Mikroklebtechnik
- Evaluation of packaging concepts for the gyro-sensor, Gyrosil, BMBF
- Fertigung von Testwafern zur Justierung von Bestückungsanlagen

- Die elektronische Baugruppe der Zukunft
- Stressoptimierte Montage und Gehäusetechnik für mikromechanisch hergestellte Silizium-Drehratensensoren
- Ag thick Film Bumping on Wafer Level
- Entwicklung einer AOI Kalibrierprobe
- Thin Wafer Handling for Backsite Processing
- Volumeneffekte und technische Zuverlässigkeit von bleifreien Lötstellen
- Oberflächeneffekte von Komponenten zum bleifreien Löten
- Glassfritt Vacuum Wafer Bonding
- Finepitch solder flip chip on flex
- Glaslotbonden mit strukturierten Capwafern und Musterwafern
- Bewertung von Aufbaukonzepten für ein Leistungsmodul
- Assembly test on PCB
- Qualitätsbewertung an bleifreien Baugruppen
- Musterfertigung von Blendenkarten mit Soft-Blenden

- Hearing-Aids with Rechargeable Power Supply, HARPOS

Patents

Patents

P. Birke, G. Neumann
Pastöse Massen mit Nanokristallinen Materialien für elektrochemische Bauelemente und daraus hergestellte Schichten und elektrochemische Bauelemente
TW 195841

P. Birke, G. Neumann
Pastöse Massen mit anorganischen, flüssigen Leitern und daraus hergestellte Schichten und elektrochemische Bauelemente
TW 195404

P. Birke, G. Neumann
Paste-like masses for electrochemical components, layers produced therefrom, and electrochemical components
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We would be glad to answer your questions.

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