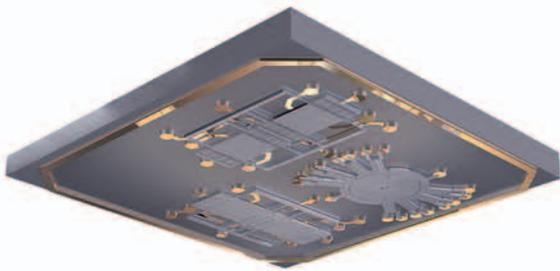
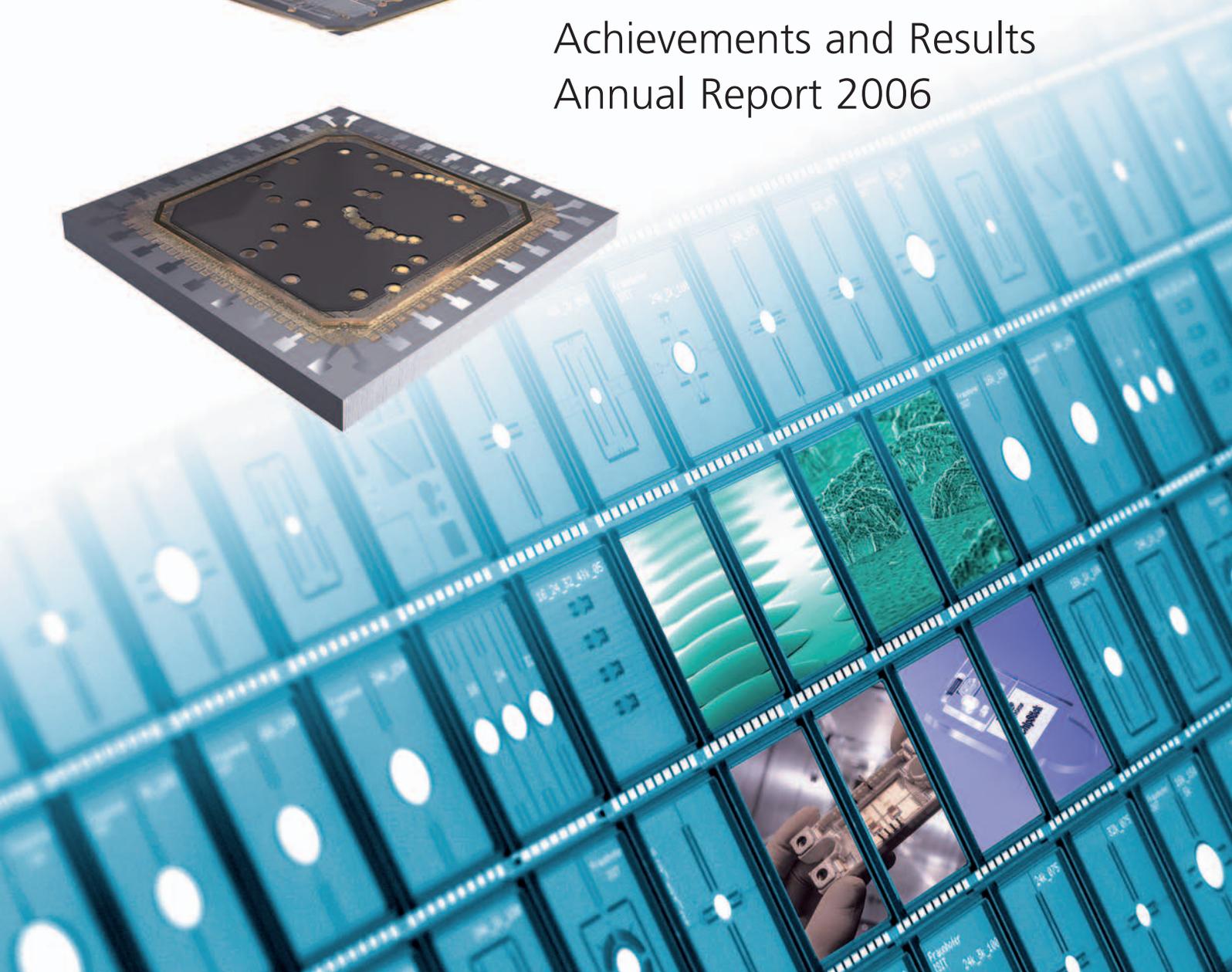
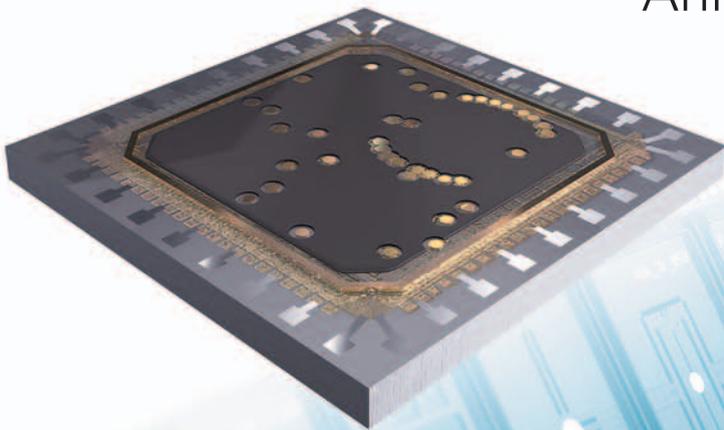




**Fraunhofer** Institut  
Siliziumtechnologie



Achievements and Results  
Annual Report 2006



Achievements and Results  
Annual Report 2006

# Achievements and Results Annual Report 2005

Preface .....	6	<b>Representative Results of Work</b>	<b>Important Names, Data, Events</b>
<b>Brief Portrait</b>		<b>Microsystems Technology</b>	Lecturing Assignments at Universities ..... 66
Fraunhofer ISIT Research and Production at one Location .....	12	Mass Flow Sensor for Measurement of Liquids (Water) .....	32
<b>Main Fields of Activity</b>		Wafer-Level Package MOEMS .....	36
Microsystems Technology (MEMS) and IC Design .....	14	Applications of Sputtered Piezoelectric Thin Films .....	38
IC Technology and Power Electronics .....	16	Development of a Crystal Silicon Force/Torque Sensor .....	42
Biotechnical Microsystems .....	18	MEMS-Test and Diagnostics .....	44
Packaging Technology for Microelectronics and Microsystems .....	19	<b>IC-Technology</b>	
Quality and Reliability of Electronic Assemblies .....	20	Nano Structures for CNT Transistors .....	46
Integrated Power Systems .....	21	Ultrathin Laser Anneal Fieldstop Trench IGBTs .....	48
Facilities and Equipment .....	22	<b>Biotechnical Microsystems</b>	
<b>Offers for Research and Service</b>		Detection of Antibodys in Human Serum with Electrical Biochips .....	50
Spectrum of Services .....	23	<b>Module Integration</b>	
Customers .....	24	The Ultimate Miniaturization of Microsystems Packaging .....	52
Innovation Catalogue .....	26	Hermeticity Testing of Vacuum- Sealed Microresonators .....	54
<b>Representative Figures</b> .....	28	Ultra Thin Die Connection by Isotropic Conductive Adhesive .....	58
<b>The Fraunhofer-Gesellschaft at a Glance</b> .....	30	Joint Industrial Research on Lead-Free CSP Reliability .....	59
			<b>Scientific Publications</b>
			Journal Papers and Contributions to Conferences .....
			69
			Talks and Poster Presentations .....
			70
			Diploma Theses .....
			71
			<b>General View on Projects</b> .....
			72
			<b>Patents</b> .....
			73
			Contact and Further Information .....
			75
			Imprint .....
			75



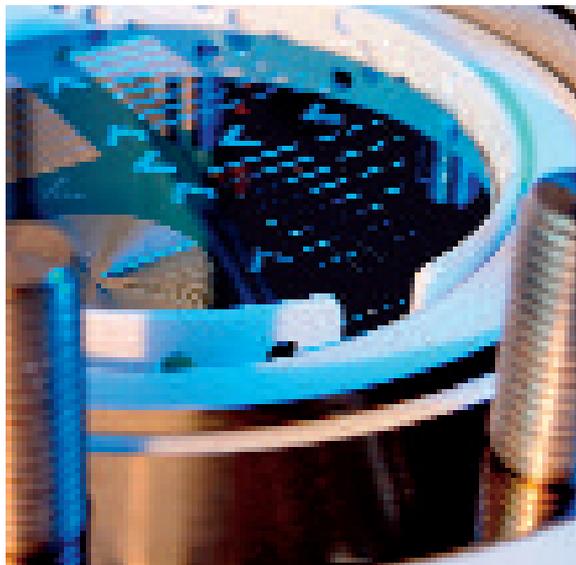
Wafer with different designs of two axis micromirror chips.

# Preface

In 2006, ISIT once again succeeded in acquiring numerous national and international research projects. Synergy effects between the various ISIT departments themselves and with local industries have thus accelerated the growth of the location as a centre for micro technologies. ISIT has now entered the fields of nano electronics and nano systems engineering with new research projects, for example in power electronics. The Institute meanwhile offers a full range of services in the field of microsystems engineering – system development, design, simulation, prototyping and production – and has increasingly begun to win major projects in which several of its departments are simultaneously involved.

One of the most extensive microsystems engineering projects, and one that is of paramount importance for the whole Institute, took a significant leap forward last year: the development and preparation for the production of an angular rate sensor (gyro) for the automotive industry in collaboration with SensorDynamics AG (SD), a specialist in the integration of innovative sensor systems. With several members of staff at the Itzehoe location, SD is currently preparing to embark on industrial series production. In the context of this cooperative venture, ISIT supports the weekly production of roughly three to four thousand such sensor elements for quality verification at a customer's facilities. In addition, SD and ISIT are already developing the next generations of angular rate and acceleration sensors and a range of integrated circuits for various sensor systems. In launching gyro production, we have gained an important reference for the acquisition of further industrial projects.

The Institute's cooperation with our largest industrial partner, Vishay Siliconix Itzehoe GmbH, is making excellent progress. The company has been sharing the use of the ISIT cleanroom facilities for ten years now. This was reason enough for Vishay to celebrate this 'round' anniversary in the presence of Schleswig-Holstein's minister of economics Dietrich Austermann, Vishay Intertechnology's president and COO Dr. Gerald Paul, as well as numerous representatives of ISIT. The success story began ten years ago, when Siliconix – a company that was at that time still part of the Daimler Benz group – was



Drying process for cantilever type MEMS structures.

looking for ways of increasing its PowerMOS production capacities and took the decision for Fraunhofer ISIT in Itzehoe. Within a very short time, the staff of ISIT and Vishay Siliconix established a professional industrial semiconductor production line. This represented a new form of cooperation between industry on the one hand, and research and development on the other, which was to become exemplary for Germany and many other European countries. In technological terms, too, the production line has undergone a truly impressive development. When production started in 1997, the line was turning out 1500 wafers per week using the old planar technology. Today, ten times as many wafers are produced using the vastly more complex trench technology.

The successful work of ISIT and Vishay is also to be continued in the future. The partners have entered into a contractual agreement for a further ten-year period of cooperation. This provides the basis for securing the continued success of Itzehoe as a hightech location. Between 2005 and 2008, Vishay will invest 80 million U.S. dollars in Itzehoe to upgrade the entire production line from 150 mm wafers to 200 mm wafers. For ISIT, this investment means that the Institute will



ISIT presentation at the exhibition „Innovation & Wirtschaft“ in the framework of „Bürgerfest zum Tag der Deutschen Einheit“ in Kiel.



continue to be able to offer its customers research and development services on a state-of-the-art industrial production line.

We have also seen some positive new developments at the Itzehoe high-tech industrial location. Bullith Batteries, a spin-off of the 'integrated power systems' department at ISIT, has merged with the Swiss battery manufacturer Leclanché SA. This merger opens up significantly greater opportunities for both companies in terms of the commercialization and global marketing of advanced Lithium-polymer battery technology. The activities of Bullith Batteries stand to gain from the industrial background and the manufacturing and sales know-how of the old-established Swiss company, while the merger with top technology provider Bullith Batteries gives Leclanché a clear competitive edge and enables the company to gain a technological lead and position itself in niche markets with a high value chain.

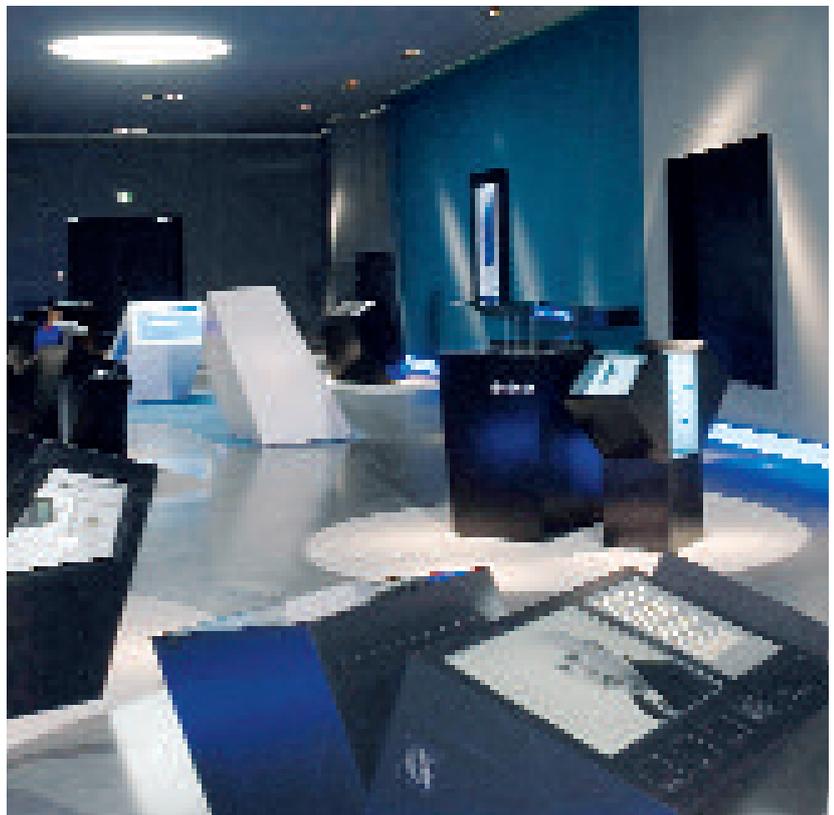
After a period of nearly one year without a director, the IZET innovation center is in capable hands once more. Prof. Dr. Ralf Thiericke was appointed managing director of the Gesellschaft für Technologieförderung Itzehoe mbH (IZET) in June 2006, and will manage the business of expanding Itzehoe as a high-tech location. The chemistry professor succeeds Dr. Ingo Hussla, who died in 2005. Prof. Thiericke faces a challenging task given that the attractiveness and potential of a region are decisively influenced by the persons who are active there. He is particularly suited to this position by virtue of his long experience in the transfer of scientific expertise and the start-up and development of companies, as well as his activities in technology and business development.

It was undoubtedly a setback for Itzehoe as a high-tech location when Silicon Manufacturing Itzehoe (SMI) ceased its business operations end of 2006. The closure of SMI was the result of a decision within the Philips group to hive off its semiconductor activities to NXP. The SMI products were not compatible with NXP's previously defined range of products. However, the loss of this former Philips subsidiary also provides an opportunity for restructuring the Itzehoe industrial location.



Timm-Florian Kraft (middle) earns the distinction of being his year's top student in the final examination as a materials tester (specializing in semiconductor technology), for which he was awarded a prize by Fraunhofer board member Dr. Dirk-Meints Polter (right). Left: ISIT training officer Jan Lähn.

View to the exhibition „Turning ideas into success“. The Deutsche Museum in Munich presents the prize winning projects of the German Future Prize e.g. Dr. Rainer Hintsche's work on electrical biochip technology.

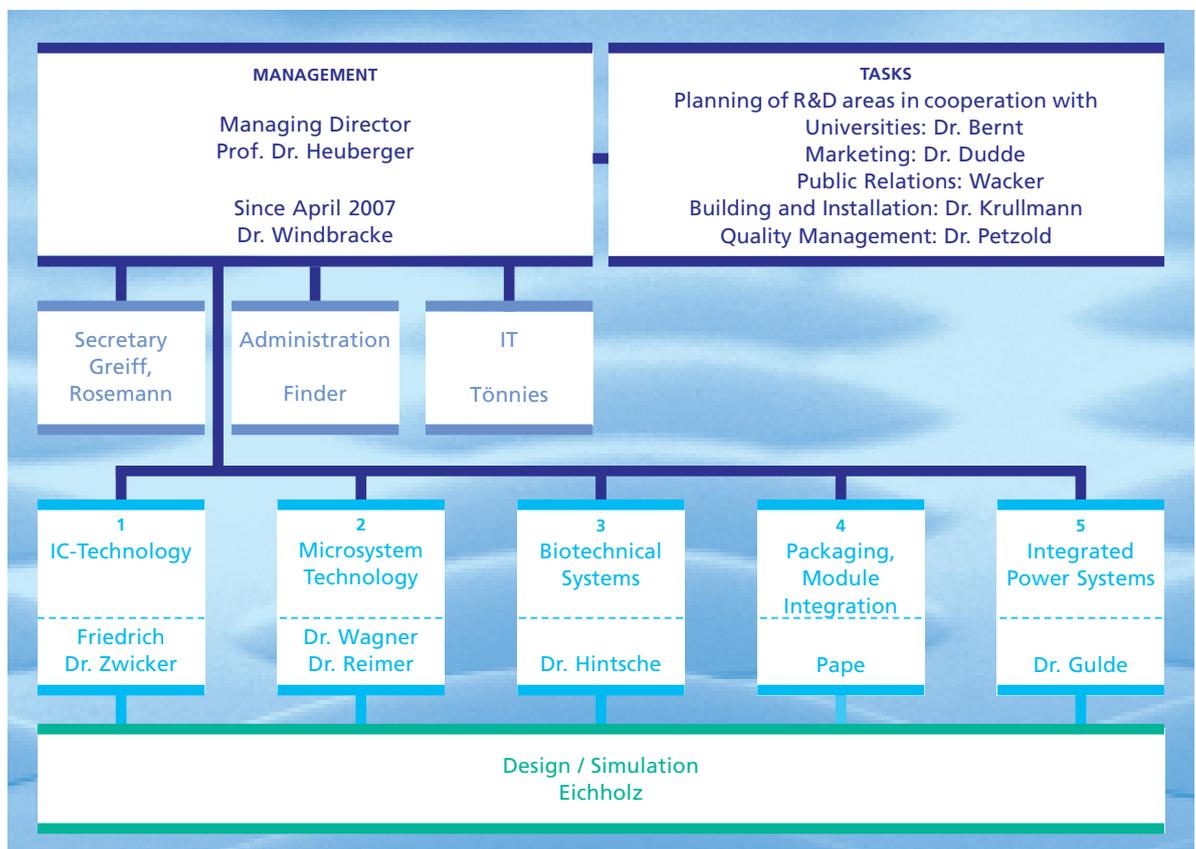


# Preface

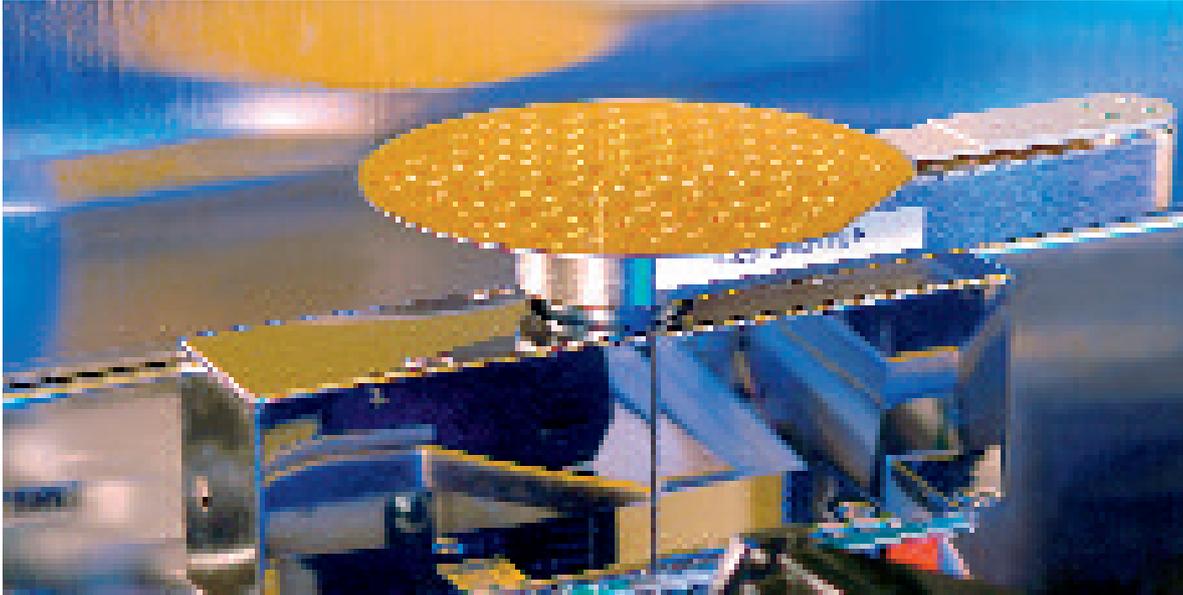
Now we can work on creating an integrated solution that includes buying back the red office building and the ground slab that has already been cast. Plans are under development to build a new semiconductor cleanroom, thanks to new opportunities presented by Schleswig-Holstein being once again declared an EU development area as of 2007. We are therefore once again entitled to claim financial support for our industrial location from the European Regional Development Fund. The construction costs amount to nearly 100 million Euros. Various users will install facilities there in order to set up the requisite production lines for their products. One of them is Vishay, which has already expressed an interest in the office building, but there are other partners as well, for instance a company that manufactures glass substrates. Preparations for this project are already well advanced.

The expertise accumulated in the past, and particularly the close interconnection between research and development, is gaining the attention of the public and corresponding recognition. Since December 19th, 2006, some of the development highlights from ISIT can be viewed at the Deutsches Museum in Munich, namely Dr. Rainer Hintsche's work on electrical biochip technology, which won the German Future Prize (the German President's Prize for Technology and Innovation) in 2004. On the initiative of Germany's president Horst Köhler, the 'German Museum for Masterpieces of Natural Science and Technology' – to give it its full name – set up an exhibition about the German Future Prize to mark the tenth anniversary of its foundation. The motto is: 'Turning ideas into success. For people. For the country'. The exhibition shows the special

ISIT Organigram



Wafertransfer in a resist coating module.



approach and the lasting effect of each of the prize-winning projects and honors the men and women who, in their capacity as researchers and developers, are turning the future into a present-day reality. For Dr. Rainer Hintsche and also for ISIT, it is a great honor to have his work displayed in this setting.

Finally, a word concerning my own person. I shall be retiring and leaving ISIT in 2007. An appointment committee jointly set up by the CAU and the Fraunhofer headquarters has already convened several times and selected possible candidates for

the post. In addition to directing the Institute, my successor will hold a professorship for silicon-based micro and nano systems engineering at Kiel university. I would like to thank my colleagues for their tremendous commitment and all the work they have done over the years, without which ISIT could never have achieved the success it enjoys today. I wish my successor the breadth of vision and patience to accompany his skill in fulfilling the tremendous task of expanding ISIT and the high-tech industrial location of Itzehoe and in generating new prospects for the future of the Institute.

  
Anton Heuberger

## Fraunhofer ISIT

### Research and Production at one Location

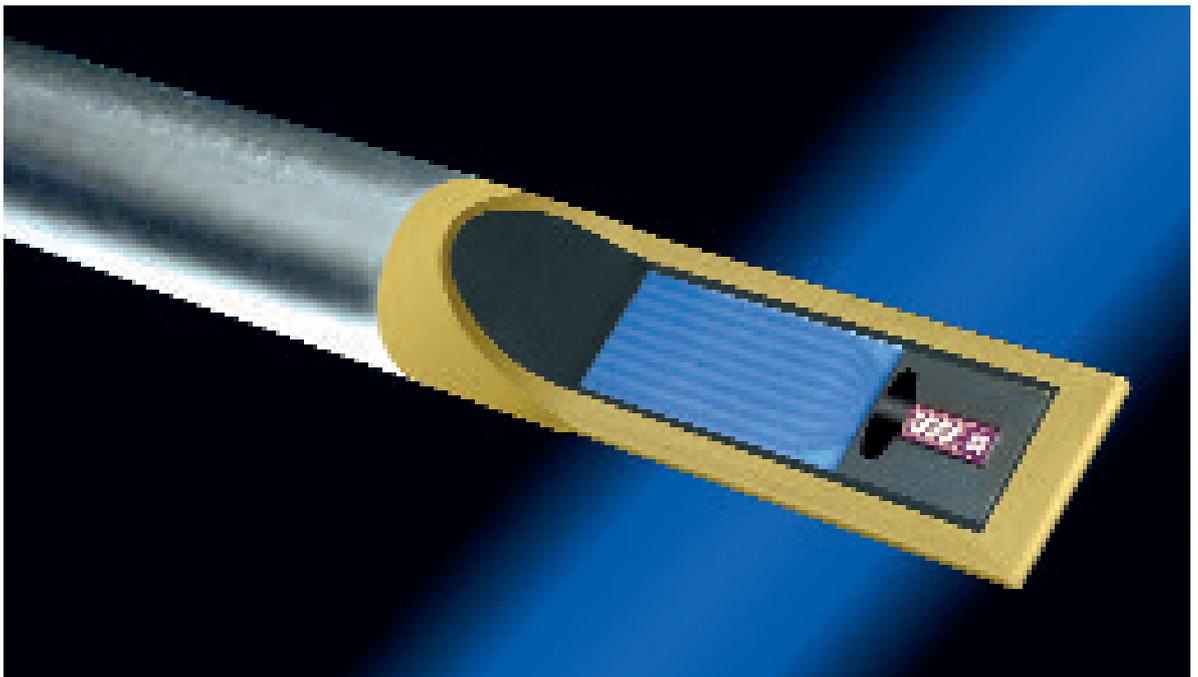
The Fraunhofer-Institut für Siliziumtechnologie (ISIT) develops and manufactures components in microelectronics and microsystems technology, from the design phase – including system simulation – to prototyping and fabrication of samples, up to series production. Though components such as valves and deflection mirrors manufactured by Fraunhofer ISIT often measure just a fraction of a millimeter in size, their range of applicability is anything but small: the devices are implemented in areas as diverse as medicine, environmental and traffic engineering, communication systems, automotive industry, and mechanical engineering. Working under contract, ISIT develops these types of components in accordance with customer requirements, also creating the application-specific integrated circuits (ASICs) needed for the operation of sensors and actuators. Included in this service is the integration into the overall microsystem using miniaturized assembly and interconnection technology.

Together with Vishay Siliconix Itzehoe GmbH, the institute operates a professional semiconductor production line which is up-to-date in all required quality certifications. The line is used not only for producing microelectronic components (PowerMOS) and microsystems, but also for R&D projects aimed at developing new components and technological processes. An ISO-9001-certified quality management system serves as the basis for the development, qualification and production of micro-engineered components.

Other groups at ISIT carry out work on assembly and packaging techniques for microsystems and sensors, analyze the quality and reliability of electronic components, and develop advanced power-supply components for electronic systems.

The institute employs a staff of around 150.

Prototype of a water flow sensor system.





## Main Fields of Activity

# Main Fields of Activity

## Microsystems Technology (MEMS) and IC Design

The work performed at the institute focuses predominantly on microsystems technology, an area which ISIT has pioneered in Germany. For over 20 years ISIT scientists have been working on the development of micromechanical sensors and actuators, micro-optic, and components for radio-frequency applications (RF-MEMS). Their work in this area also includes integrating these components with microelectronics to create small-size systems of high functionality. A multitude of components and systems have originated at ISIT.

The current emphasis in the area of sensor technology is on inertial sensor technology (acceleration, angular rate, inertial measurement units), pressure, and flow sensors, all with integrated electronics (ASICs). A microsensor core technology using thick polysilicon structural layers and waferlevel hermetic sealing is available.

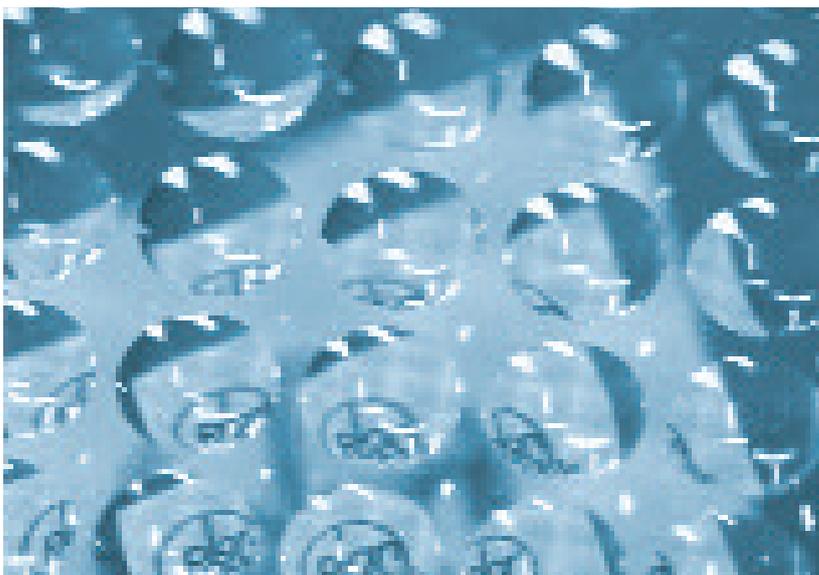
The development of customized integration concepts, ranging from simple, cost-effective assembly in a common package to complete monolithic integration, represents the core of

ISIT's offerings in this area. One integration technique that customers may find particularly valuable is the ability to mount a microsystem on the surface of a fully processed ASIC wafer using a low-temperature process such as electroplating.

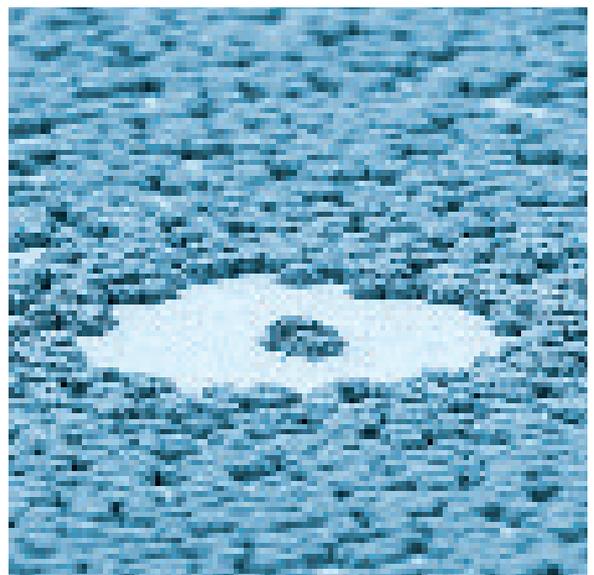
ISIT also develops optical microsystems, primarily for optical instrumentation, consumer products and communication. Examples include micromirrors for laser projection displays, laser scanners and analog or digital light modulators, and passive optical elements such as refractive and diffractive lenses, prisms, or aperture systems.

Radio-frequency microsystems developed at ISIT, designed primarily for use in reconfigurable wireless communication devices, include RF-MEMS switches, tunable capacitors and ohmic switches.

On-chip integrated microactuator systems are especially challenging in order to meet the specific requirements in the micro- and nanometer scale. In this field ISIT has a high expertise and implements electrostatic, thermal and – more



Microlenses, made of borosilicate glass (in cooperation with PlanOptik).



PZT-Perovskite crystals embedded in an amorphous matrix.



Wafer handling system in the new established epitaxy division.

recently – high-speed high-force piezoelectric actuation principles on silicon wafers.

The service approach enables ISIT to offer its customers all of these components as prototypes and also to manufacture them in series according to the customer's specific needs, utilizing the quality and capacity of the institute's in-house semiconductor and MEMS production line. The services provided also include application-specific microsystem packaging at wafer level, comprising thin wafer and vertical feedthrough capabilities.

Should customer's requirements fall outside the scope of the institute's technological capabilities, ISIT can utilize an European network to gain access to other manufacturers and processes, like production lines at Bosch, SensoNor, HL Planar, ST and Tronic's. ISIT organizes the production as a foundry service for interested customers.

One of the prerequisites for the development of microsystems and microelectronic components is a highly capable circuit design group. The staff at ISIT are specialists in the design of analog/digital

circuits, which enable the electronic analysis of signals from silicon sensors. The designers at ISIT also model micromechanical and micro optic elements and test their functionality in advance using FEM and behavioral modeling simulation tools.

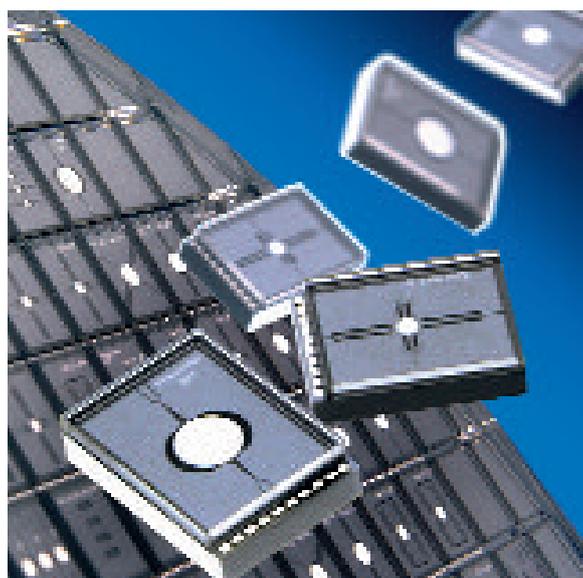
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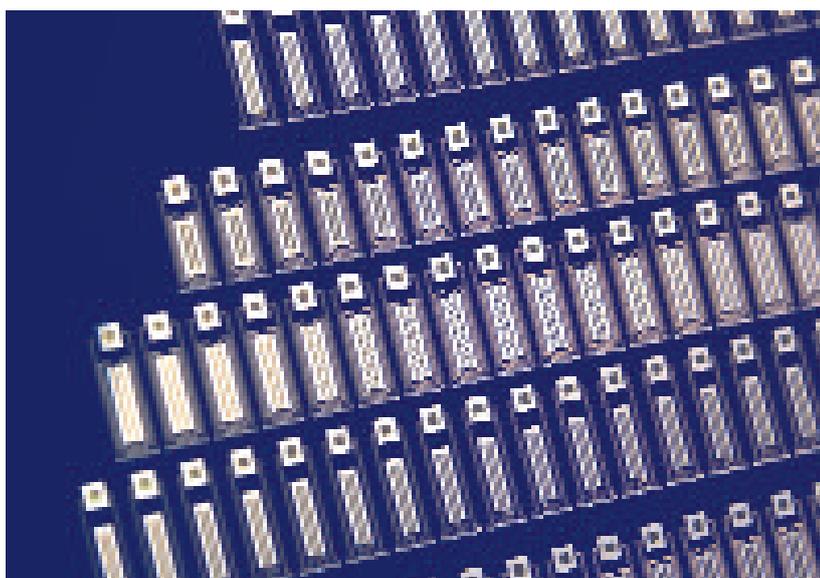
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Micromirrors, vacuum packaged on wafer level.



Wafer with different flow sensor designs.

# Main Fields of Activity

## IC Technology and Power Electronics

The power electronics and integrated circuits group develops and manufactures active integrated circuits as well as discrete passive components. Among the active components the main concern lies on power devices such as smart power chips, IGBTs, bi-directional components, PowerMOS circuits and diodes. Thereby ISIT primarily uses Vishay's customized, individual production sequences. Additional support for work in this area is provided by an array of modified tools for simulation, design and testing. ISIT also benefits from years of experience in the design and construction of CMOS circuits.

The passive components developed and fabricated at ISIT are primarily chip capacitors, precision resistors and inductors. Materials development and the integration of new materials and alloys into existing manufacturing processes play an important role in the development process.

ISIT develops individual processes, process modules and complete process flows for diverse applications. The Institute also offers customer-specific silicon components processing in small to medium-sized batches on the basis of a qualified semiconductor process technology.

To support the development of new semiconductor production techniques, production equipment of particular interest is selected for testing and optimization by ISITs staff. This practice provides the Institute with specialized expertise in challenges related to etching, deposition, lithography, and planarization methods. Planarization using chemical-mechanical polishing (CMP) in particular is a key technology for manufacturing advanced integrated circuits and microsystems.

The intensive work done by ISIT in this area is supported by a corresponding infrastructure: The institute's CMP application lab is equipped

Setting up the process for vapour phase etching at Primaxx equipment.



Placing a wafer batch into a spray acid tool for surface cleaning.



Detail from the new established RENA galvanoplaters.



with CMP cluster tools, single- and double-sided polishers and post-CMP cleaning equipment for wafers with 100 to 300 mm in diameter. The CMP group at ISIT works in close relationship to Peter Wolters AG since many years, as well as other semiconductor fabrication equipment manufacturers, producers of consumables, CMP users and chip and wafer manufacturers.

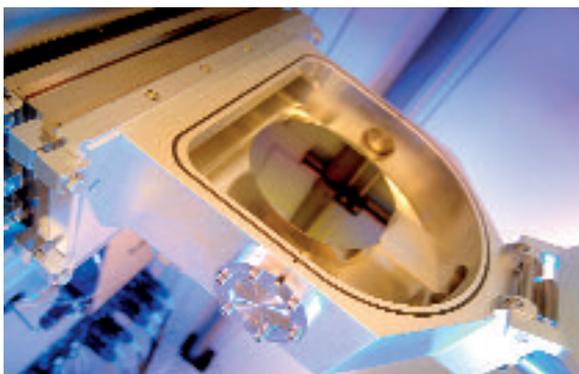
The group's work encompasses the following areas:

- Testing of CMP systems and CMP cleaning equipment
- Development of CMP processes for
  - Dielectrics (SiO<sub>2</sub>, TEOS, BPSG, low-k, etc.)
  - Metals (W, Cu, Ni, etc.)
  - Silicon (wafers, poly-Si)
- Testing of slurries and pads for CMP
- Post-CMP cleaning
- CMP-related metrology
- Implementation of customer-specific polishing processes for ICs and microsystems

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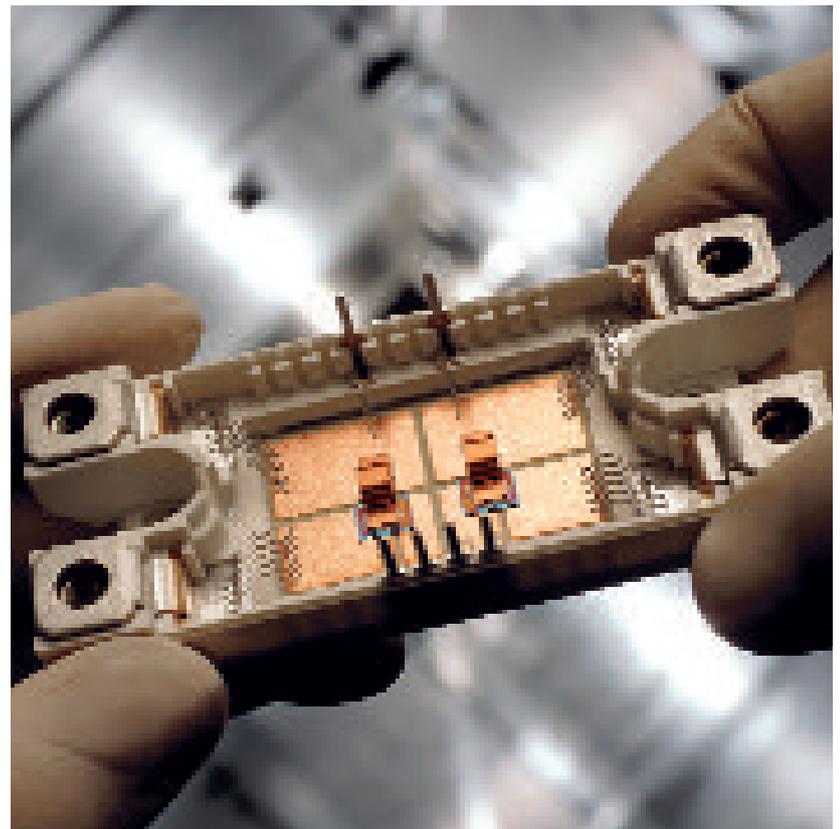
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Drying module of the Peter Wolters  
HFP 300 CMP cluster tool for 300 mm wafers.



Load lock at the Primaxx vapour phase etcher.

IGBT power module assembly based on power balling,  
manufactured in cooperation with Danfoss Silicon Power.



# Main Fields of Activity

## Biotechnical Microsystems

ISIT is worldwide leading in electrical biochip technology, and is holding around 20 patents in the area. The electrical biochips offer the intrinsic advantages vs. optical biochips because of direct miniaturization and transmission of responses of biochemical reactions into computing networks. Employing new nm-ultramicroelectrodes and integrated reference and auxiliary electrodes the construction enables powerful sensor micro arrays and the use of ultra-sensitive, ultra-selective measurement techniques, such as "redox recycling". In combination with microfluidic components and integrated electronics, these electrical micro arrays represent the fastest and most cost-effective basis for mobile analysis systems, which can be used to identify and quantify DNA, RNA, proteins and haptens.

Those electrical micro arrays, which are wireless packaged into proprietary "Chip-Sticks" are useful to detect a variety of analytes simultaneously. ISIT works closely with the Itzehoe based company eBiochip Systems GmbH ([www.ebiochip.com](http://www.ebiochip.com)), an ISIT spin-off, to facilitate the marketing of these new technologies. eBiochip Systems developed a variety of smart and portable instruments, from a low end device for education and demonstration to the high end fully automated micro array analyzer. Demonstrating very competitive applications as the identification and quantification of protein and pathogenic biowarfare agents or the antibiotics in raw milk the platform of electrical biochip technology is successfully used in several labs in Europe and in EU granted projects.

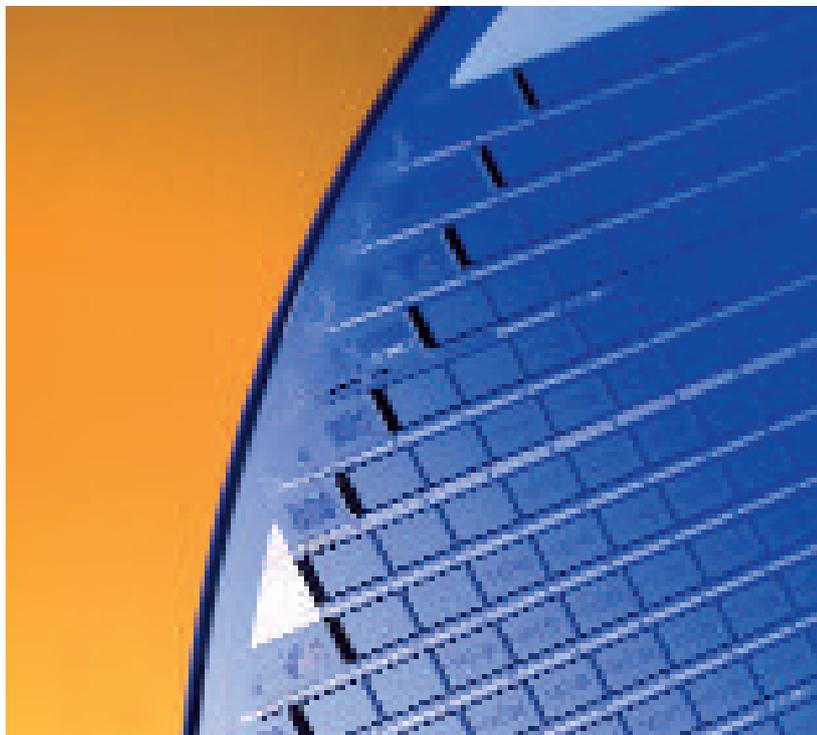
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Different automated eBiochip measuring systems to detect biological agents.



Electrical microarrays packaged in polymeric ChipSticks with integrated flow channels and reaction chambers.





## Packaging Technology for Microelectronics and Microsystems

The assembly and interconnection technology group offers customers a broad range of services, including precision assembly of microstructured components and development and qualification of customer-specific packaging. Work in this area includes hermeticity and material compatibility tests for assemblies that have to work in aggressive environmental conditions, e.g., analysis of microsystem packages intended for in vivo use in medical technology.

Another focal area is miniaturisation of chip and sensor assemblies and packages, which includes direct assembly of bare silicon chips. The institute possesses capabilities in all of the essential technical stages for chip-on-board (COB) technology, from designing the circuit boards to qualified COB assemblies. The bare ICs and microsensors are mounted using the Chip & Wire or Flip-Chip techniques.

The group also develops processes for assembling and packaging chips and sensors/actuators while still on the wafer. Due to the increasing global trend among chip manufacturers to implement this special packaging process, Wafer Level Packaging (WLP) – now considered the assembly technique of the future – has become a central focus of the group's work. WLP technology can also be applied for packaging sensors under vacuum, such as angular rate or acceleration sensors. ISIT has successfully integrated thin film getter layers for high-Q microresonators and improved vacuum lifetime.

The Institute is active in this area not only as a technology developer, but also as a manufacturer of assemblies for its customers using the available Chip-Size-Packaging production line.

The group also develops ultra-thin electronic assemblies, which involves stacked mounting flexible silicon chips as thin as 50  $\mu\text{m}$  on flexible substrates.

These techniques will ultimately lead to further miniaturization in existing systems, such as laptops, hand held PCs or mobile phones, but will also enable the development of new products like intelligent flexible product labels or smart clothes.

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3D system integration of inertial measurement units in the EU research project DAVID. A monolithic MEMS-Cluster is bonded on top of an ASIC that is covered with a getter film. The encapsulation of the movable structures takes place under vacuum.

# Main Fields of Activity

## Quality and Reliability of Electronic Assemblies

Quality evaluation – in particular for the soldering work done in pre-production, pilot and main series lots – represents a continuous challenge for ISIT, for example whenever new technologies such as lead-free soldering are introduced, when increased error rates are discovered, or if the Institute desires to achieve competitive advantages through continual product improvement. To reveal potential weak points, ISIT employs both destructive and non-destructive analysis methods, such as X-ray transmission radiography and scanning acoustic microscopy. Working from a requirements matrix, ISIT scientists also evaluate long-term behavior of lead-free and lead-containing assemblies alike. They then formulate prognoses on the basis of model calculations, environmental and time-lapse load tests, and failure analysis.

In anticipation of a conversion to lead-free electronics manufacturing, ISIT is undertaking design, material selection and process modification projects. To effect a further optimization of manufacturing processes, the Institute applies process models and produces samples on industry-compatible equipment. The group also



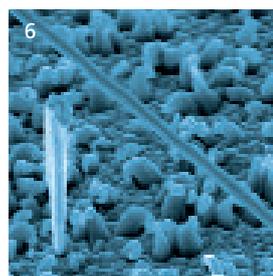
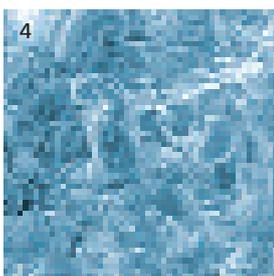
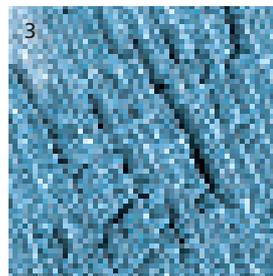
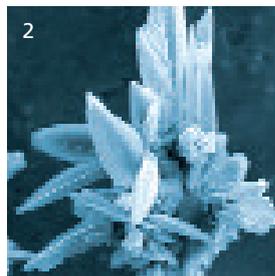
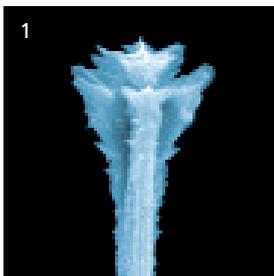
Testboard in the automated optical inspection, ISIT lead-free training line.

addresses issues related to thermal management and reliability for customer-specific power modules.

In addition to these technological activities, the group regularly holds training sessions, including multi-day classes, at the Institute or at company site.

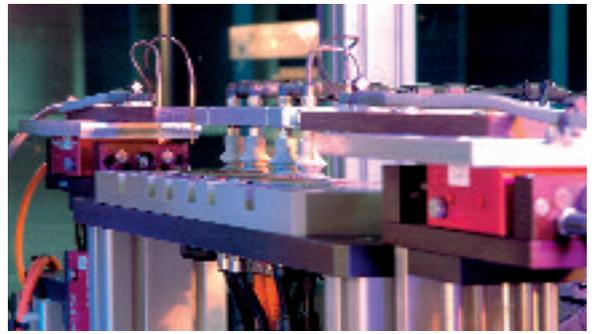
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Different scanning electron microscope pictures for analysis of electronic devices:

- 1 and 2 Silver needles
- 3 Cracks after solidification of lead-free solder alloy
- 4 First steps of Whisker growth
- 5 BGA balls
- 6 Contact surface after corrosion test



Electrical testing of battery layers.

## Integrated Power Systems

There is an ever increasing demand for high performance rechargeable batteries for mobile applications. Adequate battery solutions for mass products are available.

Applications with special needs regarding electrical performance and design of the energy storage unit call for solutions which cannot be provided by the standard battery products.

A new Lithium rechargeable battery design developed by ISIT over the last few years – for which the institute has applied for several patents – some are already granted – is capable of meeting these demands. This new concept, which features solid-state electrolytes, affords the same performance typical of Lithium-ion rechargeables, but it does not need the complicated rigid packaging technology required with conventional Lithium-ion batteries, which contain free liquid electrolytes. The battery package consists of a metallised heat-sealable plastic foil to make it air- and moisture-tight, resulting in a lower overall weight for the finished product.

ISIT's Lithium battery production process is based on the lamination of customized flexible foils containing the functional materials. This allows for tailor-made-battery solutions in a much greater variety of shapes and sizes, thus significantly diversifying the range of possible applications. Currently ISIT offers two systems characterised by different anode materials:

- The 3,7 V system is optimised with respect to power density
- The 2,3V system shows excellent robustness and long term stability

ISIT offers a variety of services: development, fabrication and small series production of customer-specific battery formats (ranging in size from micro-systems to laptops) in a broad range of available ampere-hour ratings, with various form factors and housing materials (e.g. plastic or Titanium).

Following the preparation of samples, ISIT supports the customer in the transition to series production. The institute also provides application-specific material selection of various compounds for cathodes (e.g. Lithium Cobaltite, Lithium Iron Phosphate) and anodes (Graphite, Lithium Titanate, etc.) to ensure optimal conformity to the application requirements (e.g., power density, cycle stability, capacity, product life cycle, self-discharge rate...). Battery characterisation and long-term electrical/environmental tests complete the range of services.

In close co-operation with an industrial partner ISIT established an initial production line for an industrial-scale production process, which allows for a rapid ramp up of battery production.

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Lithium polymer battery production line: automated stacking of battery layers.

# Main Fields of Activity

## Facilities and Equipment

In terms of both space and technical capabilities, the facilities at ISIT provide an ideal environment for research & development work as well as production. In addition to its 150-mm silicon technology line and 2500 m<sup>2</sup> of clean-room space (class 1), the institute has a further 450 m<sup>2</sup> of clean-room area (class 100) for specific microsystems engineering processes, including: wet-etching processes, high-rate plasma etching, deposition of non-IC-compatible materials, lithography with thick resist layers, gray-scale lithography, electroplating, microshaping and wafer bonding.

Further 200 m<sup>2</sup> clean-room (class 10-100) is equipped for chemical-mechanical polishing (CMP) and post-CMP cleaning. ISIT also offers a diverse selection of labs (1500 m<sup>2</sup>) that are utilized by working groups for the development of chemical, biological and thermal processes, electrical and mechanical component characterization, and for assembly and interconnection technology.

The ISIT facility also operates a pilot production line for Lithium-polymer rechargeable batteries with power capacities of up to several ampere-hours.



Seminar participants in the lead-free training line; page 23 right: practical work.



## Spectrum of Services

The Institute makes its range of services available to companies representing a wide variety of branches, including medical technology, communication systems, automotive industry, and industrial electronics, just to name a few. After industrial customers specify necessary requirements of the components and systems, ISIT engineers work closely with them to design, simulate and produce the components, systems and manufacturing processes. In this context, ISIT follows the technology platforms concept, which entails defining standard process flows that can be used to manufacture a large group of components simply by varying certain design parameters. Applying this modular technology concept is the optimal way to ensure that ISIT continues to offer competitive prices to its customers.

ISIT services have attractive implications for small- and medium-sized enterprises, which can take advantage of the institute's facilities and expertise in realizing technological innovations up to products.



Final adjustments at the epitaxy equipment.



# Offers for Research and Service

## Customers

ISIT cooperates with companies of different sectors and sizes.  
In the following some companies are presented as a reference:

<b>AARDEX</b> , Zug, Switzerland	<b>Basler Vision Technologies</b> , Ahrensburg	<b>eBiochip Systems GmbH</b> , Itzehoe	<b>Hella KG</b> , Lippstadt
<b>ABB</b> , Västerås, Sweden	<b>Biont</b> , Bratislava, Slovakia	<b>Elmos Semiconductor AG</b> , Dortmund	<b>Hök Instrument AB</b> , Västerås, Sweden
<b>ABB</b> , Ladenburg	<b>Bosch</b> , Reutlingen	<b>EN Electronic Network</b> , Bad Hersfeld	<b>IBM Research GmbH</b> , Zürich, Switzerland
<b>Adaptive Photonics</b> , Hamburg	<b>B. Braun</b> , Melsungen	<b>Envionics Oy</b> , Mikkeli, Finland	<b>IMS</b> , Wien, Austria
<b>Airbus-Systeme</b> , Buxtehude	<b>Bruker Daltonic GmbH</b> , Leipzig	<b>Epcos AG</b> , München	<b>Infineon Technologies AG</b> , Dresden
<b>Alcatel Vacuum Technology</b> , Annecy, France	<b>Cardi plus</b> , Sevilla, Spain	<b>Equicon</b> , Jena	<b>Jungheinrich AG</b> , Norderstedt
<b>Alma</b> , Lyon, France	<b>Carl Zeiss SMT</b> , Oberkochen	<b>ESCD</b> , Brunsbüttel	<b>Kerr McGee</b> , Krefeld
<b>Amic</b> , Uppsala, Sweden	<b>Condias GmbH</b> , Itzehoe	<b>ESW-EXTEL Systems GmbH</b> , Wedel	<b>Kristronics GmbH</b> , Harrislee-Flensburg
<b>Andus GmbH</b> , Berlin	<b>DancoTech A/S</b> , Ballerup, Denmark	<b>European Center for Power Electronics e.V.</b> , Nürnberg	<b>Lam Research</b> , Fremont, USA
<b>Applied Materials, ICT</b> , München	<b>Danfoss Drives</b> , Graasten, Denmark	<b>EVGroup</b> , Schärding, Austria	<b>Leclanché Lithium GmbH</b> , Willstätt
<b>Arithmatica Limited</b> , Warwick, Great Britain	<b>Danfoss Silicon Power GmbH</b> , Schleswig	<b>FOS Messtechnik GmbH</b> , Schacht-Audorf	<b>Litef</b> , Freiburg
<b>ARC Seibersdorf Research GmbH</b> , Seibersdorf, Austria	<b>Datacon</b> , Radfeld/Tirol, Austria	<b>Fuba GmbH</b> , Gittelde	<b>Mair Elektronik GmbH</b> , Neufahrn
<b>ASE</b> , Seoul, Korea	<b>Degussa AG</b> , Hanau	<b>GE Healthcare</b> , Finland	<b>MED – EL</b> , Innsbruck, Austria
<b>Atmel Germany GmbH</b> , Heilbronn	<b>Diehl Avionik</b> , Überlingen	<b>GPS</b> , Stuttgart	<b>Miele &amp; Cie.</b> , Gütersloh
<b>Atotech Deutschland GmbH</b> , Berlin	<b>Diehl BGT Defense</b> , Nürnberg	<b>Hannusch Industrieelektronik</b> , Laichingen	<b>Motorola GmbH</b> , Flensburg
<b>Atral</b> , Crolles, France	<b>Dräger Systemtechnik</b> , Lübeck	<b>H. C. Starck</b> , Leverkusen	<b>MRT – Micro-Resist-Technology</b> , Berlin
<b>Audi AG</b> , Ingolstadt	<b>EADS Deutschland GmbH, Corporate Research</b> , München and Ulm	<b>Heidenhain</b> , Traunreut	<b>M+W Zander</b> , Stuttgart

Nokia Research Center, Nokia Group, Helsinki, Finland	Raisio Benecol Ltd, Raisio, Finland	SMA Regelsysteme GmbH, Niestetal	Trinamic, Hamburg
NU-Tech GmbH, Neumünster	Raytheon Anschütz GmbH, Kiel	Smart Material GmbH, Dresden	Tronox, Krefeld
NXP Semiconductors, Hamburg	Rehm Anlagenbau GmbH + Co. KG, Blaubeuren-Seissen	SMI GmbH, Itzehoe	Tronic's, Crolles, France
NXP Semiconductors, Nijmegen, Netherlands	Rena Sondermaschinen GmbH, Gütenbach	SMI, Milpitas, USA	Vectron International GmbH & Co. KG, Neckarbischofsheim
Omicron Laserage GmbH, Rodgau	Robert Bosch GmbH, Salzgitter	Smith Detection, Watford, Great Britain	Via Electronic GmbH, Hermsdorf
Osram Opto Semiconductors GmbH, Regensburg	SAES Getters S.p.A., Lainate/Milan, Italy	Smyczek, Verl	Virion-Serion-Institut, Würzburg
Oticon, A/S, Hellerup, Denmark	Scanbec Oy, Oulu, Finland	Sonion, Lyngby, Danmark	Vishay Beyschlag, Heide
PAV Card GmbH, Lütjensee	Scanbec GmbH, Halle	ST Microelectronics, Crolles, France	Vishay, Dimona and Holon, Israel
Peter Wolters AG, Rendsburg	SEF GmbH, Scharnebek	ST Microelectronics, Mailand, Italy	Vishay Siliconix Itzehoe GmbH, Itzehoe
PlanOptik AG, Elsoff	SensorDynamics (SD), Lebring, Austria	Still GmbH, Hamburg	Vishay Siliconix, Santa Clara, USA
Plasmon Data Systems Ltd, Rogston, Great Britain	Sensys Traffic AB, Upsala, Sweden	SÜSS Microtec AG, Garching	Vistec, Jena
Polytec GmbH, Waldbronn	Siemens Medical, München	Suunto, Vantaa, Finland	VTT Technical Research Centre of Finland, Espoo, Finland
Prettl Elektronik Lübeck GmbH, Lübeck	Siemens VDO Automotive AG, Schwalbach	Technolas, München	Wabco Fahrzeugbremsen, Hannover
Protec Process Systems GmbH, Siegen	Siemens VDO, Babenhausen and Karben	Technovision GmbH, Feldkirchen	
Qimonda AG, Neubiberg	SiP Technologies Oy, Espoo, Finland	Telefonica, Madrid, Spain	
		Thales Avionics, Valence, France	
		Thales, Paris, France	
		Treichel Elektronik GmbH, Springe	

## Innovation Catalogue

ISIT offers its customers various products and services already developed for market introduction. The following table presents a summary of the essential products and services. Beyond that the utilisation of patents and licences is included in the service.

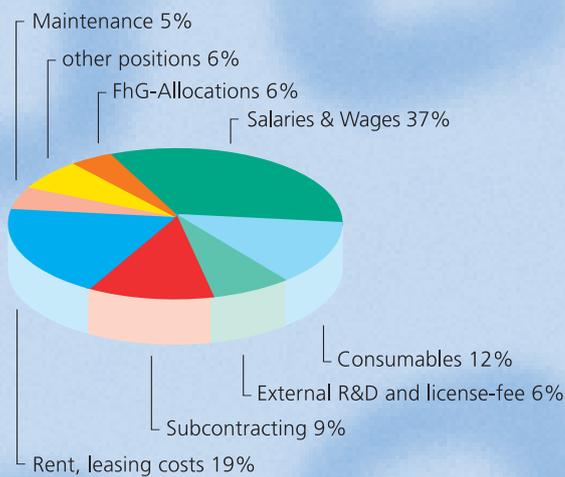
Product / Service	Market	Contact Person
Testing of semiconductor manufacturing equipment	Semiconductor equipment manufacturers	<b>Dr. Gerfried Zwicker</b> + 49 (0) 4821 / 17 - 4309 gerfried.zwicker@isit.fraunhofer.de
Chemical-mechanical polishing (CMP), planarization	Semiconductor device manufacturers	<b>Dr. Gerfried Zwicker</b> + 49 (0) 4821 / 17 - 4309 gerfried.zwicker@isit.fraunhofer.de
Wafer polishing, single and double side	Si substrates for device manufacturers	<b>Dr. Gerfried Zwicker</b> + 49 (0) 4821 / 17 - 4309 gerfried.zwicker@isit.fraunhofer.de
IC processes CMOS, PowerMOS, IGBTs	Semiconductor industry IC-users	<b>Detlef Friedrich</b> + 49 (0) 4821 / 17 - 4301 detlef.friedrich@isit.fraunhofer.de
Single processes and process module development	Semiconductor industry semiconductor equipment manufacturers	<b>Detlef Friedrich</b> + 49 (0) 4821 / 17 - 4301 detlef.friedrich@isit.fraunhofer.de
Customer specific processing	Semiconductor industry semiconductor equipment manufacturers	<b>Detlef Friedrich</b> + 49 (0) 4821 / 17 - 4301 detlef.friedrich@isit.fraunhofer.de
Microsystem Products	Electronic industry	<b>Dr. Ralf Dudde</b> + 49 (0) 4821 / 17 - 4212 ralf.dudde@isit.fraunhofer.de
Plasma diagnostics	Semiconductor equipment manufacturers	<b>Dr. Joachim Janes</b> + 49 (0) 4821 / 17 - 4601 joachim.janes@isit.fraunhofer.de
Etching and deposition process control	Semiconductor industry	<b>Dr. Joachim Janes</b> + 49 (0) 4821 / 17 - 4601 joachim.janes@isit.fraunhofer.de
Ion projection lithography open stencil mask technology and resist processes	Semiconductor industry	<b>Wolfgang Pilz</b> + 49 (0) 4821 / 17 - 4222 wolfgang.pilz@isit.fraunhofer.de
Inertial sensors	Motorvehicle technology, navigation systems, measurements	<b>Dr. Bernd Wagner</b> + 49 (0) 4821 / 17 - 4223 bernd.wagner@isit.fraunhofer.de
Thick epi poly MEMS processing	Sensors and actuators	<b>Dr. Peter Merz</b> + 49 (0) 4821 / 17 - 4513 peter.merz@isit.fraunhofer.de
Piezoelectric microsystems	Sensors and actuators	<b>Hans Joachim Quenzer</b> + 49 (0) 4821 / 17 - 4643 hans-joachim.quenzer@isit.fraunhofer.de
Microoptical scanners and projectors	Biomedical technology, optical measurement industry, telecommunication	<b>Ulrich Hofmann</b> + 49 (0) 4821 / 17 - 4553 ulrich.hofmann@isit.fraunhofer.de
Flow sensors	Automotive, fuel cells	<b>Dr. Peter Lange</b> + 49 (0) 4821 / 17 - 4220 peter.lange@isit.fraunhofer.de
Microoptical components	Optical measurement	<b>Dr. Klaus Reimer</b> + 49 (0) 4821 / 17 - 4506 klaus.reimer@isit.fraunhofer.de
Mastering and replication of micro structures in plastic	Microoptics, microfluidics	<b>Dr. Klaus Reimer</b> + 49 (0) 4821 / 17 - 4506 klaus.reimer@isit.fraunhofer.de

Product / Service	Market	Contact Person
Design and test of analogue and mixed-signal ASICs	Measurement, automatic control industry	<b>Jörg Eichholz</b> + 49 (0) 4821 / 17 - 4213 joerg.eichholz@isit.fraunhofer.de
Design Kits	MST foundries	<b>Jörg Eichholz</b> + 49 (0) 4821 / 17 - 4213 joerg.eichholz@isit.fraunhofer.de
RF-MEMS	Telecommunication	<b>Thomas Lisec</b> + 49 (0) 4821 / 17 - 4512 thomas.lisec@isit.fraunhofer.de
MST Design and behavioural modelling	Measurement, automatic control industry	<b>Jörg Eichholz</b> + 49 (0) 4821 / 17 - 4213 joerg.eichholz@isit.fraunhofer.de
Electrodeposition of microstructures	Surface micromachining	<b>Martin Witt</b> + 49 (0) 4821 / 17 - 4613 martin.witt@isit.fraunhofer.de
Digital micromirror devices	Communication technology	<b>Dr. Klaus Reimer</b> + 49 (0) 4821 / 17 - 4506 klaus.reimer@isit.fraunhofer.de
Electrical biochip technology (proteins, nucleic acids, haptens)	Biotechnology, related electronics microfluidics, environmental analysis, Si-Chipprocessing, packaging, chip loading	<b>Dr. Rainer Hintsche</b> + 49 (0) 4821 / 17 - 4221 rainer.hintsche@isit.fraunhofer.de
Secondary lithium batteries based on solid state ionic conductors	Mobile electronic equipment, medical applications, automotive smart cards, labels, tags	<b>Dr. Peter Gulde</b> + 49 (0) 4821 / 17 - 4307 peter.gulde@isit.fraunhofer.de
Battery test service, electrical parameters, climate impact, reliability, quality	Mobile electronic equipment medical applications, automotive, smart cards, labels, tags	<b>Dr. Peter Gulde</b> + 49 (0) 4821 / 17 - 4307 peter.gulde@isit.fraunhofer.de
Quality and reliability of electronic assemblies ( <a href="http://www.isit.fraunhofer.de">http://www.isit.fraunhofer.de</a> )	Microelectronic and power electronic industry	<b>Karin Pape</b> + 49 (0) 4821 / 17 - 4229 karin.pape@isit.fraunhofer.de
Material and damage analysis	Microelectronic and power electronic industry	<b>Dr. Thomas Ahrens</b> + 49 (0) 4821 / 17 - 4605 thomas.ahrens@isit.fraunhofer.de
Thermal measurement and simulation	Microelectronic and power electronic industry	<b>Dr. M. H. Poech</b> + 49 (0) 4821 / 17 - 4607 max.poech@isit.fraunhofer.de
Leadfree / RoHS transformation in electronic assembly	Electronic industry	<b>Dr. Thomas Ahrens</b> + 49 (0) 4821 / 17 - 4605 thomas.ahrens@isit.fraunhofer.de
Packaging for microsystems, sensors, multichip modules ( <a href="http://www.isit.fraunhofer.de">http://www.isit.fraunhofer.de</a> )	Microelectronic, sensoric and medical industry	<b>Karin Pape</b> + 49 (0) 4821 / 17 - 4229 karin.pape@isit.fraunhofer.de
Wafer level packaging, ultra thin Si packaging and direct chip attach using flip chip techniques	Microelectronic, sensoric and medical industry	<b>Wolfgang Reinert</b> + 49 (0) 4821 / 17 - 4617 wolfgang.reinert@isit.fraunhofer.de
Vacuum wafer bonding technology	Microelectronic, sensoric and medical industry	<b>Wolfgang Reinert</b> + 49 (0) 4821 / 17 - 4617 wolfgang.reinert@isit.fraunhofer.de

# Representative Figures

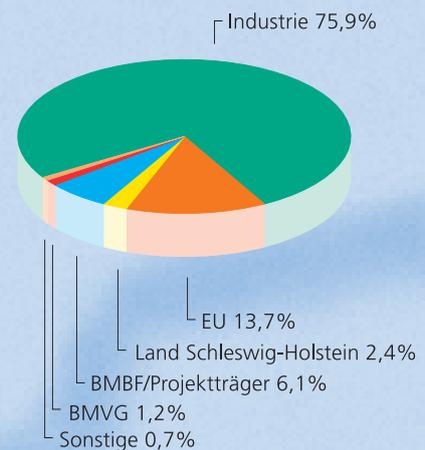
## Expenditure

In 2006 the operating expenditure of Fraunhofer ISIT amounted to 18.268,8 T€. Salaries and wages were 6.905,3 T€, material costs and different other running costs were 11.363,5 T€.



## Income

The budget was financed by proceeds of projects of industry/industrial federations/ small and medium sized companies amounting to 13.157,4 T€, of government/project sponsors/federal states amounting to 1.680,7 T€ and of European Union/others amounting to 2.498,2 T€.

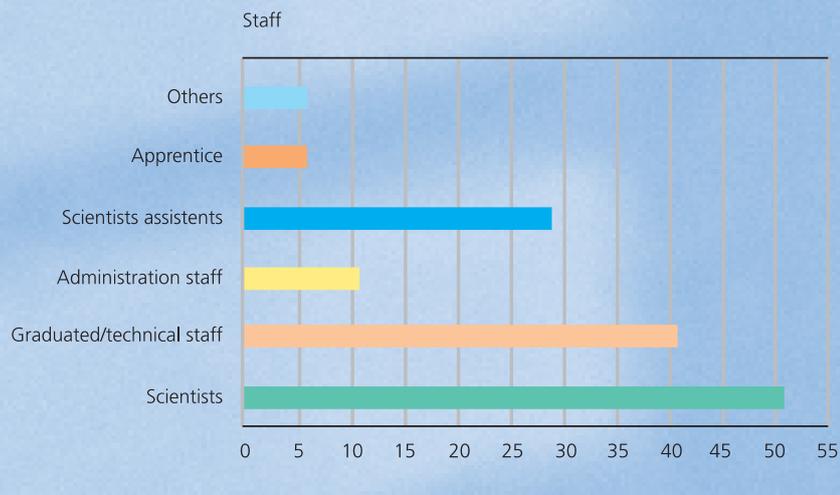
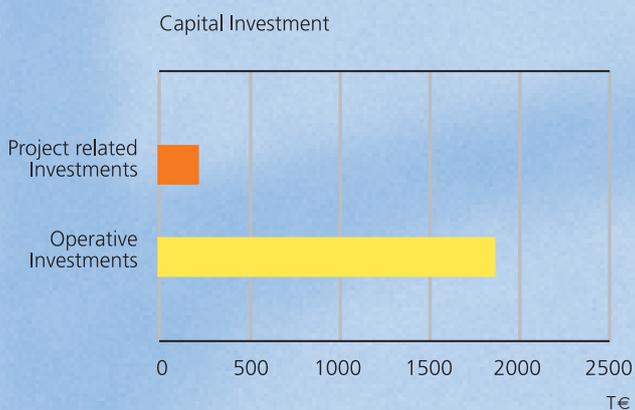


## Capital Investment

In 2006 the institutional budget of capital investment was 2.118,3 T€. The amount of operating investment was 1.874,2 T€ and project related investments were amounted to 244,1 T€.

## Staff Development

In 2006, on annual average the staff consisted of 103 employees. 51 were employed as scientific personnel, 41 as graduated/technical personnel and 11 worked within organisation and administration. The employees were assisted through 29 scientific assistants, 6 apprentices and 6 others.



# The Fraunhofer-Gesellschaft at a Glance

## The Fraunhofer-Gesellschaft

Research of practical utility lies at the heart of all activities pursued by the Fraunhofer-Gesellschaft. Founded in 1949, the research organization undertakes applied research that drives economic development and serves the wider benefit of society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration. The organization also accepts commissions from German federal and Länder ministries and government departments to participate in future-oriented research projects with the aim of finding innovative solutions to issues concerning the industrial economy and society in general.

Applied research has a knock-on effect that extends beyond the direct benefits perceived by

the customer: Through their research and development work, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. They do so by promoting innovation, accelerating technological progress, improving the acceptance of new technologies, and not least by disseminating their knowledge and helping to train the urgently needed future generation of scientists and engineers.

As an employer, the Fraunhofer-Gesellschaft offers its staff the opportunity to develop the professional and personal skills that will allow them to take up positions of responsibility within their institute, in other scientific domains, in industry and in society. Students working at the Fraunhofer Institutes have excellent prospects of starting and developing a career in industry by virtue of the practical training and experience they have acquired.

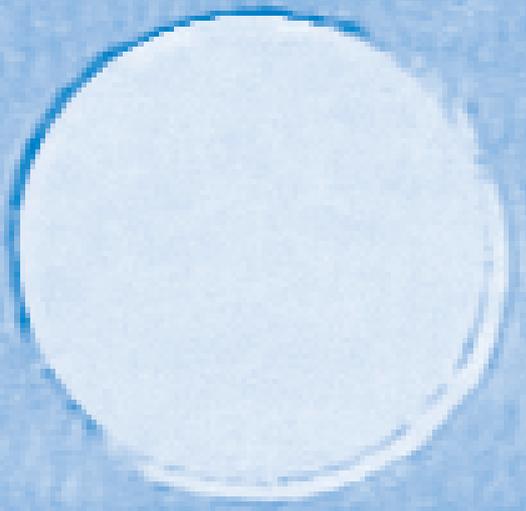
## Locations of the Research Establishment



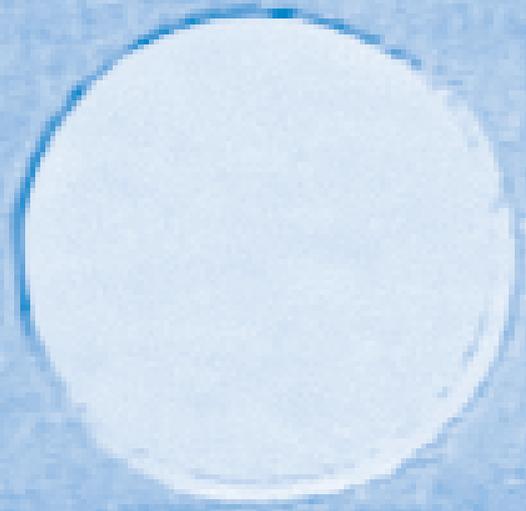
At present, the Fraunhofer-Gesellschaft maintains more than 80 research units, including 56 Fraunhofer Institutes, at 40 different locations in Germany. The majority of the 12,500 staff are qualified scientists and engineers, who work with an annual research budget of €1.2 billion. Of this sum, more than €1 billion is generated through contract research. Two thirds of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. Only one third is contributed by the German federal and Länder governments in the form of institutional funding, enabling the institutes to work ahead on solutions to problems that will not become acutely relevant to industry and society until five or ten years from now.

Affiliated research centers and representative offices in Europe, the USA and Asia provide contact with the regions of greatest importance to present and future scientific progress and economic development.

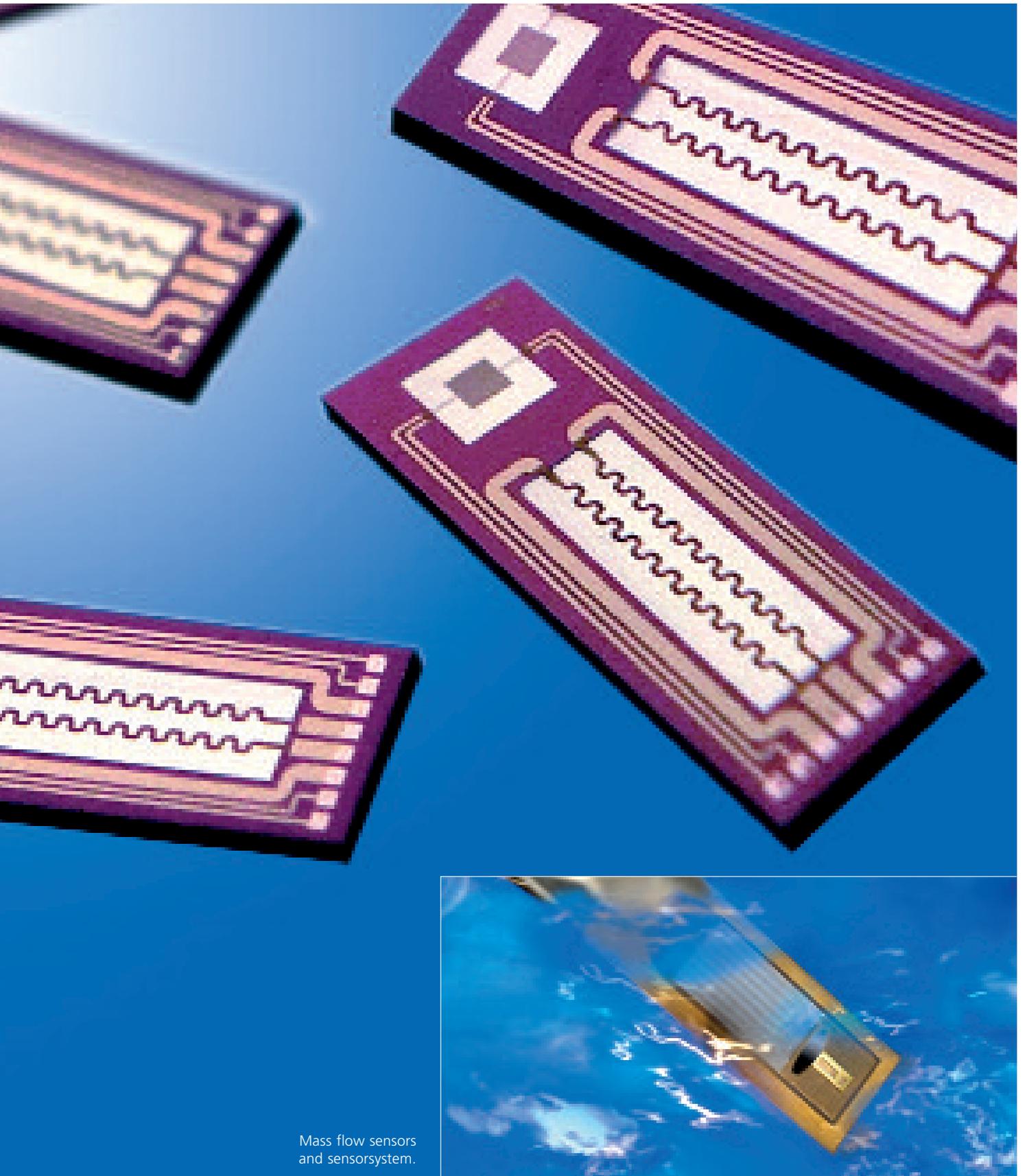
The Fraunhofer-Gesellschaft is a recognized non-profit organization which takes its name from Joseph von Fraunhofer (1787-1826), the illustrious Munich researcher, inventor and entrepreneur.



Representative  
Results of Work



# Representative Results of Work Microsystems Technology



Mass flow sensors  
and sensorsystem.

## Mass Flow Sensor for Measurement of Liquids (Water)

### Preface

A water flow sensor was developed for a public water supply company in Tuscany/Italy. This company was asking for a sensor for water flow monitoring which is cheap, accurate and easy to replace/insert into a running system. Commercial available flow sensors are generally expensive, cumbersome and sometime invasive.

A flow sensor for fluids in MEMS technology draws multiple benefits like:

- Low cost – large scale production can lead down the costs of the sensing equipment.
- Easy Replacement – very small devices can be built.

The field of potential applications is large: process control, chemical industries, fuel distribution, water monitoring or metering and more.

### Introduction

The well known principle of hot wire anemometry in air has been applied to mass flow measurements in fluids. The working principle in fluid is essentially the same as in air and shall be discussed

briefly as follows. The primary sensor of this measurement tool is a heated wire that is exposed in a flow. A second sensor is used to measure the ambient (fluid) temperature. As the fluid passes over the hot wire, it carries away heat. The heat loss depends on the mass flow rate, the heat capacity of the fluid, and the temperature difference between the wire and the fluid. Since the heat capacity of the fluid is known and the temperatures are monitored in real-time, the mass flow rate can be determined from the heat loss (related to the electrical resistance of the wire via the Ohm's law) and the temperature coefficient of the wire. The wire resistance  $R_w$  is a function of temperature according to

$$R_w = R_0 [1 + \alpha (T_w - T_{ref})]$$

with  $R_0$ , the heater resistance at reference temperature  $T_{ref}$  (ambient). In an operation in a constant temperature mode the temperature of the heated wire ( $T_w$ ) relative to the ambient temperature ( $T_{ref}$ ) is kept constant by a Wheatstone bridge. The current  $I$  (or voltage  $U$ ) which is needed therefore, is proportional to the mass

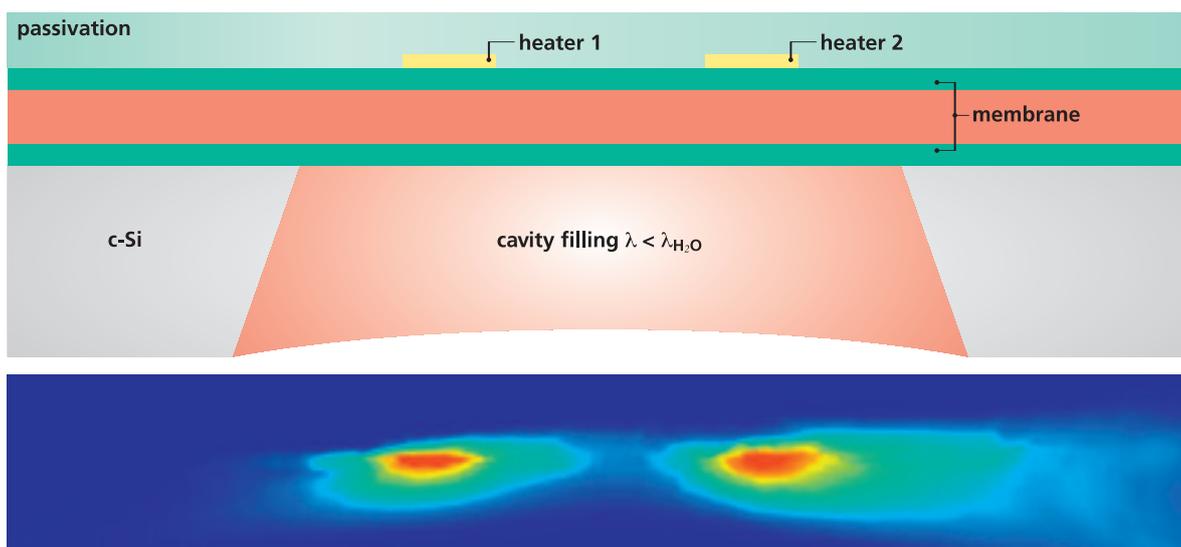


Figure 1: Visualization of fluid flow over the two heaters located on the membrane of the MEMS sensor (bottom, © COMSOL MULTIPHYSICS). In the upper part of the figure a schematic cross-section of the flow sensor is given.  $\lambda$  is an acronym for the heat conduction of the materials, c-Si is indicating the crystalline silicon substrate, in which the cavity is etched.

# Representative Results of Work Microsystems Technology

flow. However, there are deviations from a linear dependence according to the “Kings Law”. The King’s law takes account for the different contributions to the heat transfer through the boundary layer by convection and conduction with flow and is empirically described as

$$I^2 R_w^2 = U^2 = (T_w - T_{ref})(A + B \cdot v^n)$$

The voltage drop (U) is used as a measure of velocity (v). The constants A, B and the exponent n are empirically determined and ambient specific. This nonlinearity must be compensated by a special signal conditioning. For the measurement of the direction of a flow the heating resistors are arranged twice on a chip in a way that they are adjoined closely in parallel. The fluid picks up heat at the first resistor and transfers this to the second resistor. This is shown in the visualization of the flow in figure 1. The results are different cooling effects on the two resistors. This difference can be taken for the measurement of directionality.

## Technology

The thin wires are deposited on a thin membrane, which is a stack of three layers – Siliconnitride, Silicodioxide and Siliconnitride. These layers are formed in LPCVD (Low Pressure Chemical Vapour Deposition) processes, which generate highly stoichiometric layers without

contaminants and high long-time reliability. The membrane is formed by anisotropic KOH etching and shows only slightly tensile stress, which results in high mechanical stability. Beyond this the membrane enables a high thermal isolation of the heated wires to the chip edges. The membrane with the wires is subsequently covered with a Siliconnitride layer formed in a Plasma Enhanced CVD process. This final passivation is known to be inert against most environmental detrimental effects and is also biocompatible. For the application in water the backside cavity is filled with a flexible organic material with a significant lower heat conduction as water. This assures an explicit signal from the front side, and prevents uncontrolled fluctuations on the backside. In addition an enhanced stability against water pressure is achieved. The resistors are made of Titanium and completely covered with a nanolayer of Titaniumnitride to eliminate any reaction of Titanium with adjacent media. The Ti/TiN layer show no drift due to electrical or temperature stress. Production of this chip is done in a Standard MOS – line. Thus it can be manufactured in quantity with guaranteed uniformity, a factor that is critically important to manufacturers. A schematic cross-section of the device is given in the top of figure 1.

## Application

Hot wire or hot film anemometry is known since nearly 100 years. The first paper was published by L.V. King in 1914. This technique was used mainly for measuring the velocity of gases, particularly turbulent fluctuations in pipes. It has proved less successful in liquids because of bubbles and deposits, which disturb the signal. Converting the “old” wire or film technology into state of the art MEMS technology opens new promising possibilities. However, for the measurements in water two major problems appear. Firstly, the generation of bubbles by heated wires and their sticking on the surface of the sensor is disturbing the heat transfer from the wire to the fluid. In addition this effect is enforced by the concomitant deposition of  $\text{CaCO}_3$  by the reaction

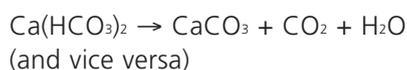


Figure 2: Prototype of the water flow sensor system containing a ceramic substrate with the sensor.

Secondly, the right choice of assembly for the electrical contacts is very important with respect to leakage current and corrosion problems. The first challenge could be solved by employing pulsed voltage technique in conjunction with reduced overtemperature (compared to air). Due to the extremely thin membran technology (2  $\mu\text{m}$  thickness including a passivation layer) the response times are reasonable short, even in water; this prevents significant heating of the device and ambient. Also, the right choice of a passivation layer results in a better protection against deposits. A water resistant coating including a proper adhesion on the underlayer of all bonds and wires assures long time reliability.

A first prototype has been developed and is shown in figure 2. A steel pipe is equipped with a sensor head, which is inserted into water, parallel to the flow and fulfills the following requirements:

- Contact robustness
- No water infiltrations through the board
- Easy connection to the pipe
- Smooth pipe profile.

These devices are tested with respect to:

- resistance against pressure,
- pollution of the surface,
- corrosion of electrical contacts and
- drift in resistance.

For measurements an evaluation board with an Intelligent Sensor InterFace (ISIF) developed by SensorDynamics for generic sensor conditioning has been used. ISIF is a complex mixed-signal IC featuring digital and analog inputs. The chip is based on the LEON core: a 32-bit RISC processor and a set of memories, buses and peripherals for external communication. The analog section comprises filters, amplifiers, regulators DACs and ADCs for sensor driving and conditioning. Testing was performed in a test environment at ISIT and more extensive at a real site in a water supply station in Tuscany/Italy. The results of a three month continuous testing including an accelerated testing show very promising results, particularly with respect to very little pollution of the sensor surface.

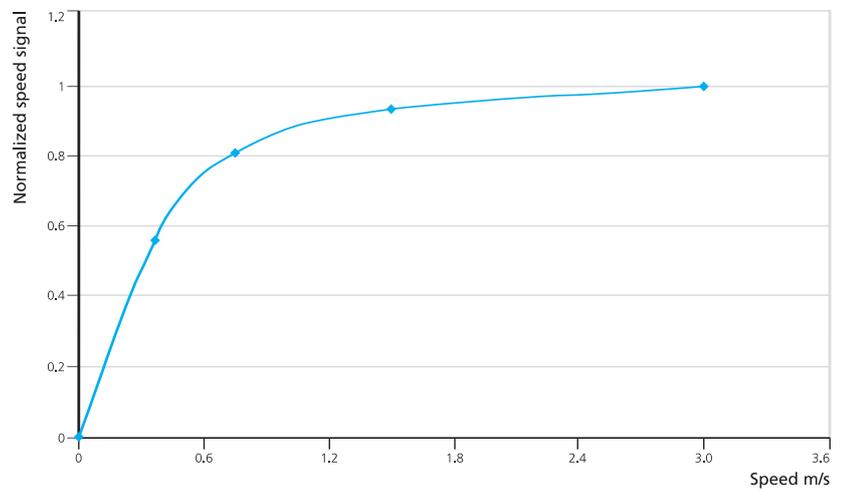


Figure 3: Normalized response signal to water flow.

A typical response of the signal to water flow is shown in figure 3. Currently the next 100 complete systems including a new sensorhead which is more smooth and easier to mount are fabricated. The assembly is in a steel pipe, which contains batteries for power supply and a specially designed ASIC for signal evaluation on top inside the pipe. Via an USB connector the signal can be read out using a simple Laptop. This will be replaced later on by wireless RF technique. Testing will be performed for 6 month in Tuscany in comparison to a commercial magnetic flow meter.

The main properties of this new sensor are summarized as follows:

- Clear direction detection
- In measurement range (0 cm/s to 230 cm/s) the resolution is in the range of  $\pm 0.75$  cm/s to  $\pm 4$  cm/s (worst-case) that is  $\pm 0.35\%$  up to  $\pm 1.76\%$  respect to the full scale
- Repeatability roughly  $\pm 1\%$  respect to the full scale
- Current consumption of about 9 mA for typical applications

The current consumption in collaboration with a proper pulse technique guarantees a lifetime clearly above one year.

After these tests have been successfully completed a mass production in collaboration with SensorDynamics in the range of 50 000 to 500 000 dies per year is planned.

# Representative Results of Work Microsystems Technology

## Waferlevel Packaged MOEMS

### Introduction

Microscanning mirrors attract increasing interest for numerous applications, such as mobile and automotive laser projection, medical imaging, laser writing and measurement technology. Mainly used to deflect laser light beams, such silicon manufactured MOEMS (**M**icro **O**ptical **E**lectro **M**echanical **S**ystems) devices combine the advantage of small size, high functionality and low cost mass producibility.

The torsionally suspended mirror plate can be actuated by various driving principles, like thermo-mechanical, magnetic, piezoelectric and electrostatic forces. Due to low power consumption and high achievable scan frequencies Fraunhofer ISIT develops for more than twelve years electrostatically driven scanning micromirrors.

While such MOEMS developments are undertaken worldwide, Fraunhofer ISIT is the first to provide a complete process technology not only for the manufacturing of microscanning mirrors but also for a suitable hermetic waferlevel package.

This waferlevel package is essential for mass producibility and high yield since the fragile actuator structures need to be protected against harsh environmental influences directly after the release process. Especially during dicing the wafers into separate chips protection against contamination with particles and fluids is necessary.

While for microsensors such packaging processes are state of the art, MOEMS packaging is more difficult due to not only mechanical but also optical functionality of the package.

High resolution laser projection (e.g. HDTV) requires large mirror deflections, therefore an optical package must incorporate deep cavities with depths up to 500  $\mu\text{m}$ . The mirror deflection is largely influenced and limited by viscous gas damping. For that reason mirror actuation in vacuum enables large deflection angles and low driving voltages even at highest scan frequencies exceeding 100 kHz.

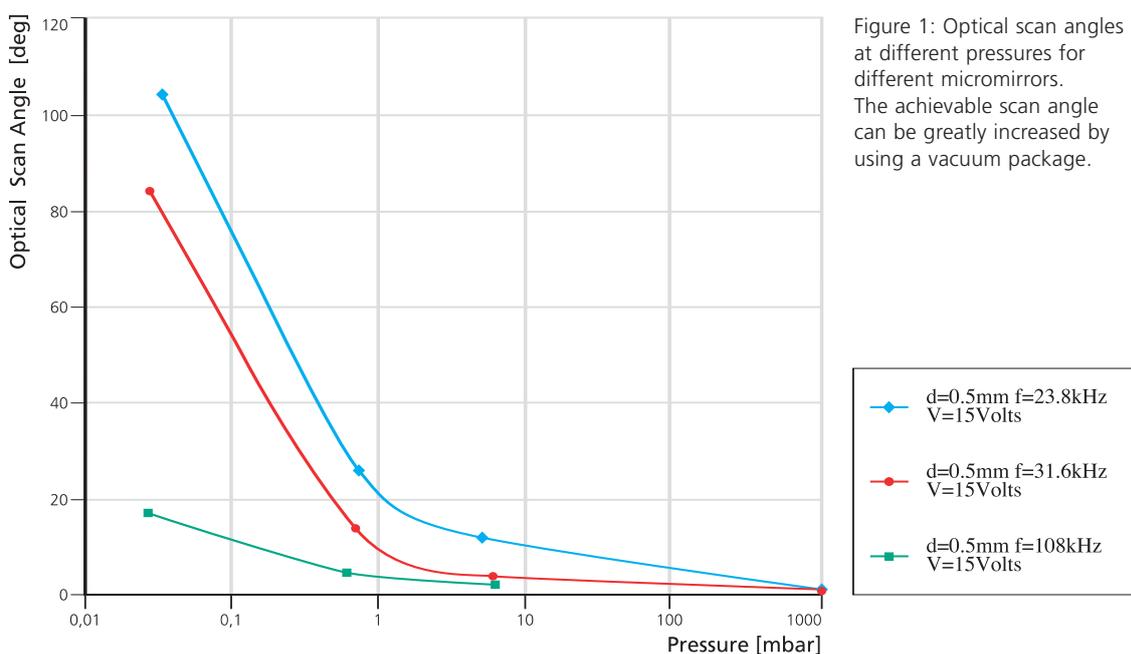


Figure 1: Optical scan angles at different pressures for different micromirrors. The achievable scan angle can be greatly increased by using a vacuum package.

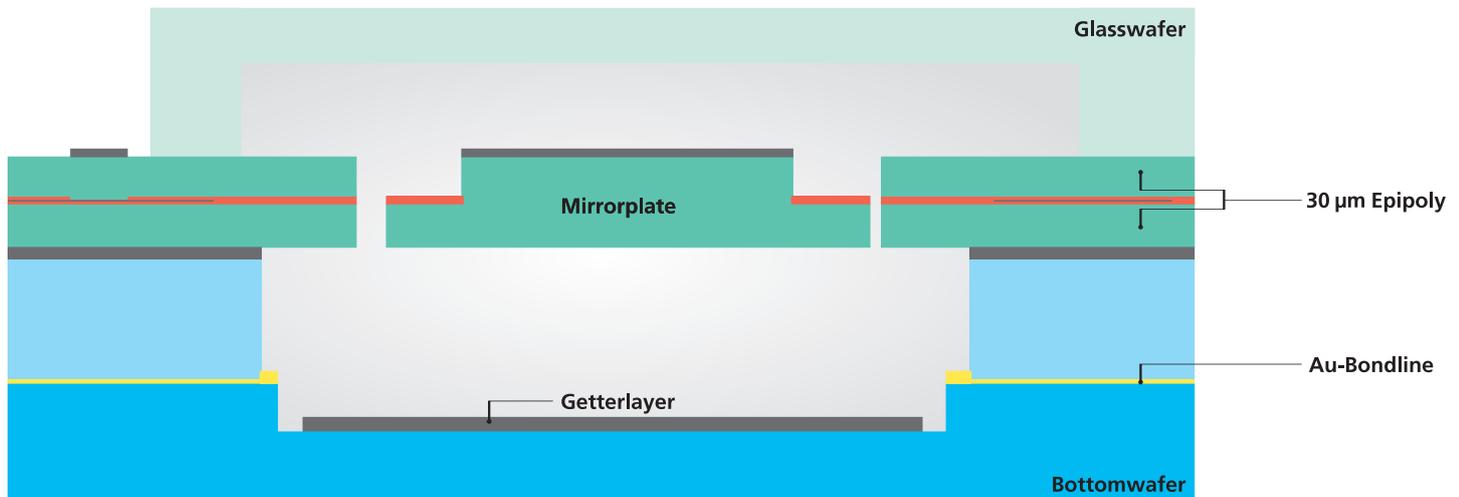


Figure 2: Schematic of a vacuum packaged micromirror. An optional getter layer enhances the achievable vacuum level.

### Process

The manufacturing process of the wafer containing the active mirror structures is based on two 30 microns thick vertically isolated polysilicon layers. DRIE etching of front and backside realizes structures with different thicknesses. By this, it is possible to design suspension beams and comb-drives with thicknesses of either 30 or 60 microns while the mirror plate consists of 60 µm thick poly silicon without any stress-inducing intermediate layer (e.g. oxides).

Lateral feedthroughs enable different potentials inside the cavity for sensing and actuation without loss of hermeticity. The polished flat surfaces on the front and backside of the wafer allow standard wafer bonding processes, such as anodic and eutectic bonding.

To realize a hermetic package on wafer level, an anodically bonded glass wafer seals the frontside of the mirror wafer, while a eutectically bonded silicon wafer seals the stack at the backside.

The manufacturing of glass wafers with the needed deep cavities is quite a big challenge due to a lack of adequate methods for structuring glass. While former work mainly used silicon spacer wafers bonded with unstructured glass wafers to form cavities, Fraunhofer ISIT developed a proprietary method for structuring glass wafers with

perfect optical quality. It depends on casting a silicon wafer mold, i.e. a structured silicon wafer is bonded with a glass wafer and subsequently heated above the glass softening temperature. A following wet etch process releases the structured glass wafer.

### Results

Tested micromirrors manufactured with the new technology showed excellent mechanical and optical properties:

- Resonance frequencies of up to 108 kHz
- Optical deflection angles of up to 100°
- Mirror flatness: radius of curvature > 18 m



Figure 3: The application range for scanning micromirrors is vast. A virtual keyboard is only one amongst many others.

# Representative Results of Work Microsystems Technology

## Applications of Sputtered Piezoelectric Thin Films

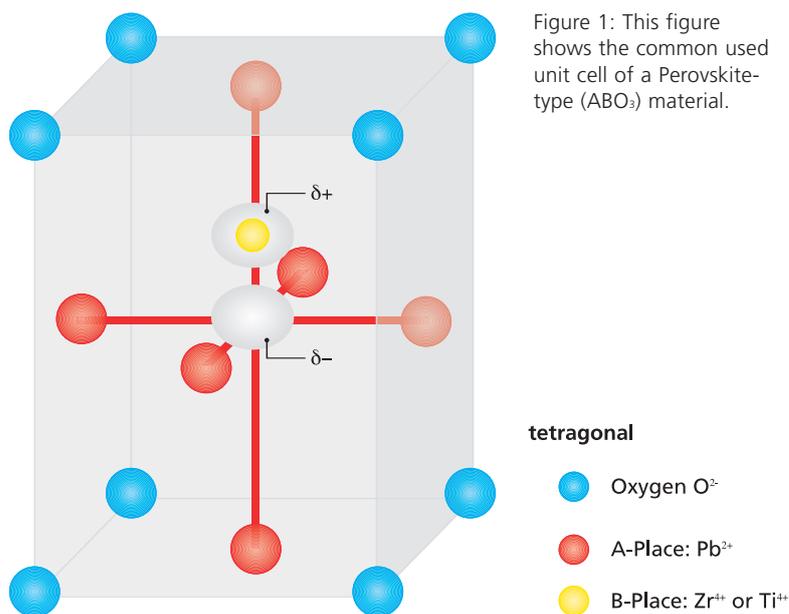
In general, the Microsystem Technology can be divided into two areas, sensor systems, for capturing data from the environment, and actuators which are influencing the environment. The background of each sensor or actuator is a physical sensing and acting principle, respectively.

In the majority of actuators masses need to be moved, thus principles which are generating forces need to be integrated in the MEMS. Due to the small dimensions and the so called scaling law three force-principles are widely accepted: electrostatics, thermal drives and electromagnetic drives. For an increasing number of applications these physical principles for the generation of forces become more and more insufficient, because either higher forces (as in the case of the electrostatic) or higher velocities (as in the case of thermal drives) are necessary. Because of the combination of short response times and comparatively high forces, the piezoelectric effect, observed in many ceramics, seems to be the most promising candidate to close this open gap.

In the field of micro-sensors the need of a piezoelectric layer is less obvious. Commonly used sensing methods, e.g. the shift of a capacity or the piezo-resistive effect, are well established in several applications. Nevertheless, there are some niches where the direct piezoelectric effect has advantages: AFM tips for memory applications, Bulk Acoustic Waves (BAW) for modern wireless communication, microphones, and resonant pressure-sensors. The charm of a piezoelectric material within the above mentioned sensors is the direct coupling between electrical- and mechanical values.

In mainstream MEMS technology, materials are restricted to those used in microelectronics in order to profit from materials and processes that are readily available. In addition, the same fabrication facilities are often used for both MEMS and microelectronics, but do not allow an application of materials with fast diffusing ions. However, in order to cover the whole range of physical phenomena that are exploitable for sensors and actuators, as described, it is necessary to add a variety of functional materials to the existing base materials. An important family of functional materials are polar materials. Their piezoelectricity can be used in sensors and actuators. Their pyroelectricity is employed in infrared detectors. In this article emphasis is given to aluminium-nitride (AlN) and lead zirconate titanate (PZT, see figure 1), a solid solution of ferroelectric  $\text{PbTiO}_3$  and anti-ferroelectric  $\text{PbZrO}_3$ . AlN is sputtered in a commercial magnetron sputtering tool from Oerlikon, Switzerland and the PZT thin films are developed within a bilateral R&D project in cooperation with Fraunhofer IST, Braunschweig, funded by the state of Schleswig-Holstein (see annual report 2004).

In most of the structures applied in MEMS, the piezoelectric film is part of a composite structure, i.e. the piezoelectric film is clamped to another elastic substrate. A rigorous treatment of this problem requires the solution of the equations of state with two piezoelectric and several elastic coefficients. The latter are, however, usually not



known precisely. Following the approach of P. Muralt, EPFL, effective piezoelectric coefficients of films clamped to a rigid substrate are introduced.  $d_{33,f}$  describes the thickness change as a function of the applied field, i.e. the longitudinal effect;  $e_{31,f}$  the in-plane stress as a function of the applied field, i.e. the transverse effect. The film is clamped in the film plane (coordinates 1, 2). In the offplane direction (coordinate 3), the film is free to move (figure 2). This corresponds to a mixed boundary condition. The directly measured piezoelectric coefficients of thin films on substrates are therefore functions of standard piezoelectric coefficients and elastic constants. These effective coefficients are related to the ordinary coefficients by the following relations:

$$e_{31,f} = \frac{d_{31}}{s_{11}^E + s_{12}^E} = e_{31} - \frac{c_{13}^E}{c_{33}^E} e_{33}$$

$$d_{33,f} = \frac{e_{33}}{c_{33}^E} = d_{33} - \frac{2s_{13}^E}{s_{11}^E + s_{12}^E} d_{31}$$

Most of the potential applications are based on

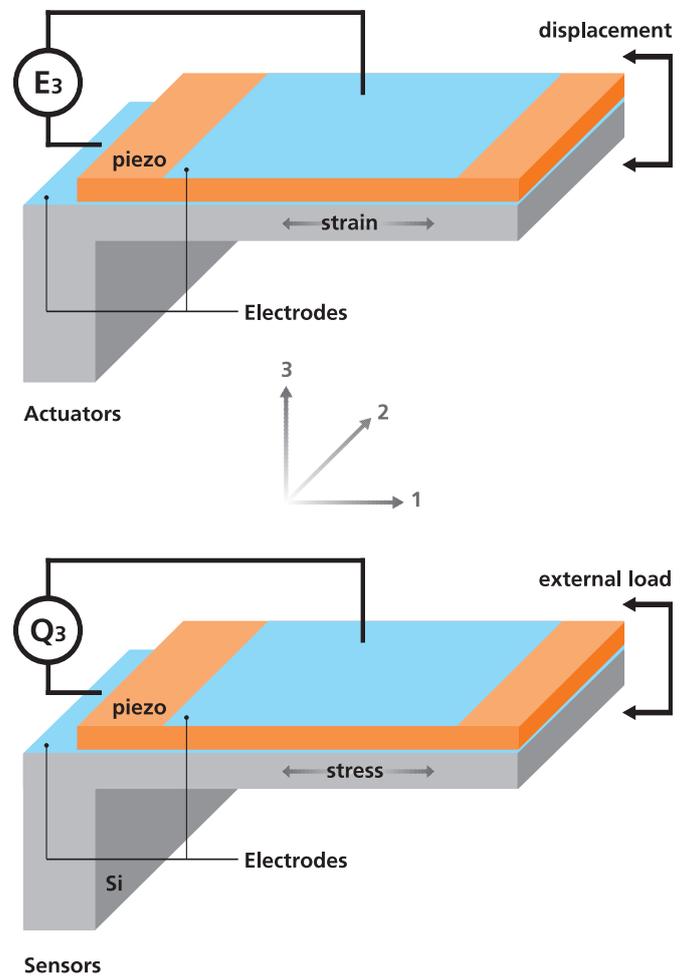


Figure 2: Schematic description of the geometry and the working principle of the piezoelectric film applied in actuators (input:  $E_3$ , output: displacement) and in sensors (input: external load, output charge:  $Q_3$ ).

Coefficients/ figures of merit	Unit	ZnO	AlN	PZT
$e_{31,f}$	[Cm <sup>-2</sup> ]	-1,0	-1,05	-8 ... -12
$d_{33,f}$	[pmV <sup>-1</sup> ]	5,9	3,9	60 ... 130
$\epsilon_{33}$	1	10,9	10,5	300 ... 1300
$e_{31,f}/\epsilon_0\epsilon_{33}$	[GVm <sup>-1</sup> ]	-10,3	-11,3	-0,7 ... -1,8
$e_{31,f}^2/\epsilon_0\epsilon_{33}$	[GPa]	10,3	11,9	6 ... 18
tan $\delta$	1	0,01 ... 0,1	0,003	0,01 ... 0,03
$e_{31,f}^2/\sqrt{\epsilon_0\epsilon_{33}\tan\delta}$	[10 <sup>1</sup> Pa <sup>1/2</sup> ]	3 ... 10	20	4 ... 8
$c_{33}^E$	[GPa]	208	395	85 ... 100
$d_{33,f} \cdot c_{33}^E/\epsilon_0\epsilon_{33}$	%	7,4	6,5	7 ... 15

Table 1: Thin film piezoelectric and dielectric properties.

# Representative Results of Work Microsystems Technology

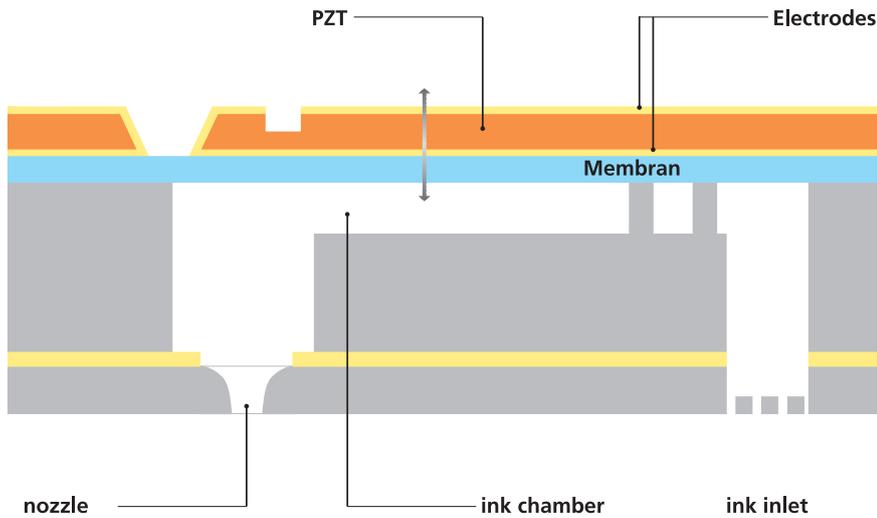


Figure 3: Schematic cross section of a piezoelectric driven ink-jet head.

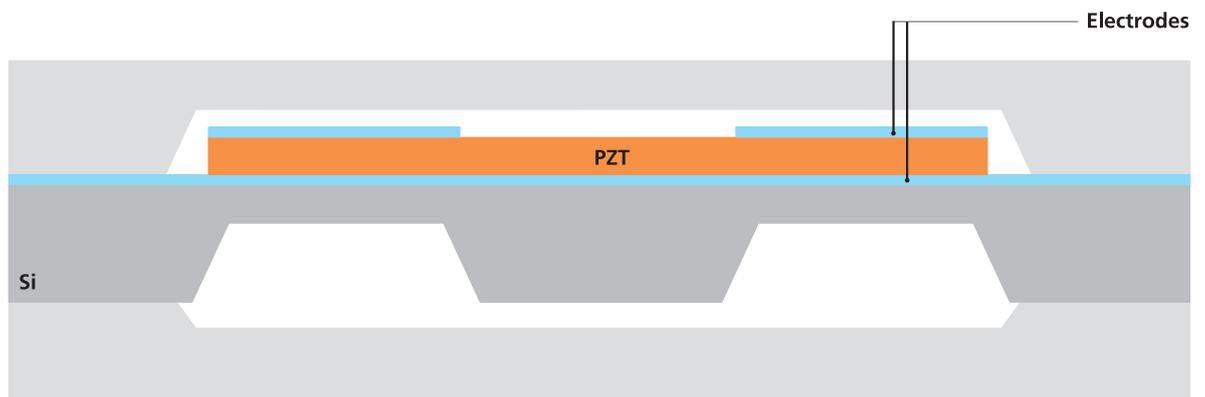
the transverse coefficient  $e_{31,f}$ . Bending of beams and deflections of membranes are much more suited principles for obtaining large responses or large excursions. In terms of piezoelectric coefficients, PZT is clearly the leader among the above materials. This translates into a superior performance in force, torque, and output power of actuators and motors, and also of sensors with current detection.

However, when voltages are detected, when the dielectric noise current limits the signal-to-noise ratio, and when the coupling coefficient is important (power consumption, power yield and transducer response), the dielectric constant and

the dielectric losses also have to be considered. In these cases, PZT is no longer so brilliant because of its high dielectric constant. AlN and ZnO are more suited for voltage detection (see table 1).

Due to the relations from table 1 a general trend within the field of piezoelectric MEMS can be observed. PZT with its high piezoelectric coefficients  $d_{33,f}$  and  $e_{31,f}$  is becoming more and more the choice of material for fabricating powerful actuators where high forces are required, e.g. ink-jet head (figure 3). Another interesting application for PZT is energy harvesting (figure 4) where the mechanical input power is not the limiting value. AlN with its good signal to noise

Figure 4: A possible design of a micro energy harvester for energy autonomous MEMS.



ratio is chosen rather than PZT, if the considered application is a sensor or even a resonant system like bulk acoustic wave resonators (BAW).

The nozzle of an ink-jet head (figure 3) as well as the energy harvester (figure 4) is basically micro-mechanical membrane-structures. Thus, it is self-evident that the first test structure to demonstrate the functionality of the PZT-layers and to gain experiences is also a membrane-like actuator. The membranes are fabricated using bulk-micromachining. Several process steps are necessary, before etching the membrane by KOH/TMAH and dicing the wafer by sawing. Starting with a diffusion barrier (500 nm SiO<sub>2</sub>, 150 nm Si<sub>3</sub>N<sub>4</sub>, 100 nm HTO), and avoiding the interaction between lead and silicon, a suited bottom electrode (20 nm Ti, 80 nm Pt) is evaporated. The 4 μm to 10 μm thick functional PZT-layer is sputtered by a high rate process called Gas-Flow-Sputtering (GFS). To end up with a capacitor-like structure the Au-top electrode is deposited by electroplating. A SEM picture of the

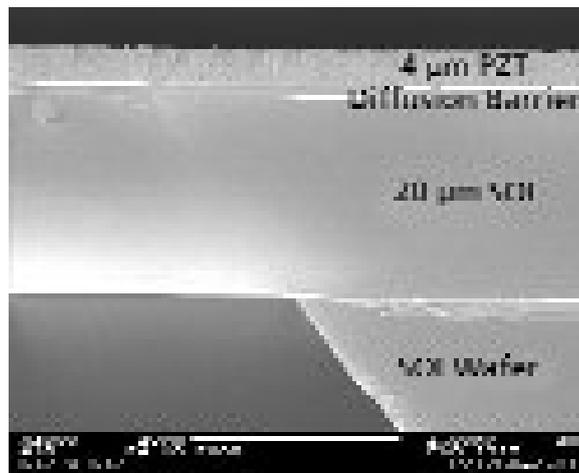


Figure 5: REM picture of the cross section of a Si-PZT-membrane-actuator.

final membrane is shown in figure 5.

The electrodes of the membrane-actuator are connected to a DC voltage (0 V – 50 V) and the static deflection is measured by a white-light-interferometer. With this setup, the function  $z = f(U)$  has been measured, where  $z$  is the deflection in the centre of the membrane (see figure 6).

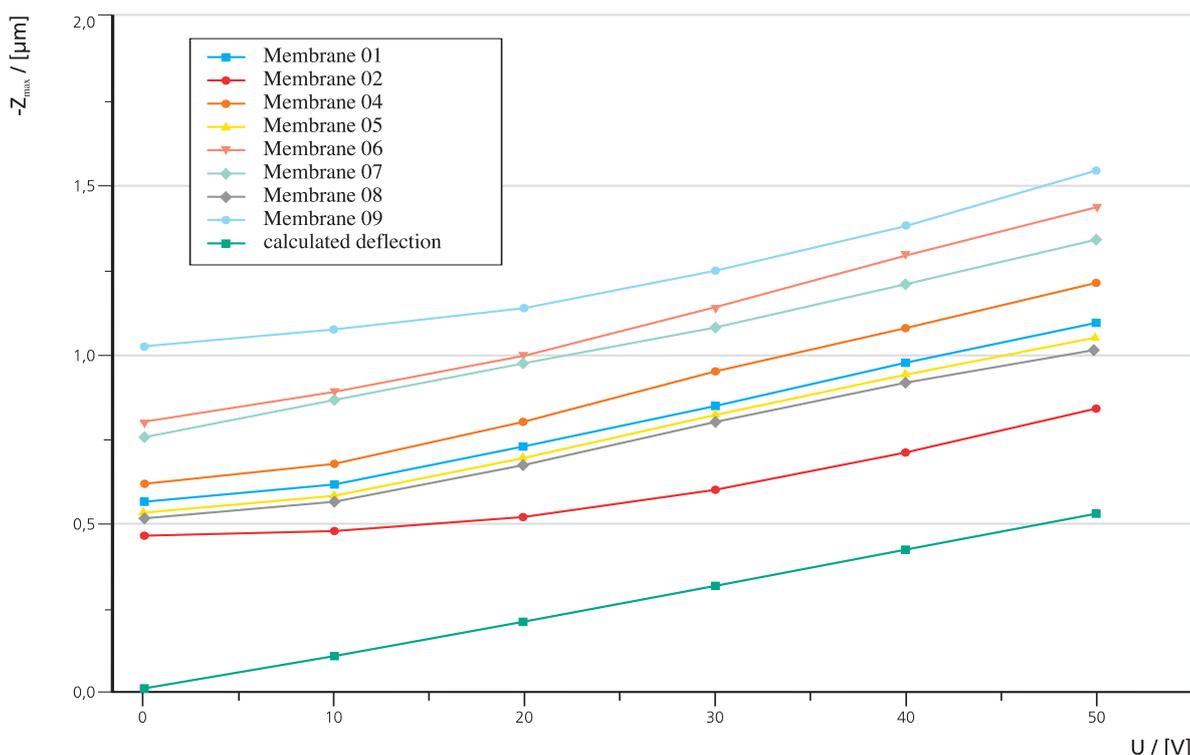


Figure 6: The calculated and the measured static deflection  $z = f(U)$  of membrane-actuators.

# Representative Results of Work Microsystems Technology

## Development of a Crystal Silicon Force/Torque Sensor

Robots are important tools in the field of automation in European industry. Most robots can be found in work areas where very heavy or dangerous work under unhealthy conditions with high precision at high repetition is necessary. Typical works are welding of large steel elements or spraying of color to large surfaces. Conditions are likely very loud, there is the danger of heavy stuff falling, and the air is full of toxic gases. These tasks under the same conditions has to be done in small and medium sized enterprises (SME) too, but the European manufacturing SMEs are characterised by high-quality production in relatively small series. Here no robots are used, the work has to be done by human workers. The reason for the missing of robots are manifold:

- Robots are too unflexible for being useful in small series.
- Robots are very heavy, i.e. it very difficult to move them to different work places.
- Robots can't share the work space with a worker, the work space of robots is protected by fences.
- Robots are too expensive for the potential benefit.

SMErobot™ (public webpage [www.smerobot.org](http://www.smerobot.org)) is an European integrated project (IP) in the 6th framework, started on 1st March 2005 with a duration of four years. The research and development in SMErobot™ is geared towards creating the following technical innovations:

- robot capable of understanding human-like instructions (by voice, gesture, graphics)
- safe and productive human-aware space-sharing robot (cooperative, no fences)
- three-day-deployable integrated robot system (modular plug-and-produce components)

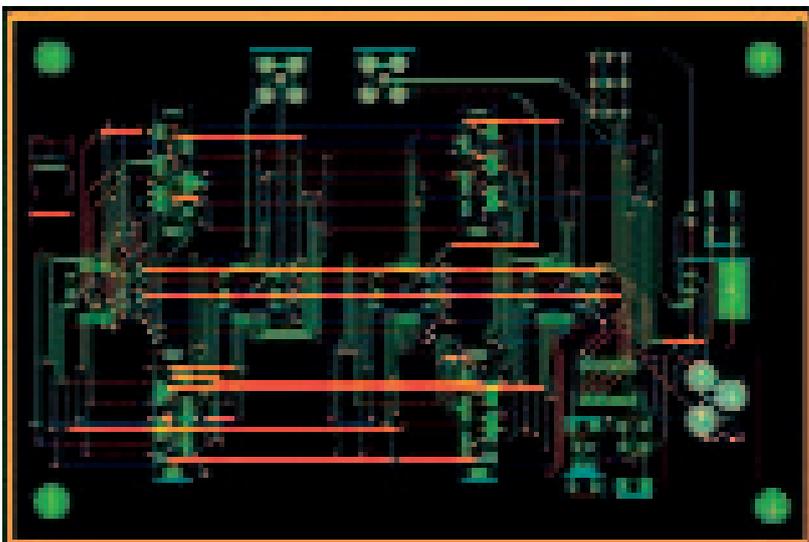
ISIT is involved in the field of force/torque sensors made of silicon that will be used to monitor the emerging forces and torques so that the sensors can be used to make robots much more safe by introducing control functions so that they can share the work space with workers. The use of such sensors is clearly not limited to this purpose. Today's available commercial force/torque sensors (F/T-sensor) cost several thousand Euro so they are only rarely used in robotics. So the main target is to provide cheap F/T-sensors, which cost far below 1000 Euro.

To measure forces typically strain-gauges are used. Here the electrical resistance is changed by the deformation due to the applied force. Normally metals are used, here the effect of the change of resistivity is a pure geometrical one. Stretching a long and small metal stripe makes the resistor even longer and smaller and increases the resistance.

It was decided to take crystal silicon for force sensing: the effect  $K = \Delta R / \Delta l$  is up to factor 50 higher than in metals due crystal lattice effects, it is known as the piezo-resistive effect. The main specifications are:

- Max Measurement Force/Torque:  
80 N / 25 Nm
- Max Overload Force/Torque:  
300 N / 900 Nm
- Resolution <0.3 N / <0.1 Nm
- Linearity Error <5 %

Figure 1:  
PCB for electronic.



Force/Torque	F <sub>x</sub> =10N	F <sub>y</sub> =10N	F <sub>z</sub> =10N	M <sub>x</sub> =0.5Nm	M <sub>y</sub> =0.5Nm	M <sub>z</sub> =0.5Nm	Δ T=100K
Resistivity change [%]	6.0	6.0	6.4	6.8	6.8	5.9	2.8
Stress at piezo [MPa]	80	80	85	67	67	166	42

Table 1:  
FEM-simulation values.

To show the feasibility of the concept it was decided to start with a low force version of the F/T-sensor with maximum measurement range 10 N / 0.5 Nm.

A FEM model of the sensor was built up and a design was found, which showed in the simulations an isotropic response, i.e. the resistivity change for each of the 6 degrees of freedom is nearly the same, while the temperature effect is relatively small. The values given by FEM-simulation are shown in the table 1.

The technology developed for the F/T-sensor consists of four main steps:

- definition of piezo-resistive sensor elements
- contacts to the piezo-resistors
- structuring the metal layer that connects the piezo-resistors of the pads
- etching the silicon to define the areas with largest stress, where the piezo-resistors are located.

To be able to apply a force as well as a torque to the sensor parallel to the design of the silicon sensor a transducer was developed. The transducer will be made of steel and will then be mounted to the robot. The mounting of the transducer to the robot will be realised by screwing, the connection of the steel transducer to the silicon will be done by using a glue. The requirements for the glue are:

- high holding forces in every direction
- no plastic deformation
- defined viscosity for handling and to achieve a constant thickness

Many tests have been set up to find the right glue. The size of the F/T-sensor of 12 mm times 12 mm is mainly defined by the areas for the glue. Future work will be done to reduce the

areas, since the production costs of each sensor are highly affected by the overall area.

The electronics needed for such a F/T-sensor is planned to be realised on a small ASIC mounted directly onto the transducer. For the first tests this electronic is placed on a small PCB, where the main components are multiplexer to switch from one to another resistor, see figure 1. To connect each resistor to this PCB a flexible printed circuit board that will be glued on to the transducer is necessary, as can be seen in figure 2, where to the tip shown at the bottom of the figure the resistors will be bonded.

The relationship between the applied forces or torques and the measured change of resistances is linear, the coefficients of this matrix will be extracted in a calibration procedure. The calculation algorithm of the forces and torques will be realised later using a FPGA.



Figure 2:  
PCB to be glued  
on transducer.

## MEMS-Test and Diagnostics

The manufacturing efficiency of MEMS devices is enhanced if faulty components are sorted out at an early processing stage. Therefore, it is vital to perform wafer-level testing. Methods to achieve this goal are developed and explored. Enhanced optical techniques for 3D-geometry and vibration measurements are applied in real production environment.

Currently, the world of micro device manufacturing lacks exact knowledge of the behavior of materials used for MEMS devices e.g. acceleration and pressure sensors, micro mirrors and RF switches. The dynamic properties of micro parts

show different behavior compared to the same material in a macro world. The investigations concentrate on methods that will enable the determination of material parameters needed in the production of MEMS devices.

Existing techniques such as white light interferometry, confocal microscopy, laser Doppler vibrometry and stroboscopic microscopy are used as a basis for new analytical processes that will need to be developed. All methods and techniques that are developed will be tested in real life. The results of the investigations are highly anticipated, as they will provide far-reaching

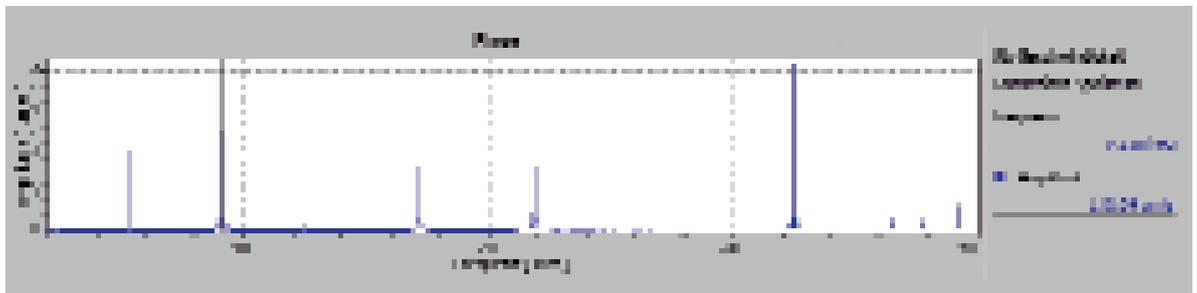


Figure 1: Eigen-spectrum of a gyro fabricated at ISIT in a range up to 40 kHz. Using a chirp excitation the velocity amplitude averaged over about 100 points distributed across the gyro surface is recorded.

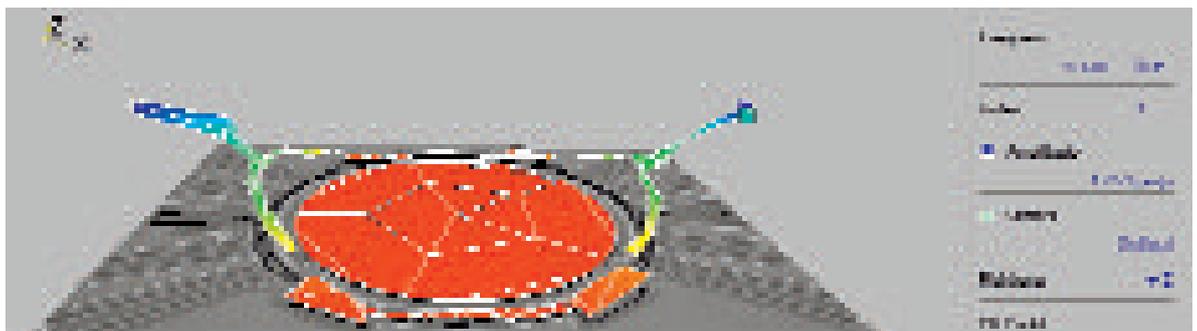


Figure 2: Visualization of an eigen-mode in velocity space of a gyro fabricated at ISIT at an eigen-frequency of about 9.1 kHz.

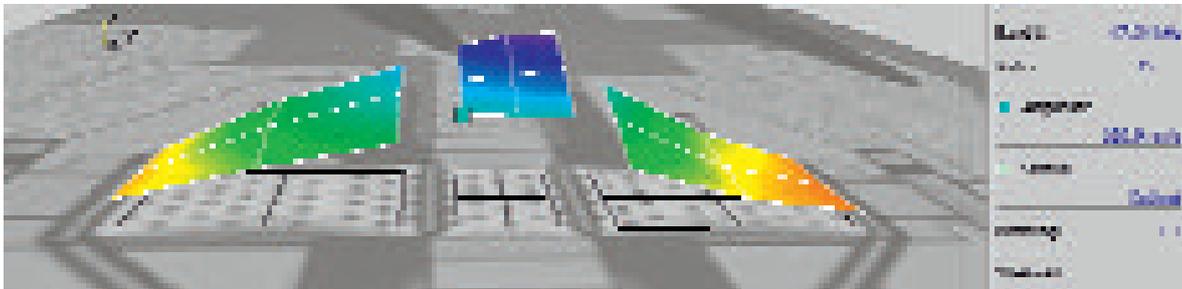


Figure 3: Distribution of velocity amplitudes across the bridge of a RF-switch produced at ISIT using electrical chirp excitation.

benefits for the industry. The diagnostic methods will equip MEMS producing companies with the processes to test the quality and function of their devices in an early stage of process development in order to save time and money in the production process. Furthermore the investigations provide semiconductor equipment manufacturers with the technology critical for developing the production and test systems of tomorrow.

The structural dynamics of MEMS devices, here a gyro and a RF-switch both fabricated at ISIT, are characterized by analyzing the eigen-spectrum of the devices. By doing so, variations in gyro performance are identified and can be linked to process specifics. One example of an eigen-spectrum of a gyro is shown in figure 1 for an out-of-plane vibration in the velocity space using a Doppler vibrometer. Comparing the measured frequencies with simulated spectra, differences in understanding or in process performance can be eliminated. In figure 2 the visualization of a typical eigen-mode of a gyro is presented. The perspective square in the figure sketches the lay-out of the device and defines the basic plane for out-of-plane vibrations. The distance of the colored parts of the device from the basic plane is an indication of the vibrational elongation. One can identify, that for this specific

eigen-mode the central plate of the device stays at rest while the ring surrounding the inner plate performs a mechanical out-of-plane vibration. One can identify the symmetric z-translation mode exhibiting maximum velocity values at the outer ends of the device with nearly identical amplitudes. The analysis of the eigen-modes and eigen-frequencies enables the identification of production variations and gives rise to optimization measures.

The same procedure is applied for e.g. functional tests of RF-switches. In figure 3 an example of an eigen-mode of a RF-bridge is shown elucidating the distribution of velocity amplitudes at selected points across the bridge. Again, the distance of the color-coded parts of the device from the surface plane is an indication of the vibrational elongation in velocity space. One can identify, that the switching membrane vibrates in a longitudinal basic mode with a superposition of a longitudinal torsion mode. Analyzing the dynamic behavior of the membrane for RF-switching devices on wafer level one can easily distinguish between bridges suited for further processing and those with inferior switching performance. By doing so the lay-out of the device and the fabrication process can be optimized such that the process yield may be improved.

## Nano Structures for CNT Transistors

Following the Gordon-Moore road map on high integration CMOS scaling it is generally admitted that the miniaturisation of Silicon based transistors will reach some fundamental limits within the next decade. Most advanced CMOS technology is already focused on feature sizes clearly below 100nm for transistor gate structures and will probably be scaled down to 20 nm within the scope of the next 3 – 4 CMOS generations. However, the limits of transistor scaling, as it was successfully applied since the early beginning of CMOS technology, becomes obvious. This was motivating an intense research activity for alternative devices and materials such as Si-nanowires and carbon nanotubes (CNT).

Single Wall Carbon Nano Tubes (SWCNT) consisting of a mono atomic 2D graphene layer wrapped up to a tube with a diameter in the nanometer range. Depending on the orientation of the wrapped up graphene cylinder (chirality) the CNT can be either metallic or semiconducting. In most cases carbon nano tubes are grown in a CVD reactor by decomposition of hydro carbon. For the nucleation of the growth Ni, Fe or Co catalysts are needed. The orientation of the CNT

growth is influenced by an electric field, means vertical alignment of CNTs is possible.

End of the nineties it was shown that SWCNTs can be operated as Field Effect Transistors using the CNT as a nano-channel controlled by an insulated Gate electrode. Next to the CNT dimension of less than 5nm in diameter, which obviously can create new possibilities for high integration purposes, the main interesting aspect of CNT transistors is the extremely high mobility up to several 10 000 cm<sup>2</sup>/Vs. This is due to a quasi 1D transport mechanism with electron scattering lengths in the  $\mu\text{m}$  range.

Within the European project (CANDICE) ISIT is developing a vertical CNT transistor based on CMOS-compatible processes. For this purpose arrays of nano trenches and nano holes with dimensions down to 30 nm have to be realized as confinements for the vertical CNTs. The growth of the SWCNT is carried out by the partners CNRS and University of Cambridge. The principle architecture of a vertical CNT transistor is shown in figure 1.

### Technology approach for nano structures

The realisation of nano structures in the sub-50 nm range is based on a self-aligned spacer damascene approach which is inspired by side wall spacer technique of materials having a high dry etch selectivity, e.g. SiO<sub>2</sub> and Poly-Si.

In a first step SiO<sub>2</sub> lines and spaces with critical dimensions of 0.3  $\mu\text{m}$  are structured anisotropically with steep walls near to 90°. Subsequently, Poly-Si with a thickness of 20-30 nm is deposited and side wall spacers are formed along the SiO<sub>2</sub> lines by selective dry etching of Poly-Si. After a further deposition of SiO<sub>2</sub> followed by Chemical Mechanical Polishing (CMP) the initial SiO<sub>2</sub> structures are globally planarized. As a result a stripe pattern of nm-scale Poly-Si lines embedded within SiO<sub>2</sub> is realized in one direction.

In order to end up with nano trenches in one direction the exposed Poly-Si lines can be etched selectively by RIE. Figure 2 is illustrating the principle of the technology used with SEM pictures showing nano trenches with 30 nm in widths. The

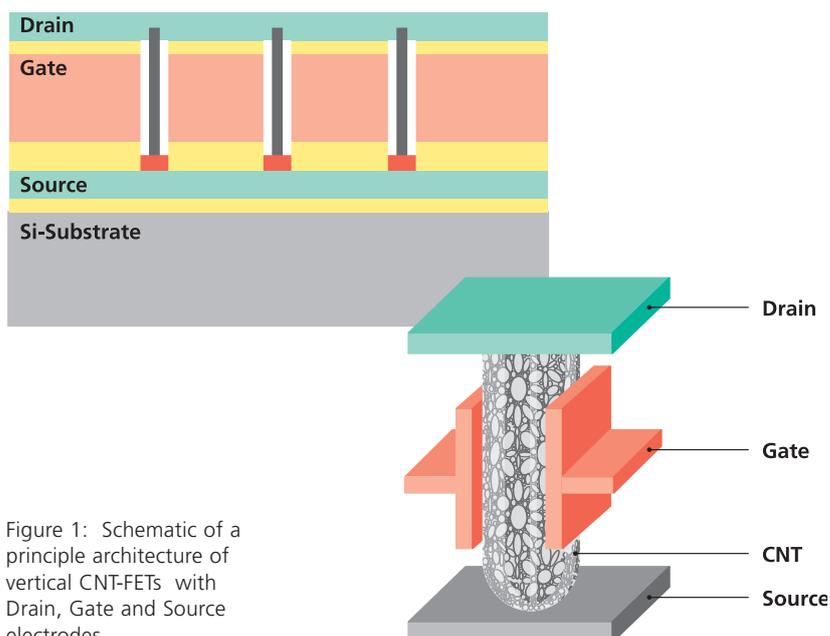


Figure 1: Schematic of a principle architecture of vertical CNT-FETs with Drain, Gate and Source electrodes.

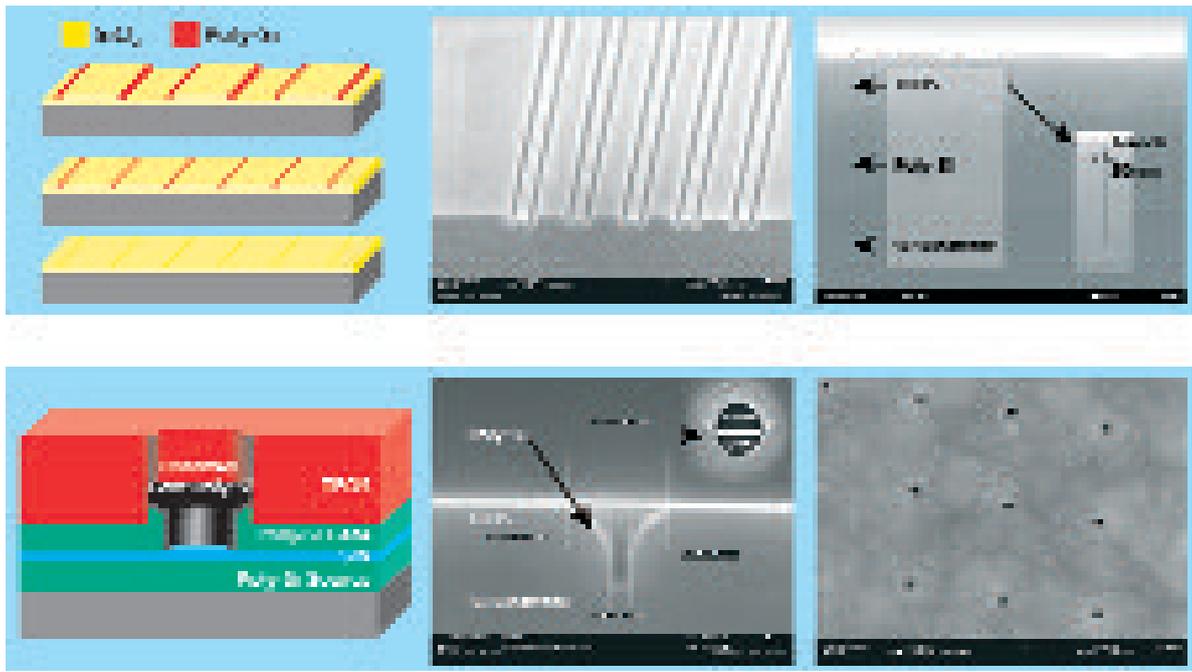


Figure 2: Processing of nano trenches in one direction by a side wall spacer damascene approach.

Figure 3: Realisation of nano holes by diameter reduction based on Poly-Si side wall spacer formation.

aspect ratio is in the range of 30. The dimensions of the nano trenches are not defined by the resolution of lithographic patterning, but instead defined by the thickness of the poly-Si side wall spacers and the selectivity of the etch process.

For the realisation of nano holes instead of nano trenches the same technique can be applied in a second level with an orientation of the embedded nano trenches perpendicular to the first level. The nano holes can then be structured by selective dry etching at the crossing points of the level one and level two nano trenches.

An important feature of this method is the self alignment and lithography independent approach for the realisation of the nano holes. The widths of the nano holes are defined by the side wall spacer thicknesses only, whereas their depth is determined by the thickness of the SiO<sub>2</sub> layer. This gives the opportunity for a variation of the nanohole dimensions by adjustment of the layer thicknesses. The resolution of the lithography determines the nano hole density of the array, not the lateral dimensions of the nano holes themselves.

An alternative method for nano hole fabrication is based on simply hole diameter reduction by side wall spacer technique.

In a first step a layer stack is deposited bottom up comprising out of the Poly-Si Source plate, the SiN Source-Gate isolation, the Poly-Si Gate electrode and the SiO<sub>2</sub> Gate-Drain isolation. An array of holes is then structured into the upper SiO<sub>2</sub> layer and underlying Poly-Si with critical dimension in the 0,3 μm range. In a next step a Poly-Si layer has to be deposited for reducing the hole diameter down to the target hole dimension in the nm-range. By anisotropic etching a Poly-Si side wall spacer within the holes is formed which can simply be recessed by Poly-Si overetching. After oxidizing the inner Poly-Si sidewall spacer the later Gate ring electrode will be isolated against the CNT. The last step for finalizing the template is the SiN bottom layer etch off in order to get access to the Poly-Si Source plate. Here the catalyst will then be deposited by electroplating inside the hole acting as a nucleation side for the CNT growth. The principle technology scheme is illustrated in figure 3 showing first nano holes in the range of 70 nm. From the first results obtained the potential for further down scale of the hole diameter is obvious.

The general technology approach for fabricating nano structures based on selfaligned side wall spacer formation was verified for two different architectures.

## Ultrathin Laser Anneal Fieldstop Trench IGBTs

Energy efficiency is one of the main topics in public discussion driven by the increase of global CO<sub>2</sub> emission. Therefore, power electronics becoming more and more importance, hence power semiconductor devices.

The discrete IGBT (Insulated Gate Bipolar Transistor) is the most important power semiconductor device for power conversion and control in the medium power range with voltages > 400 V. IGBTs are used for most power switching applications in the fields of e.g. automotive, industry and consumer electronics. The main advantage of IGBTs is the excellent conduction behaviour combined with high robustness, so IGBTs are widely used for all kinds of motor control purposes. IGBTs have been continuously improved over the years with special focus on reduction of switching and conduction losses. Here, one of the main activities is the reduction of the substrate thickness down to a blocking voltage dependent minimal value which ensures the Off-state without voltage breakdown. The continuous down scale of the substrate thicknesses over the last years for IGBTs and PowerMOS devices is shown in figure 1. For a 600 V IGBT the device physical limit for the substrate thickness will be reached with the next generations of Trench Fieldstop IGBT development having a substrate thickness below 50 µm. The currently best Fieldstop IGBTs reaching thickness values of about 70 µm.

Discrete IGBTs are vertical transistors, means the current flow is directed from the frontside of the device to the backside. So, the backside is electrically active, since the Emitter and the fieldstop layer are located there.

The challenge in fabrication of ultrathin Fieldstop IGBTs is the handling of substrates with thickness in the range of 50 µm after backside grinding and the limited thermal budget for backside processing in the case the frontside has been finalized before. The limited thermal budget is due to the fact that the frontside metallization do not allow a high temperature treatment for the activation of a fieldstop layer.

Within a BMBF project a new approach for IGBT backside processing was investigated based on low thermal budget laser annealing combined with a carrier concept for ultrathin wafer handling. The principle process sequence is illustrated in figure 2.

After the frontside processing is completed the IGBT wafer is temporarily bonded up side down on a carrier wafer by use of a thermal release tape. Subsequently, the backside of the IGBT wafer can be grinded down below 50 µm since the substrate is mechanically stabilized by the carrier wafer. Ion implantation of Phosphorous for the fieldstop layer and Boron for the Emitter can be applied to the backside of the ultrathin wafer without any risk of wafer breakage. The activation of the implanted dopants is the most crucial process and is carried out by laser annealing technique. It is the advantage of laser annealing that the frontside of the IGBT wafer will not heat up since the the energy of the laser pulse is totally absorbed within a few microns from the backside surface. Depending on the wavelengths of the laser used the absorption depth is different. Finally, the wafer backside is metallized and can be debonded for electrical testing.

First experiments were carried out with a 308 nm XeCl eximer laser for IGBT Emitter annealing having pulse energies around 3,2 J/cm<sup>2</sup> and pulse

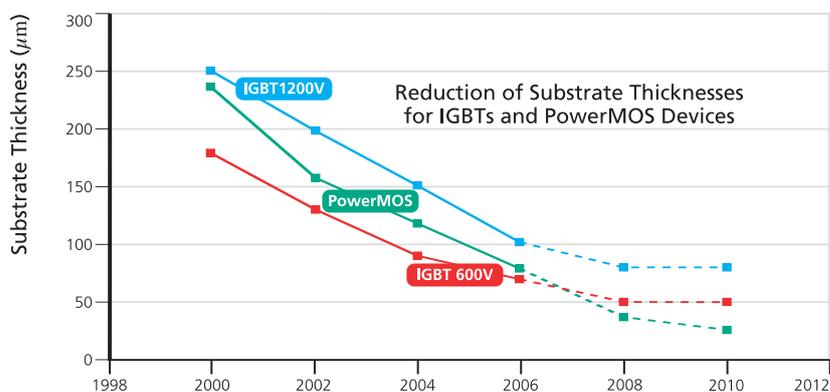


Figure 1: Substrate thickness reduction of power devices during the 2000 – 2010 decade.

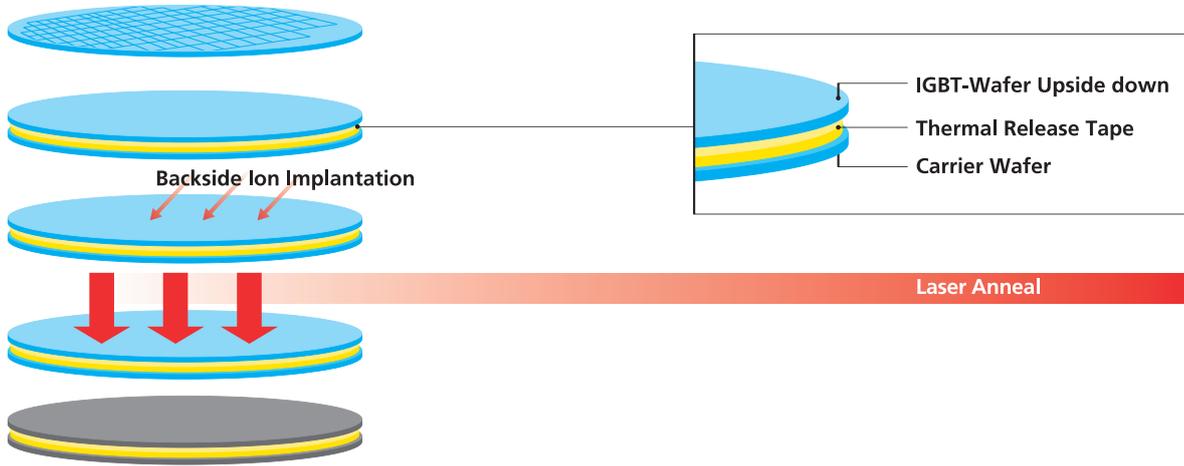


Figure 2: Illustration of the principle process sequence for backside processing of ultrathin Fieldstop Trench IGBTs.

durations of 200 nsec. In this case the fieldstop layer was defined by the substrate itself which was thinned down to a residual distance of 5  $\mu\text{m}$  to the epitaxial Base drift zone. Laser annealing experiments for both, the fieldstop layer and the Emitter simultaneously, have shown that the activation of the deeper Phosphorous fieldstop implant becomes difficult in case a laser wavelength of 308 nm is used. This is due to the high energy absorption within the first 200 nm of the Si-substrate.

Alternatively, solid state laser annealing at a wavelength of 532 nm with an energy density of 3,2 J/cm<sup>2</sup> and a pulse duration in the 600 nsec range was investigated. Sufficient dopant activation of the implanted fieldstop layer down to a Si-depth of 1  $\mu\text{m}$  could be observed in this case. Since the minimum activated dose required for a fieldstop layer is about  $2 \times 10^{12} \text{ cm}^{-2}$  the depths of the fieldstop layer can be in the 1  $\mu\text{m}$  range or even below as long the dopant concentration is in the upper range of  $10^{16} \text{ cm}^{-3}$ . The implantation of both, fieldstop layer and Emitter with subsequent laser annealing is preferential since in this case homogenously doped float zone substrates can be used instead of substrates with epitaxial drift zone layers. A comparison of the spreading resistance doping profiles between both concepts is shown in figure 3. The red curve exhibit the Emitter activation only by 308 nm excimer laser anneal, whereas the blue curve represents the doping profile of the laser activated Emitter and fieldstop layer at a wavelengths of 532 nm.

With the laser annealing technique first electrical results for Fieldstop Trench IGBTs have been achieved with saturation voltages in the range of

1,3 V and switching times  $t_{\text{off}}$  below 50 nsec. A typical turn-off characteristic is shown in figure 4. The blue curve exhibit the Collector current characteristic during turn-off at room temperature with a switching time  $t_{\text{off}} = 30 \text{ nsec}$ . The carrier concept of temporary bonding was suitable for the fabrication of ultrathin IGBTs with substrate thicknesses in the range of 60  $\mu\text{m}$ .

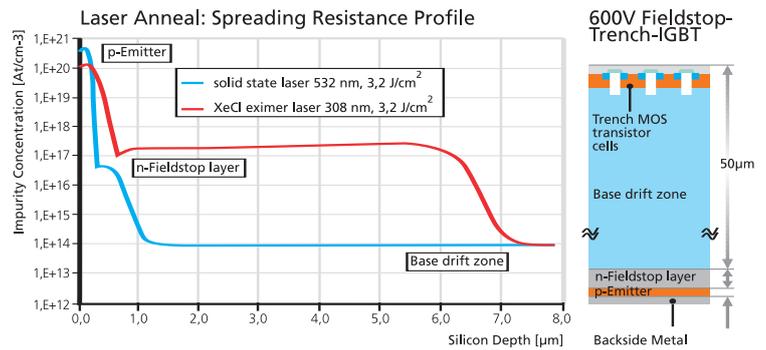


Figure 3: Spreading Resistance doping profiles activated by laser annealing. (red curve: 308 nm, blue curve: 532 nm)

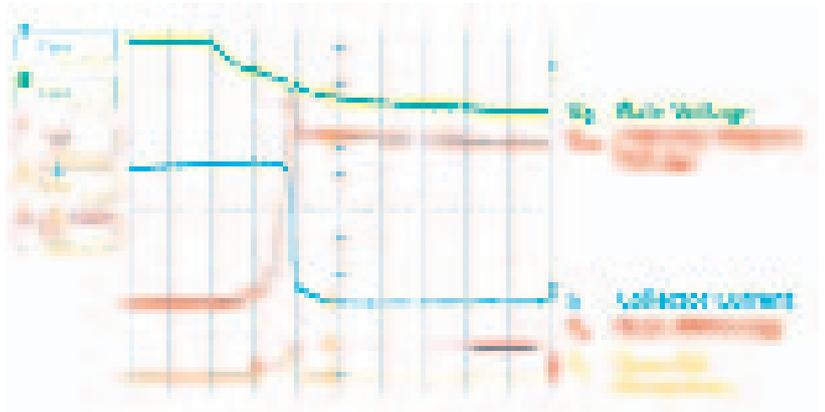


Figure 4: Turn-Off characteristic of a Fieldstop Trench IGBT with Emitter activation by laser annealing.

# Representative Results of Work Biotechnical Microsystems

## Detection of Antibodies in Human Serum with Electrical Biochips

The point of care diagnosis of antibodies in human blood is of high interest because it indicates the state of immunisation. For patients it has to be decided, if a new immunisation against harmful diseases is necessary or not. At present samples had to be transported to external laboratories where ELISAs are commonly used for the measurements. Rapid and inexpensive tests with high sensitivity and reproducibility for the parallel identification of human antibodies, for example against Tetanus or Diphtheria, are not at the market today.

Together with our industrial cooperation partners "eBiochip Systems GmbH" (Itzehoe) and "Institut Virion\Serion GmbH" (Würzburg) we have developed an assay for the detection of Tetanus antibodies in human serum. This ELISA-like assay was performed on an electrical biochip array with 16 positions. Each of the 500 µm positions consists of interdigitated array (IDA) gold ultramicro-electrodes with 800 nm width and 400 nm gap.

All 16 positions have a common cathode. The 16 anodes of the 16 positions are addressed and read out individually. An integrated Iridium oxide reference electrode on each array chip enables fixed potentials set to the cathode and the anodes (figure 1).

The whole assay and the electrochemical detection of an enzyme generated redox active product were done by an "eMicroLISA" device (eBiochip Systems GmbH).

The Tetanus toxoid antigen (Institut Virion\Serion GmbH) was spotted by an automated microdispensing device onto 3 chip positions. It immobilized via thiol links and adsorptive forces to the gold electrodes. Another 3 positions were covered with a human IgG antibody (Institut Virion\Serion GmbH) for positive control. All other positions were covered with a nonbinding protein (BSA) for negative control. The spotted and housed

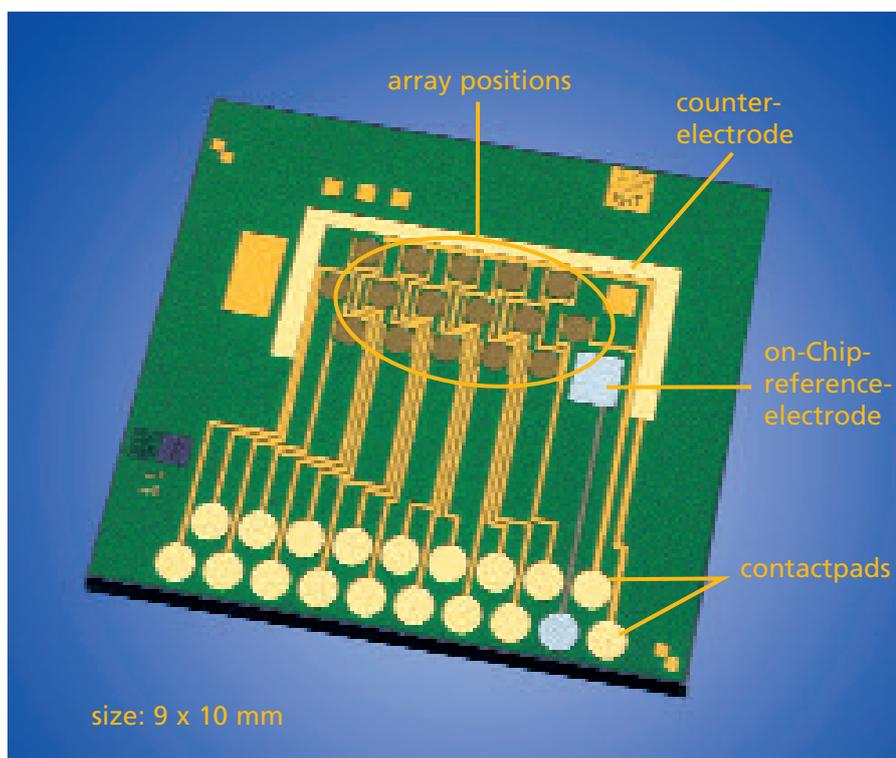


Figure 1: picture of the array chip with 16 positions, reference electrode and counter electrode.

Figure 2: The array chip equipped with a flow cell, "eChipStick" (left) and the "eMicroLISA" device (eBiochip Systems GmbH) (right).



chip (figure 2, left) was simultaneously contacted (electrical, thermal and fluidic) by the "eMicroLISA" device (figure 2, right).

The diluted human serum sample was automatically pumped over the chip and during incubation Anti-Tetanus antibodies bind to the immobilized Tetanus antigen. An added Anti-Human IgG antibody enzyme conjugate acts as a label. It binds to the positive control positions and to Anti-Tetanus antibodies at the Tetanus positions. The BSA positions left unbound. After this labelling step a substrate was added. This substrate was converted by the label enzyme into its redox active form and could be measured specifically for each position in a stopped flow modus. The resulting current slopes are directly proportional

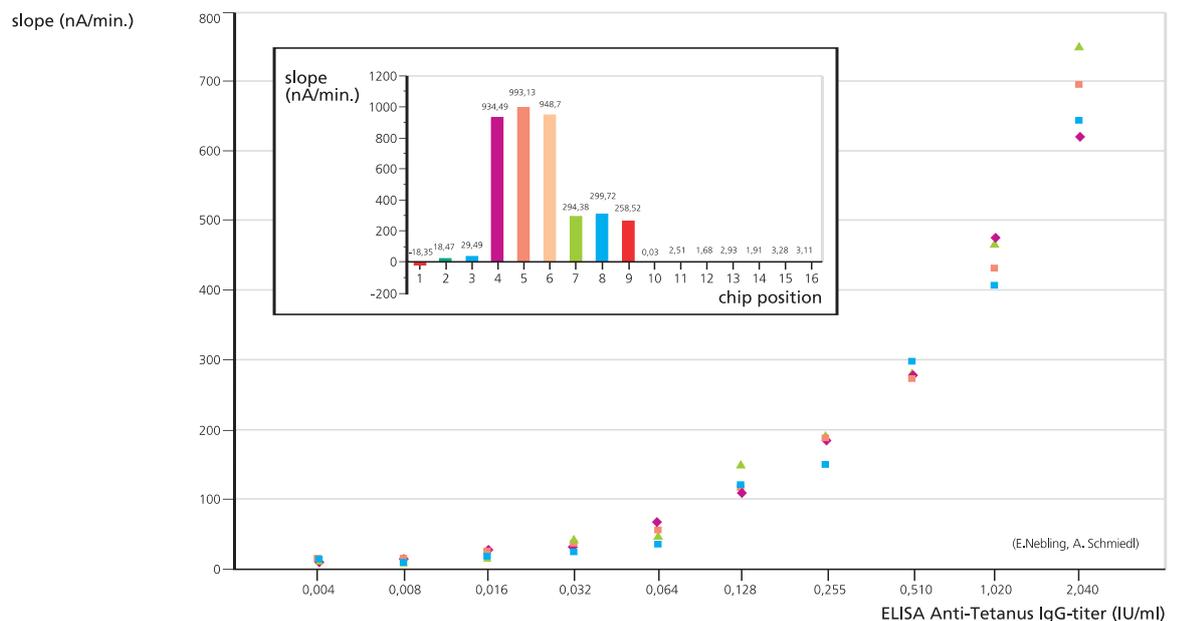
to the Anti-Tetanus antibody concentration and their activity in the sample.

In figure 3 the measurements of different concentrations of a human serum sample are shown. The detection limit is 0,064 IU/ml of Anti-Tetanus antibody. At values higher than 0,1 IU/ml no new immunisation is necessary. The inserted picture shows the detection of a sample containing 0,510 IU/ml (Chip position 4–6: Positive control, 7–9: Tetanus, 1–3 and 10–16: Negative control).

The positive and negative control positions were used for an internal calibration. The whole assay time is 20 minutes. An excellent reproducibility with a correlation coefficient < 10 % was demonstrated for our Tetanus assay in 100 individual tests.

Figure 3: Titration curve of a human serum sample with 4 measurements for each concentration. Inserted picture: The slopes of all 16 positions of a chip incubated with a 0,510 IU/ml sample (Chip position 4 – 6: Positive control, 7 – 9: Tetanus, 1 – 3 and 10 – 16: Negative control).

### ELISA Anti-Tetanus IgG-titer (IU/ml)



# Representative Results of Work Module Integration

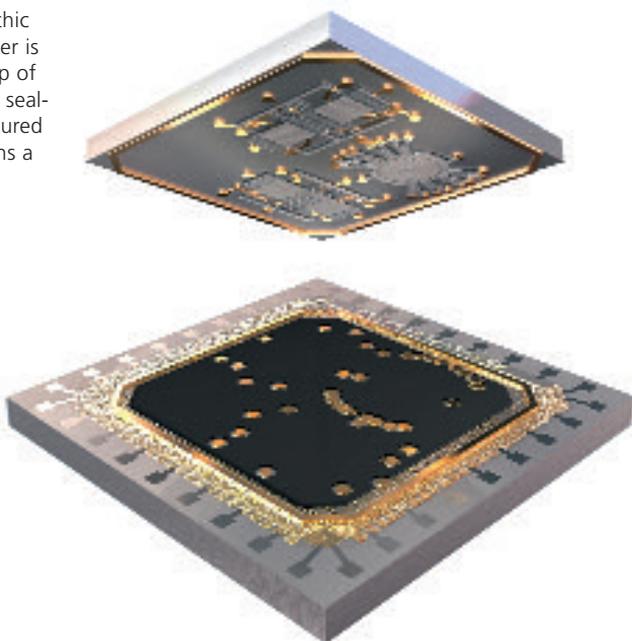
## The Ultimate Miniaturization of Microsystems Packaging

Almost each microelectronic sensor type requires an individual packaging solution: It is obvious that image sensors need a window to the outside, while the thin membrane of pressure sensors must not be covered with thick polymer compounds. But what is special about micromechanical devices?

Micromechanical structures are generated at ISIT by a surface micromachining process. One of the largest application fields is the inertial measurement, e.g. of accelerations (accelerometers) or angular velocity (gyroscopes). Due to their operation principle, these devices need to operate under a controlled gas pressure: While an accelerometer needs a relatively strong atmospheric damping, a gyroscope is designed as a resonator that requires almost no damping at all. This means that a package must be guaranteed to maintain defined pressure of 500 mbar in one case, or even below 0,1 mbar in the other.

Controlling the ambient pressure in smallest cavities was subject of the very successful research project VABOND and is now finding it's way into the automotive industry.

Figure 1: A monolithic inertial sensor cluster is being placed on top of an ASIC. Inside the seal-frame, a fine structured getter film maintains a high vacuum.



But ISIT already prepares the next step:

### The DAVID project.

DAVID stands for "Downscaled Assembly of Vertically Interconnected Devices". The project is funded by the European Commission and is carried out by renowned European semiconductor companies and academic partners under the coordination of Fraunhofer ISIT.

DAVIDs targets are to advance the most important key technologies in microsystems packaging and integration:

- Electrical feedthrough technology on processed CMOS wafers
- Chip-to-wafer bonding of MEMS on ASICs
- Deposition and fine-structuring of getter films on ASICs
- Waferlevel transfer molding
- Fine-pitch solder balling on molded wafers

The ISIT activities in the project are related to the hermetic encapsulation and the feedthrough technologies.

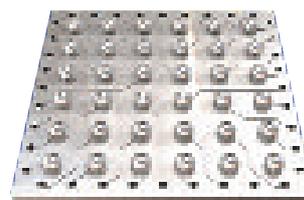
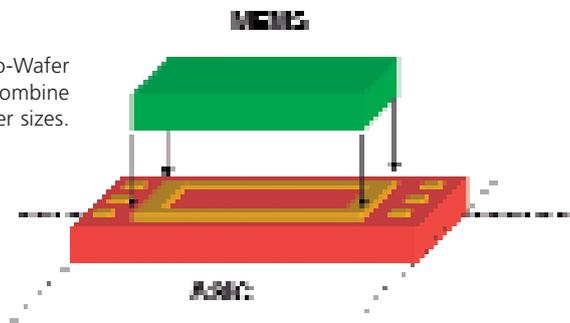


Figure 2: Backside redistribution and fine-pitch ball array for direct soldering to a printed circuit board.



Figure 3: High cost reduction potential can be achieved by waferlevel transfer molding.

Figure 4: The Chip-to-Wafer concept allows to combine dies from different wafer sizes.



### Chip-to-Wafer Bonding (C2W)

Already today, ISIT offers a world-leading gyroscope packaging technology for the automotive market with a lifetime-guaranteed vacuum level. This waferlevel approach uses a passive silicon cap, covered with a thin getter film that absorbs gas molecules to compensate eventual ultra-fine leaks. The two dies needed for the micromechanical sensor (MEMS) and the electronic circuitry (ASIC) are placed next to each other on the leadframe of a conventional IC package.

The new challenge is to provide a chip-scale solution where MEMS and ASIC are facing each other directly to form a small cavity. Instead of a peripheral contact pad array for wire bonding, the top metal layer of the ASIC provides a seal-frame structure and an arrangement of contact pads anywhere within the cavity to allow for shortest interconnects to the MEMS. This optimized signal routing can dramatically increase the performance of the sensor by eliminating parasitic capacitance and reducing signal-to-noise ratio.

The manufacturing of this new “chip-scale system in package” (CSSiP) is a semi-waferlevel packaging process: Tested, singulated MEMS are placed on an ASIC wafer. By means of a wafer map, the die bonder can skip bad ASICs to optimize the total yield.

### Electrical Feedthrough in CMOS Circuits:

Although the die stack presented above could be wire-bonded in a conventional way, ISITs vision is to integrate the whole sensor system in a chip-scale package. This requires a 3D signal redistribution from the ASIC frontside to a solder ball array on the backside.

The key element is an electrical feedthrough technology that can be applied on processed CMOS chips. This is a globally followed challenge mostly targeting for 3D-integration of logic circuits. In contrast to the ultra-thin silicon used in these approaches, ISIT works with wafer thicknesses of 300 µm to achieve best mechani-

cal properties for sensor packaging. The main problems to overcome result from the necessary high aspect ratio of feedthrough holes: A high performance is expected from the deep reactive ion etching (DRIE) process to create smooth, cylindrical sidewalls, stopping right under the frontside metal layers.

Conformal coating processes for sidewall insulation and metallization must be developed. For compliance with CMOS structures, all processes shall remain in a temperature range below 400°C. Novel copper and nitride deposition processes are being developed in collaboration with ISIT by Fraunhofer IST in Braunschweig; first studies have shown a remarkable quality in terms of process time and uniformity of the conformal deposition in deep structures.

→ [www.david-project.eu](http://www.david-project.eu)

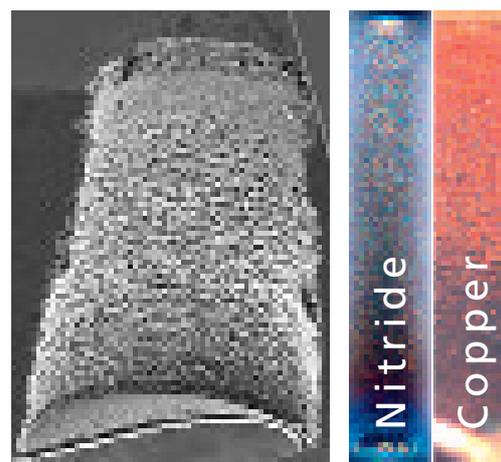


Figure 5: After the via etching process, the contact pad on the CMOS frontside becomes a very thin membrane.

Figure 6: Conformal coating with a nitride insulator and a conductive copper layer are basic elements of an electrical feedthrough process.

# Representative Results of Work Module Integration

## Hermeticity Testing of Vacuum-Sealed Microresonators

It is widely understood that microsensor packaging is one of the most important and challenging, technology areas. In particular, hermetic packaging on wafer level is a key technology of many microelectromechanical systems (MEMS). Beside the effective parallel production, the hermetic sealing protects the devices from harmful environmental influences. The hermetic package is often the base to guaranty device reliability and lifetime. Recently many sensors are using micro-resonating structures to improve their sensitivity. These microresonators need a specified gas damping (fine vacuum environment) within the sensorpackage to function as desired. Beside the many possible causes affecting the lifetime of a microresonator, a new question arises on the long-term vacuum degradation. The manufacturer is often asked to guaranty a lifetime of every single device of inbetween 10 – 20 years, depending on the application. ISIT has therefore studied the different effects that cause a degradation of the cavity vacuum to understand the available parameters to prolong the vacuum lifetime by optimized device construction.

### Selection of a Vacuum Wafer Bonding Technology

For a new device, the first question will be to select the optimum wafer bonding technology to achieve a good initial cavity vacuum. The technology selection within the available wafer bonding techniques at ISIT is affected:

- by the device construction
- by cost and yield requirements
- by necessary vacuum level
- by the stress sensitivity of the device,
- by different compatibility issues like wafer cleaning or backfilling
- by the lifetime demand
- the field operation environment
- the second level packaging and
- qualification tests that have to be passed

Even the availability of a second source for either critical materials used during the bonding process or for outsourcing the bonding procedure may

be serious selection criteria. In the last years, ISIT has developed different wafer level metal sealing technologies for process temperatures ranging from 250 °C to 420 °C and a fine line glass frit sealing process working at 430 °C. A AuSn to Au sealing process is currently before industrialization for RF-MEMS and a Au to poly-Si sealing process has been successfully industrialized for inertial MEMS sensors. ISIT provides narrow glass frit seal frames deposited on customer specific cap wafers that can be bonded at the customer side if required. All sealing technologies can pass standard reliability tests including pressure cooker test at 121 °C for 96 h.

### Vacuum Lifetime

The cavity atmosphere at the end of the device lifetime is defined by the total gas pressure at room temperature, for that the driving ASIC is reaching the calibration limits at one of the operation temperature extremes. The use of Non Evaporable Getter (NEG) material (Zr based alloy) is required to ensure suitable vacuum (total pressure under  $1 \times 10^{-3}$  mbar) and helps to achieve a long-term stability of the damping atmosphere in MEMS devices. NEG can chemically absorb all active gases, including H<sub>2</sub>O, CO, CO<sub>2</sub>, O<sub>2</sub>, N<sub>2</sub> and H<sub>2</sub>. The main constraints imposed by the device design and process are the compatibility of the getter with the fabrication process, the thickness of the getter film and an activation temperature compatible with the bonding process.

### Definition of Damping Atmosphere

ISIT has developed a unique wafer bonding process that achieves a defined gas damping for resonating sensors. A gas-backfilling procedure has been introduced just before the sealing of the sensor cavities. Only noble gases or gases that do not consume the getter or alter the getter sorption performance may be backfilled in the device cavities. Argon, Krypton or Xenon may be selected because of good damping characteristics and low outdiffusion. The backfill operation is typically one step in the wafer bond cycle. The cavity pressure can be tuned to any value between  $10^{-4}$  mbar and 1000 mbar, even

overpressure is possible depending on the wafer bonder infrastructure. For pressures over 10 mbar, no integrated getter is required. The pressure inside the individual sensor cavities is determined by a measurement of the quality factor of the microresonator. ISIT applies the so called ring-down method to measure quality factors in the range of 500 – 500.000 with low measurement failure. The measured quality factor does not give the atmospheric gas composition, merely it is a measure of the total pressure in the device cavity based on a reference plot, see figure 1.

### Hermeticity Testing

If no noble gas backfill is performed, the pressure inside of the vacuum encapsulated devices depends mainly on the outgassing of the inner surfaces, the leakage rate through fine leaks and permeation through the walls, see figure 3.

The outgassing depends mainly on the fabrication process of cap and device wafer, which has to be optimized. Due to the high Helium permeation in silica a long-term stable, high vacuum better than  $10^{-4}$  mbar is very difficult to achieve.

Fine leaks arise from imperfect bonding or crack initiation. The pressure change per unit time in a device can be expressed as

$$dP/dt \approx q / V$$

where  $q$  is the standard leak rate and  $V$  the cavity volume of the device. Typical cavity volumes range from  $0.1 \text{ mm}^3$  to around  $5 \text{ mm}^3$ .

Since fine leaks may always be present a leak test is necessary to guarantee a leakage rate which is small enough to be compensated by the getter. This maximum allowable leak rate may be called the critical leak rate, as it defines the devices within the statistical cavity pressure distribution that fails first after the guaranteed lifetime is fulfilled. Typical tolerable leakage rate for a cavity volume of  $< 1 \text{ mm}^3$  with getter range in the order of  $1014 \text{ mbar}\cdot\text{l/s}$ .

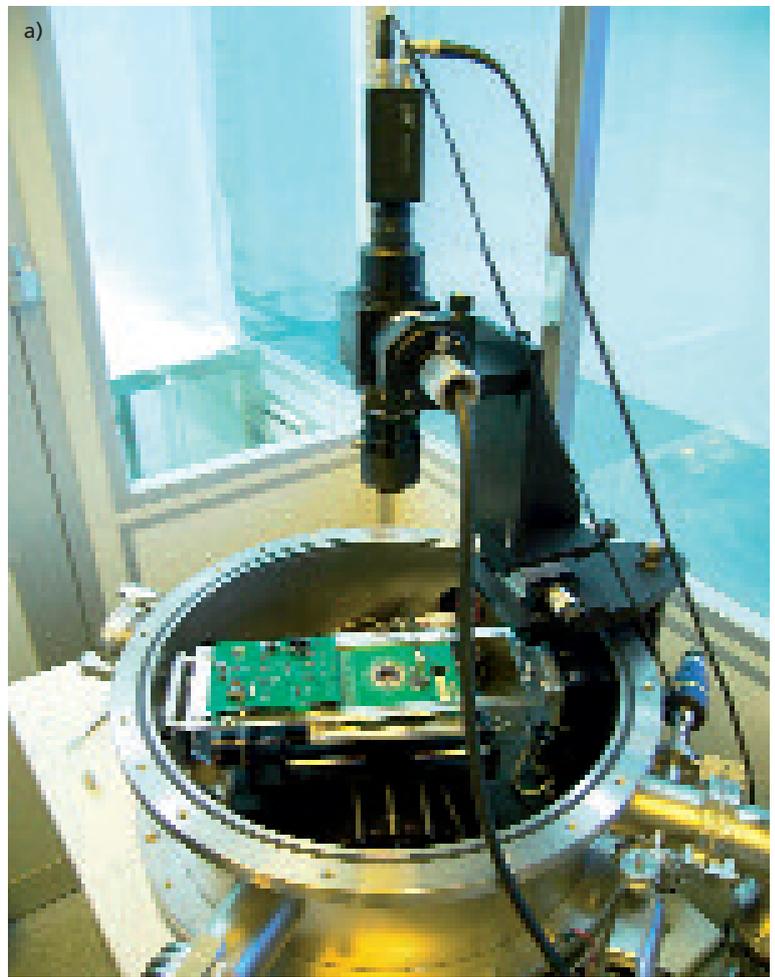


Figure 1:  
a) Vacuum wafer prober to measure pressure dependency of Q factor.  
b) Neon bombing chamber.

The quality factor monitoring methodology has been further elaborated by Fraunhofer ISIT. The test procedure is now called the Neon Ultra-Fine Leak Test. This hermeticity test based on Neon test gas is the first test worldwide that can be performed in-line on wafer level. The initial leak rate of every single resonating device before further packaging can be measured without big efforts or time delay using existing wafer probers. Leaking devices will be identified and sorted out before shipping. The in-line test is compatible with all existing vacuum wafer bonding technologies e.g. glass frit bonding, metallic bonding, eutectic

# Representative Results of Work Module Integration

bonding, low temperature bonding and anodic bonding, reactive and thin film sealing as well as transfer cap sealing technology. The test is not affected by the material selection of the device wafer. The hermeticity of lateral and vertical electrical feed throughs is tested in the same instance.

## Common Methods for Leakage Detection

This ultra-fine leak test overcomes the limitations of He and Kr<sup>85</sup> fine leak testing. The sensitivity of the He fine leak test is limited by the capabilities of the mass spectrometer used and the delay times between bombing and measurements. Typically, the sensitivity is limited to 10<sup>-9</sup> mbar l/s, which is a factor of 100.000 below the necessary sensitivity to assess the hermeticity of modern inertial sensors. The test can be performed on single devices or in batch mode, but is very ineffective for device cavity volumes below 50 mm<sup>3</sup>. The Kr<sup>85</sup> fine leak test differs from He fine leak test in measuring the outgoing gamma-radiation from within a device cavity and not the outdiffusion of the tracer gas itself. The short-

comings of the radioisotope method are the long bombing time to achieve a leak rate sensitivity around 10<sup>-12</sup> mbar·l/s, the high cost of test equipment, the interference during scintillator measurements of neighbouring devices on a wafer, and handling of radioactive Kr<sup>85</sup> gas. Not to forget, both test methods have to be performed with an additional cross leak test to check for rough seal defects.

## In-line 100% Hermeticity Screen

The new developed *Neon Ultra-Fine Leak Test* developed at Fraunhofer ISIT is based on high pressure bombing in Neon atmosphere and the measurement of the quality factor before and after the bombing. The main strength of the test is that it allows a 100% hermeticity screen on wafer level using standard wafer probers. The use of automatic wafer probers for test eases electronic mapping of the results obtained. Other than with He or Kr<sup>85</sup> test, no further cross leak test in liquids has to be performed to verify the measured leak rate. The delay between bombing and Q-factor measurement is not critical. Gas may leave the sensor cavity only if the partial pressure of the test gas in the atmosphere is lower. Even in this case, the partial pressure difference will be very small. Gas leaving the sensor cavity will also be substituted by air entering the cavity through the same leak. Even when all active air gases will be gettered and do not change the Q-factor, the high Argon partial pressure in the atmosphere will make the device be identifiable as leaking. No false reading can be generated, that the device is more hermetic than it really is.

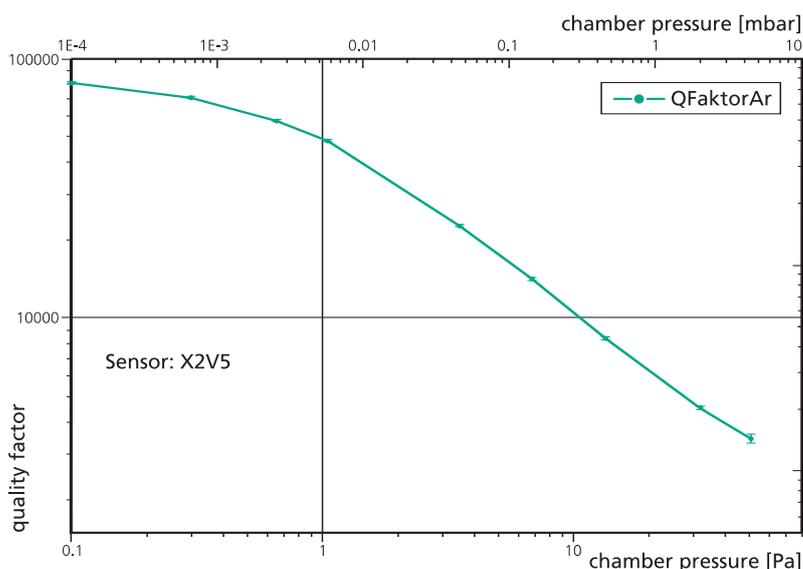


Figure 2: Dependency of the Q-factor vs. cavity pressure for a typical surface micromachined resonator.

The test procedure is compatible with integrated getter films. The use of inert gas is mandatory for the test as all other active air gases will be gettered and do not increase the cavity pressure. The new in-line ultra-fine leak test is unaffected by the typically very small cavity volumes. Other than with all existing fine leak tests, the sensitivity of the test increases with decreasing cavity volume, as the pressure increase during the Neon exposure is larger in a smaller cavity

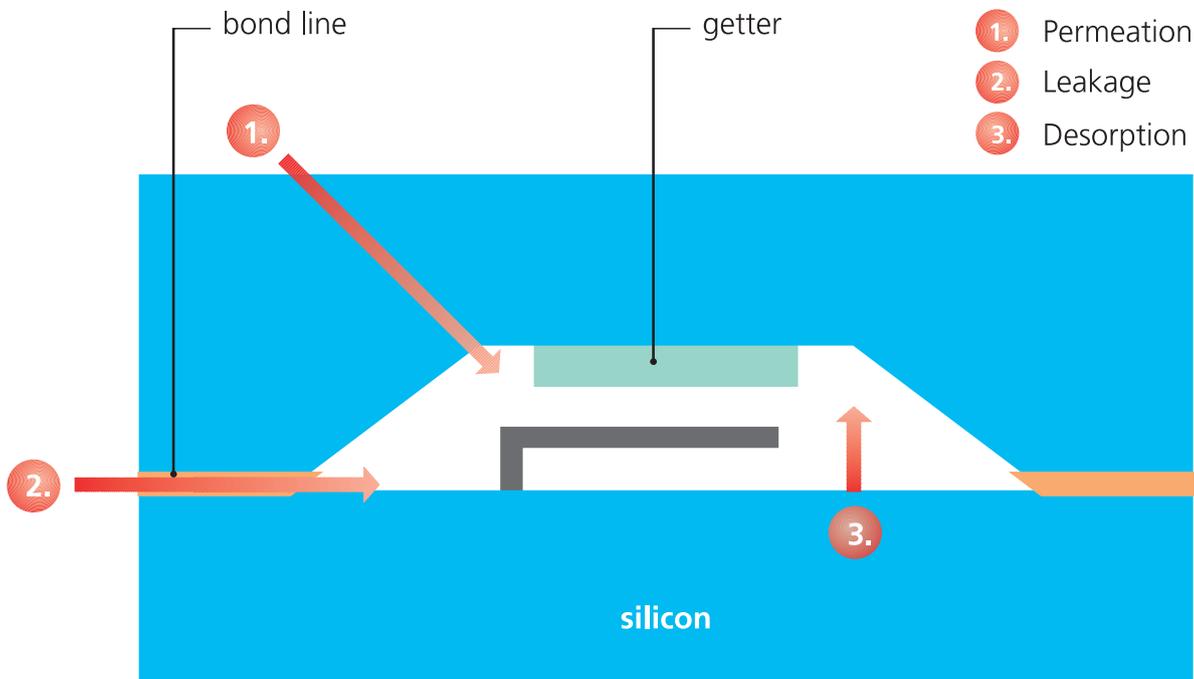


Figure 3: Effects degrading the cavity pressure.

for a given leak rate and exposure time. The test is not limiting the lateral size and pitch of devices on a wafer. Only the ability to access the bond pad locations with a needle prober is required. The Q-factor measurement of every single device is highly selective and not affected by leaking neighbouring devices. The Neon tracer gas is selected to achieve a high leak penetration rate but on the other side prevent permeation through the wall materials of hermetic devices. Helium as a tracer gas would cause wrong leak rate measurements as the permeation of Helium in fused silica even at room temperature is around a factor of 1000 higher than for Neon. Experiments with Helium bombing show a Q-factor decrease of all hermetic bonded devices by Helium uptake, that can be verified by residual gas analysis. On the other side, the use of Argon or any other heavier inert gas will decrease the test performance through the much smaller gas transport rates of these gases in nano-meter size leak channels.

With a bombing time of one day in Neon at 3 bar absolute pressure, devices with maximum allowable critical leak rates in the range of  $10^{-14}$  mbar-l/s will be identified with a sensitivity demand of the quality measurement corresponding to  $10^{-2}$  mbar pressure change.

The measured initial leak rate states the 0h hermeticity of the tested devices and does not guarantee the stability of the leak during aging. The influence of device aging and external stresses on the standard air leak rate have to be investigated for each sensor package construction separately. Fraunhofer ISIT has started to find a 100 % hermeticity test for highly damped MEMS devices (e.g. accelerometers) where Q-factor measurements do not work anymore.

# Representative Results of Work Module Integration

## Ultra Thin Die Connection by Isotropic Conductive Adhesive

Moore's law predicts an ongoing shrinkage of transistor dimensions combined with an exponential increase of chip functionality and speed. As a consequence handheld products like cellular phones are combining increasing functionality with decreasing dimensions. For many applications the size of the final product is limited by the dimensions of the chip package. Nowadays bare dies without any housing are used in many applications. To achieve a further reduction of space the dies are typically thinned down to a thickness of some hundred microns. Our institute has worked on several projects like FLEXSI and FLIBUSI where this trend has been carried forward to chips well below 100 micron thickness.

In the majority of cases these bare dies are glued face-up onto a substrate whereas the electrical connection is realized by wire bonding. An alternative approach is called flip-chip technology because the chip is placed face-down, i.e. flipped, onto the substrate. In this case the electrical connection can be achieved by soldering (common practice), thermocompression, ultrasonic bonding, or gluing. The latter approach splits even further in gluing with isotropic conductive adhesive (ICA), anisotropic conductive adhesive (ACA), and non conductive adhesive (NCA).

In the course of an industrial project we have developed a flip-chip process based on isotropic conductive adhesive for dies with 55 micron thickness. The process has been realized on our fully automated flip-chip bonder Datacon APM 2200. During the placement process the stud-bumped chips are picked from a dicing tape, flipped face-down, dipped into a thin film of isotropic conductive adhesive, and placed onto the substrate. To achieve a non fragile assembly the space between the chips and the substrate is commonly filled with a dedicated epoxy glue. To optimize the throughput, a one-step process and a two-step process have been investigated. In the first case the epoxy glue was dispensed immediately after the chip placement, whereas the conductive glue was cured first in the second approach.

Since the chips are not fixed during the curing of the single-step approach a misalignment of approximately 70 microns has appeared due to the shrinkage of the underfill material in combination with the asymmetry of the underfill process. In case of two separate curing steps this effect could not occur, resulting in a final placement accuracy around 10 microns.

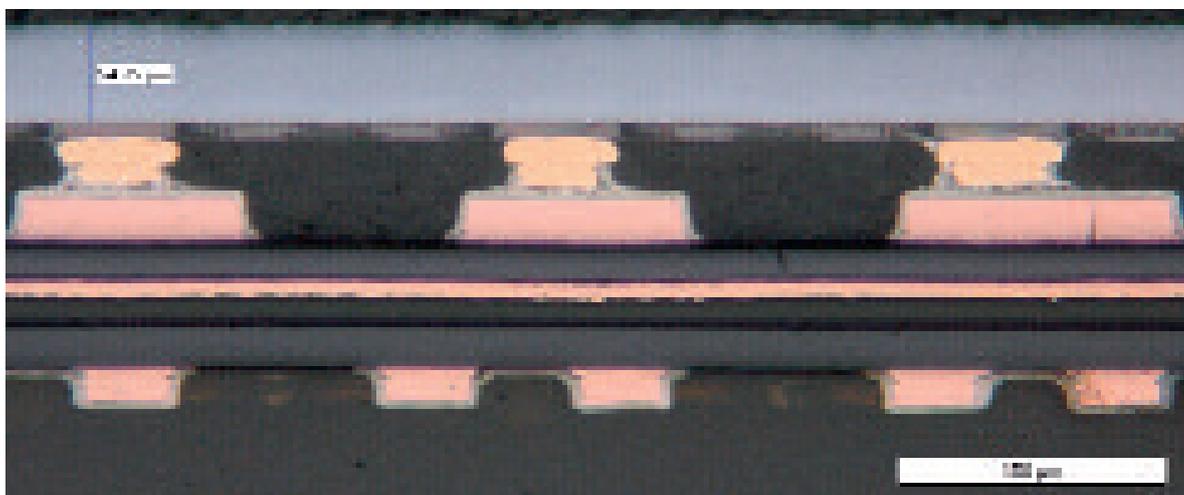


Figure 1: Cross-sectional view of an ultra thin silicon die connected with isotropic conductive adhesive to a flexible substrate.

## Joint Industry Research on Lead-Free CSP Reliability

Reflow solder joints contain voids. These voids form during surface mount assembly by flux reactions with metal oxides during wetting of a metallic surface, in part also resin droplets remain inside the solder melt and, upon cracking of the large resin molecules, they form bubbles. Many factors affect the void formation: flux activity, boiling point of the flux solvent, amount and type of oxides on the contact surface, faults in the surface, and last not least design induced voids, e.g. microvia in land, on which regularly large voids are found. For example, a void size exceeding 25 % of the ball area as found in x-ray transmission radiography of a BGA component is considered a defect by industry standard. The same industry standard states, however, that design induced voids, e.g., microvia in land, are excluded from these criteria. Therefore, an extensive study was started to understand the correlation of microvias, void size and location, and solder joint life. The reliability study was performed combining analytical and FE simulation by partner TU Dresden with temperature cycles applied at the ZVE laboratory, and crack length measurements on CSP solder joints performed at the metallography lab at Fraunhofer ISIT, Itzehoe.

### Testboard Layout, Sample Manufacturing and Verification

A testboard was manufactured from standard FR4 material, with variations in microvia design e.g. solder mask defined CSP pads with and without concentric microvia-in-pad. Other components like BGA, QFP, TO220 and R0805 were integrated in the layout with microvia design options partly excentric in the pads. The focus was laid on lead-free CSPs, although there were also lead containing CSP components used for comparison. Soldering was performed on a convection reflow oven, using a linear ramp profile for some, and a plateau profile for others, along with peak temperatures of 240°C and almost 250°C. The total reflow profile time was ca. 6 min.. As voiding was found in uneven distribution over each single component, several assemblies were investigated by 2-D-/3-D x-ray methods to classify the voiding rate and to select locations of large voids especially for microsection (see figure 1). Part of the project task was development of an automated method for this void classification, achieved by the partner Fraunhofer IIS at its x-ray laboratory EZRT in Fürth.



Figure 1: Vertical section through CSP-solder balls from 3D x-ray volume reconstruction.

# Representative Results of Work Module Integration

## FEM-Simulation Conditions

Creep strain accumulates during temperature cycles in the solder joints due to thermal mismatch between CSP (Chip Size Package) component and PCB (Printed Circuit Board) until crack formation and fracture leads to electrical failure. The FEM (Finite Element Modelling) calculations simulated 6 characteristic void configurations, 2 temperature cycle profiles, namely a fast versus a slow one, and compared Sn63Pb37 with the lead-free solder alloy Sn95,5Ag3,8Cu0,7. For both alloys, creep deformation material constants were taken from experimental data available from Schubert and Wiese (TU Dresden) from former studies. The chosen boundary conditions for the 3D-model reflect ideal shear loading of the solder joint. To avoid artefacts arising from comparison of different FE nets, the voids were incorporated indirectly by implementing an inhomogeneous Young's Modulus. Minimum creep band strains and the Coffin-

Manson law was the base for life time assessment. In order to keep computing time short, the calculation of these 24 conditions was performed on the super computer at the "Zentrum für Hochleistungsrechnen" (Centre for High Performance Computing) at TU Dresden (see figure 2).

## Results of FE-Modelling

1. Stress concentrates to higher values around the solder joint circumference than in the void surface, i.e. crack initiation is to be expected on the outside of the joint (see figure 3).
2. Creep band location and shape, reflecting the anticipated crack path in the solder material, depends mainly on the void configuration. There is no significant influence from solder material or temperature profile.
3. Increased void volume yields increased life for both alloys in all void configurations in the current model (ideally stiff substrate). The reason is the accompanying increase of joint compliance, lowering global stress and creep strains. On the other hand, voids induce force flux deflection leading to local stress concentration, which may lead to crack initiation in void surfaces (see figure 4).

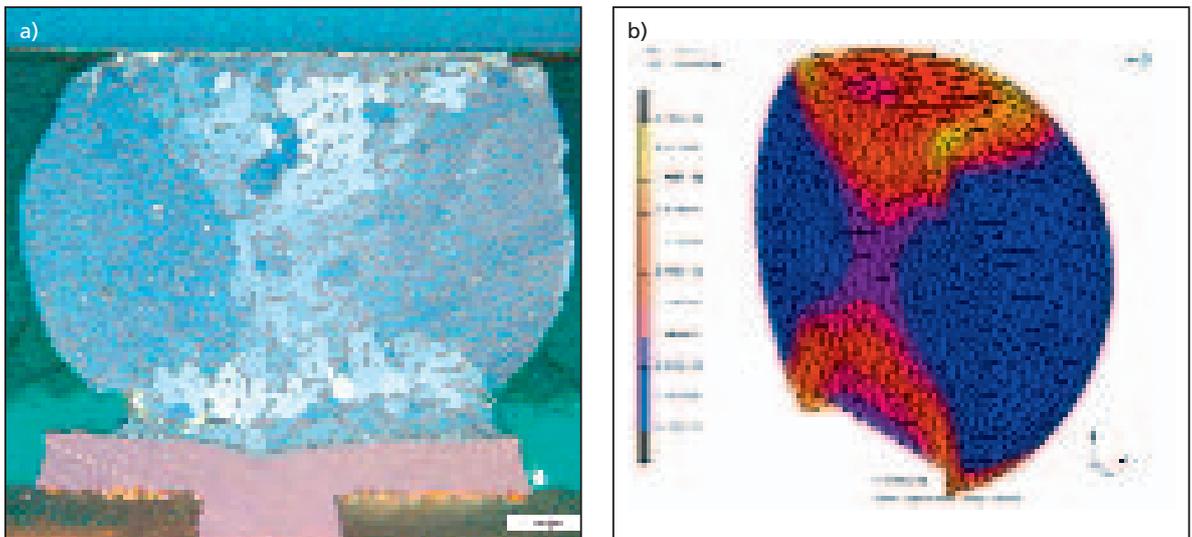


Figure 2: a) Solder ball microstructure with recrystallized areas. b) FEM result of creep deformation.

4. The lead-free solder alloy, with its distinctly higher Young's Modulus, provokes higher creep strains, but leads mostly to longer cycle life as compared to Sn63Pb37.
5. Slower temperature cycles and shorter distance to the component centre induces also longer life time, due to reduced creep strains.
6. The indirect method of void incorporation ensures constant network accuracy, however leading to different extrapolation errors in the calculation of the creep band strain. It is suggested here to apply a creep strain hypothesis.
7. The direct method for void assessment means higher effort, but is essential in case the total stress and strain distribution in the void surface needs to be evaluated.
8. Microsections support the predicted crack path along the creep bands.

#### Strain Measurements on CSPs Mounted on PCB

The thermal mismatch between silicon and substrate material causes bending of the CSP and the printed circuit board it is soldered on. This bending is measured by two strain gages mounted on the opposite sides on top of the CSP and under the bottom side of the PCB. For comparison, the free strain of a non constricted part of the PCB is measured at the same time in X- and Y-direction (see figure 5).

It was found that SAC (Sn Ag Cu) solder causes a high stress build-up, which is measured as a large strain difference between the circuit board underneath the CSP, and the free PCB area. With SnPb solder, the stress bildup is comparatively small, relaxing almost completely at elevated temperature, see figure 5 (red circles versus green triangles). A model treatment, performed with the CTE values for CSP/Si = 3.0 ppm/K and PCB = 12.5 ppm/K supports this finding.

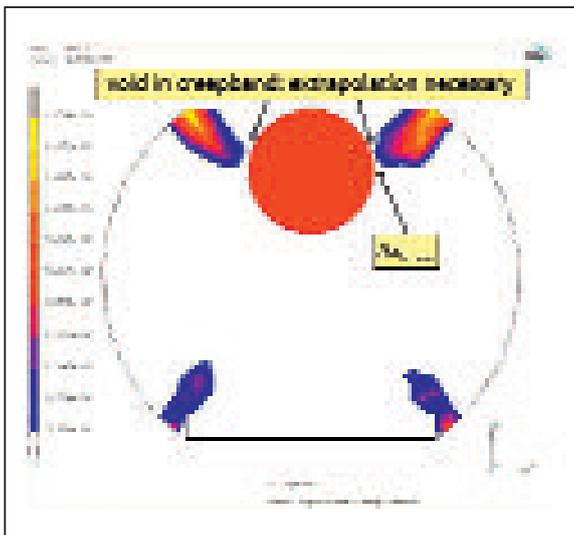


Figure 3: FEM result – void top.

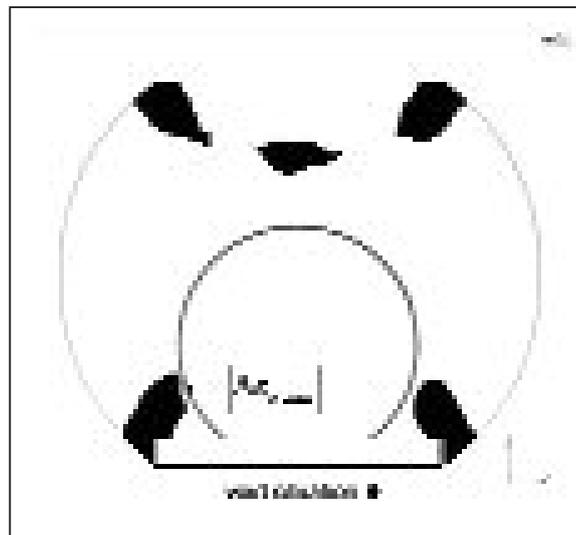


Figure 4: FEM result – void bottom.

# Representative Results of Work Module Integration

## Correlation from the View of Analytic Modelling

Generally, voids are not location of crack initiation. Depending on void size and location, however, the local strain amplitude may become more inhomogeneous, thus the local strain amplitude which leads to fatigue damage may be enhanced or reduced. Voids reduce the cross section and with it, the mechanical stress associated with a given displacement amplitude. Smaller reaction forces increase, at a given stiffness of the assembly, the displacement amplitude, i. e. the load is aggravated. The FE calculations yield reduced strain amplitudes due to voids at a given load, meaning that a void does not generally reduce the lifetime.

The stiffness of the current model resembles an assembly where two CSPs are mounted opposite each other on both sides of the PCB.

A single void in a single solder joint within an array will not incur notable influence of the stiffness of the total assembly; arrayed voiding, however, will reduce the stiffness averaged over all joints, and, by that increase the deformation of each connection of the array. This means increase in deformation amplitude for each connection and thus reduced lifetime.

## Temperature Cycles and Crack Length Evaluation

The experimental part of this investigation consists mainly of multiple microsection layers, i. e. 5 layers through each CSP component, and crack length measurements on each of the ten ball shaped solder joints in the micrograph. The crack length was measured separately on the component and on the PCB side, and to the left and the right of the center axis. Further, the void radius was documented, if a void volume was present above the PCB copper surface (a void present in the microvia below the surface was not counted). The void radius was always measured as a projection of the largest hollow volume into the PCB surface.

Larger voids were found in lead-containing than in lead-free solder joints. This can be attributed to the fact that the same solder profile was used for both solder alloys. Therefore, the lead-containing solder joints were decidedly longer in the molten state. This yields more time for flux residues cracking and vapourizing when trapped and enclosed in spots along the interface between the solder melt and the metallisation surface on the PCB or the component.

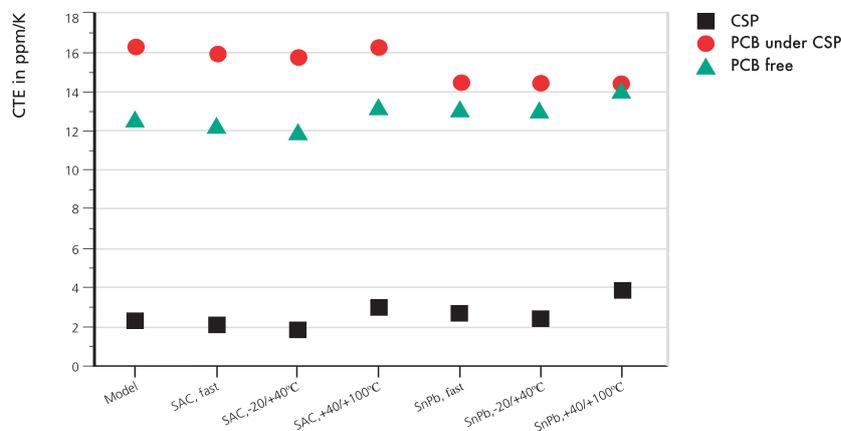


Figure 5: Coefficient of thermal expansion (CTE) measured and calculated (model).

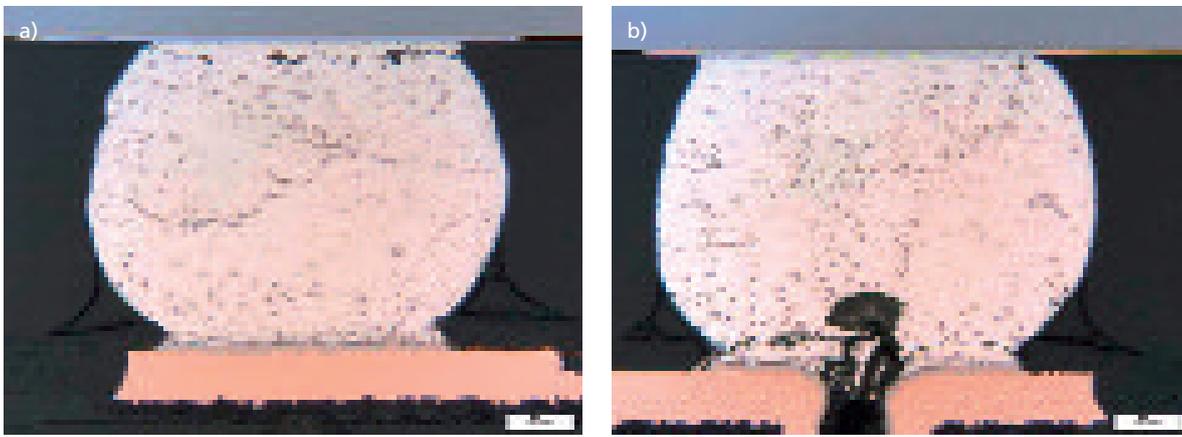
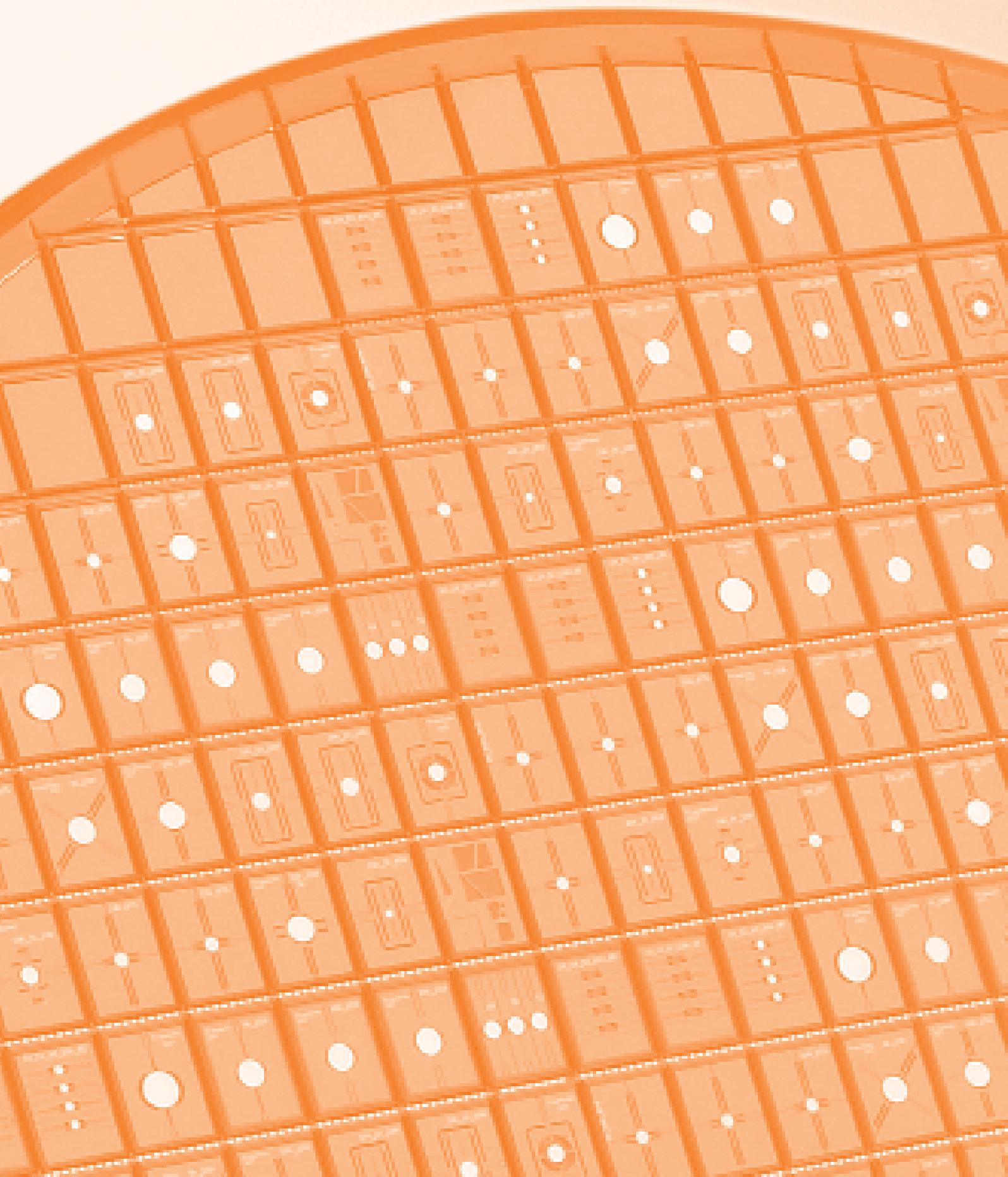


Figure 6: a) SnAgCu without microvias, 500 cycles, crack top. b) SnAgCu with microvias, 500 cycles, crack bottom.

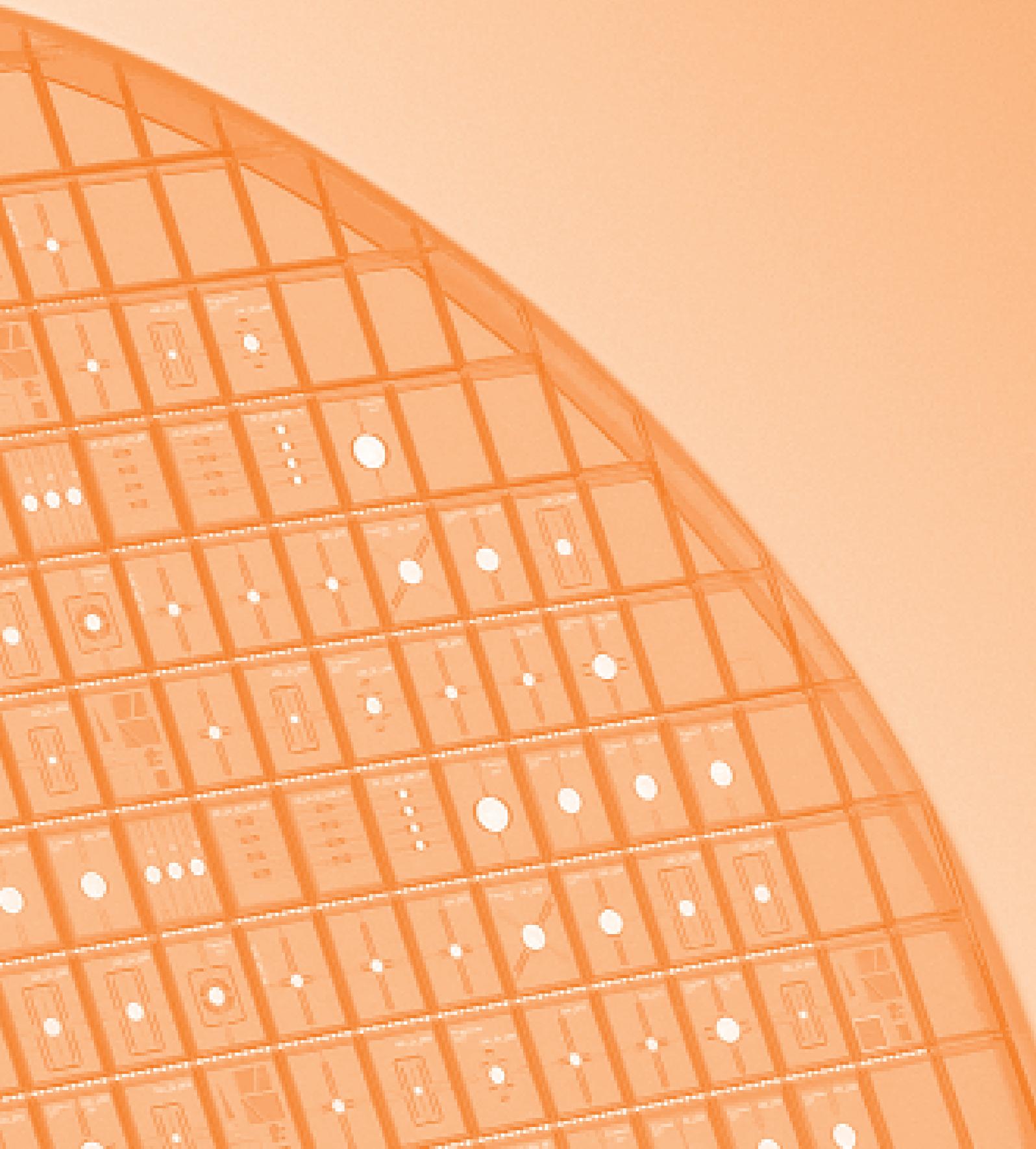
Each microsection represents a variation of load amplitudes from the outside into the centre of the CSP component. Shear cracks start from diagonal “corners” (see figure 6), demonstrated in graphics in which crack lengths are added as “top left plus bottom right”, which is largest on the left outermost solder joint, and “top right plus bottom left”, which is largest on the right outside edge solder joint. The crack path lies in a deformation band as described from the FEM-analysis, and is located at the component side when there is little or no voiding within a joint, and on the PCB side for the CSPs mounted on microvias in pads, where there is strong voiding. Thus, microvia-induced void arrays seemingly attract the crack path location towards the void seating plane. As voids reduce the solder joint cross section in the crack path, the joint lifetime is reduced at least by the length covered by the void cross section. This may be counteracted by the decreased stiffness of the void-containing solder joints. The microsections showed one example where a lead-free solder joint was found completely cracked after 250 temperature cycles, with a void area of 15% as seen in transmission X-ray. This is far less than the 25% void area defined as acceptable by the IPC-A-610D standard. However, this void was found on a microvia and is as such not covered by the IPC-A-610D document.

The lead containing solder joints have practically reached the end of their lifetime after 500 temperature cycles. Solder joints located along the edge of the component were found cracked, no matter with or without voids. This degree of cracking was higher than that found in the lead-free solder joints. The reason for the earlier failure of the lead-containing solder joints is seen in part in the higher stiffness of the lead-free solder material. Due to the higher stiffness, the board deflection yields less creep deformation of

the lead-free solder joint within one temperature cycle. Less creep means less damage per cycle, and thus the higher number of cycles to fracture in comparison with the lead-containing solder joints. In this project, the cycle duration was chosen with two hours per cycle, which is more than the 30 minutes or one hour cycle duration normally applied by industry. However, as field cycle times may be ten hours or more, this may show a reduction of the cyclic lifetime of lead-free solder joints. Investigations on the impact of very slow cycles on the reliability of lead-free solder joints are still under way.



Important Names, Data, Events  
Annual Report 2006



## Lecturing Assignments at Universities

**H. Bernt:**  
Halbleitertechnologie I und II,  
Technische Fakultät der Christian-  
Albrechts-Universität, Kiel

**R. Dudde:**  
Semiconductor Devices –  
Physics and Technology,  
ESE 521, School of Engineers and  
Applied Science,  
University of Pennsylvania,  
Philadelphia, USA

**A. Heuberger:**  
Lehrstuhl für Halbleitertechnologie,  
Christian-Albrechts-Universität, Kiel

**B. Wagner:**  
Micro- and Nanosystem  
Technology I and II,  
Technische Fakultät der Christian-  
Albrechts-Universität, Kiel

## Memberships in Coordination Boards and Committees

**T. Ahrens:**  
Member of ELF NET (European  
Leadfree Network)

**T. Ahrens:**  
Coordinator of AOI-Anwenderkreis  
(Automated Optical Inspection)

**T. Ahrens:**  
Member of DVS Fachausschuss  
Löten

**T. Ahrens:**  
Member of Hamburger Lötzirkel

**W. H. Brünger:**  
Member of Steering Committee:  
Electron, Ion and Photon Beams  
and Nanofabrication, EIPBN, USA

**W. H. Brünger:**  
Member of VDI Fachausschuss:  
Maskentechnik, VDI, Düsseldorf

**W. H. Brünger:**  
Section Head: Micro and Nano  
Engineering, MNE 06, Barcelona

**W. H. Brünger:**  
Session Chair for Electron and Ion  
Beam Lithography 1, Micro and  
Nano Engineering, MNE 06,  
Barcelona

**Heuberger:**  
Advisory Editor of International  
Journal of Semiconductor  
Manufacturing Technology;  
Microelectronic Engineering

**Heuberger:**  
2. Chairman of an International  
Conference on Micro Electro,  
Opto, Mechanic Systems and  
Components

**J. Janes**  
Member at MEMUNITY, The MEMS  
Test Community

**K. Pape:**  
Member of VDI Fachausschuss  
Assembly Test, VDI, Frankfurt

**K. Pape:**  
Member of BVS, Bonn

**K. Pape:**  
Member of FED

**M. H. Poech:**  
Member of  
"Arbeitskreis Bleifreie Verbindungs-  
technik in der Elektronik"

**W. Reinert:**  
Speaker of working group "Wafer  
level packaging" in ZVEI

**W. Reinert**  
Member of Arbeitskreis A 2.4  
Drahtbondtechnik, DVS

**W. Reinert:**  
Member of DVS Fachausschuss  
Mikroverbindungstechnik

**M. Reiter:**  
Member of Gf Korr "Arbeitskreis  
Korrosionsschutz in der Elektronik"

**M. Reiter:**  
Member of "Arbeitskreis  
Lotpasten"

**M. Reiter:**  
Member of "Arbeitskreis Bleifreie  
Verbindungstechnik in der  
Elektronik"

**H. Schimanski:**  
Member of VDE/VDI Arbeitskreis  
"Prüftechniken in der  
Elektronikproduktion"

**G. Zwicker:**  
Head of Fachgruppe  
Planarisierung/Fachausschuss  
Verfahren/Fachbereich  
Halbleitertechnologie und -ferti-  
gung der GMM des VDE/VDI

**G. Zwicker:**  
Member of International Executive  
Committee of 2006 International  
Conference on Planarization/CMP  
Technology (ICPT)

**G. Zwicker**  
Opponent at the Public Defence  
of the Doctoral Thesis of Martin  
Kulawski, Technical University  
of Helsinki, Finland, October 20,  
2006

## Cooperation with Institutes and Universities

Rheinisch Westfälische Technische Hochschule, Aachen	Wehrwissenschaftliches Institut, Munster
Fachhochschule Anhalt	CSEM, Neuchâtel, Switzerland
Robert-Koch-Institut, Berlin	Sintef ICT, Oslo, Norway
Slovak Academy of Sciences, Bratislava, Slovakia	University of Oulu, Finland
Cambridge University, UK	University of Pavia, Italy
University of Cardiff, Great Britain	University of Pennsylvania, Philadelphia, USA
Technische Universität Dresden, Institut für Halbleiter- und Mikrosystemtechnik	University of Perugia, Italy
VTT, Espoo, Finland	Drexel-University, Philadelphia, USA
Universitätsklinikum Essen	University of Pisa, Italy
University of Exeter, Great Britain	National Inst. for NBC Protection, Pribram, Czech Republic
Fachhochschule Flensburg	TNO, Rijswijk, Netherlands
University of Gdansk, Poland	Royal Institute of Technology (KTH), Stockholm, Sweden
Ernst-Moritz-Arndt-Universität (EMAU), Greifswald	Swedish Defence Research Agency, Stockholm, Sweden
CEA Leti, Grenoble, France	IMS Chips, Stuttgart
Hochschule für Angewandte Wissenschaften, Hamburg	VTT, Technical Research Center of Finland, Tampere, Finland
Technische Universität Hamburg-Harburg	VDI/VDE-Technologiezentrum Informationstechnik, Teltow
Universitätskrankenhaus Eppendorf, Hamburg	LAAS-CNRS, Toulouse, France
Technion, Haifa, Israel	University of Twente, Netherlands
Fachhochschule Westküste, Heide	Universität Ulm
Technische Universität, Ilmenau	Uppsala University, Sweden
Christian-Albrechts-Universität, Technische Fakultät, Kiel	Centre d'Etude le Bouchet, Vert le Petit, France
Fachhochschule Köln	Plant Research International, Wageningen, Netherlands
MIMOS, Kuala Lumpur, Malaysia	University of Warsaw, Poland
École Polytechnique Fédérale de Lausanne, Switzerland	Fachhochschule Wedel
IMEC, Leuven, Belgium	

## Distinctions

**Timm-Florian Kraft**  
Distinction of being his year's top student in the final examination as a materials tester (specializing in semiconductor technology), for which he was awarded a prize by Fraunhofer board member Dr. Dirk-Meints Polter, München, December 5, 2006

## Trade Fairs and Exhibitions

### Sensor 2006

The Measurement Fair,  
May 30 – June 1, 2006 Nürnberg

### SMT Hybrid Packaging 2006

System Integration in Micro  
Electronics, Exhibition and  
Conference, May 30 – June 1,  
2006, Nürnberg

## Miscellaneous Events

### Aspekte moderner Siliziumtechnologie

Public lectures. Monthly presentations, ISIT, Itzehoe

### Der bleifreie Lötprozess in der Fertigung elektronischer Baugruppen

Seminar: February 21 – February 24 and October 10 – October 13, 2006, ISIT, Itzehoe

### Produktgestaltung: Aktuelles Design for Excellence

FED-Seminar: March 15, 2006, ISIT, Itzehoe

### Baugruppenfertigung mit Schwerpunkt im Lötprozess

FED-Seminar: March 16, 2006, ISIT, Itzehoe

### SMT-Rework-Praktikum – auch mit bleifreien Loten

Seminar: March 20 – March 22 and November 6 – November 8, 2006, ISIT, Itzehoe

### Manuelles Löten von SMT Bauelementen auch mit bleifreien Loten

Seminar: March 20 – March 22 and November 6 – November 8, 2006, ISIT, Itzehoe

### 16. CMP Users Meeting

April 7, 2006, Forum am Deutschen Museum, München

### Press conference "Bullith Batteries AG fusioniert mit dem Schweizer Unternehmen Leclanché".

Speakers: Dr Gerold Neumann (ISIT), Dr. Bernd Roß (Ministerium of Science, Economic Affairs and Transportation of Land Schleswig-Holstein), Dr. Christian Friedemann (Bullith Batteries), Armin Weiland (Leclanché, Bullith Batteries, Germancapital), April 21, 2006, Bullith Batteries, Itzehoe

### ISIT-Presentation for the Attachés for Science and Culture of the Embassies in Germany

Speaker: Dr. Wolfgang Windbracke, May 18, 2006, ISIT Itzehoe

### LEADFREE Praktikum/Fertigung elektronischer Baugruppen

Seminar: June 12 – June 16, 2006, ISIT, Itzehoe – FED-Fachverband Elektronik-Design e.V.

### ISIT Presentation at the Exhibition "Innovation & Wirtschaft" in the Framework of "Bürgerfest zum Tag der Deutschen Einheit 2006"

October 2 – October 3, Kiel

### 17. CMP Users Meeting

October 27, 2006, Fraunhofer IZM, Chemnitz

Opening of the exhibition "Deutscher Zukunftspreis: Aus Ideen Erfolge machen" with ISIT Contributions to the Subject Electrical Biochip Technology, by Federal President Horst Köhler  
December 19, 2006, Deutsches Museum, München

## Journal Papers and Contributions to Conferences

**J. Adam, M.-H. Poech:**  
Simulation der Leiterplatte im  
Reflow-Ofen.  
Tagungsband FED Konferenz, Kassel,  
September 21 – September 23,  
2006

**T. Ahrens:**  
Elektronikfertigung - Training zum  
Selbstkostenpreis.  
Elektronik Praxis, Sonderheft 5,  
p. 28 – 31, May, 2006

**T. Ahrens, O. Lawien, J. Quenzer:**  
Ein gläsernes Prüfmuster für die  
automatische Optische Inspektion  
in der Fertigung elektronischer  
Baugruppen.  
Schweißen und Schneiden 58,  
11/06, p. 550 – 558, 2006

**L. Bertels, W. Reinert:**  
UV-Blende erzeugt ein präzises  
Laserprofil – Intensitätsregelung  
schont Auge und Material.  
Laser+Photonik 1, p. 22 – 23,  
March 1, 2006

**A. Dietzel, W.-H. Brünger, H.  
Löschner, E. Platzgummer:**  
Micro- and Nano-Structuring Using  
Ion Beams.  
Proceedings of Second  
International Conference on Multi-  
Material Micro Manufacture,  
Grenoble, September 20 –  
September 22, 2006

**R. Dudde, Th. Vering, T.  
Piechotta, R. Hintsche:**  
Computer-Aided Continuous Drug  
Infusion: Setup and Test of a  
Mobile Closed-Loop System for the  
Continuous Automated Infusion of  
Insulin.  
IEEE Transactions on Information  
Technology in Biomedicine,  
Vol. 10, No. 2, p. 395 – 401, 2006

**R. Dudde, G. Piechotta, R.  
Hintsche:**  
Micromachined Amperometric  
Cells for Continuous Monitoring of  
Glucose and Lactate. Proceedings  
of the 1st Distributed Diagnosis  
and Home Healthcare (D2H2)  
Conference, Arlington, Virginia,  
USA, p. 1 – 4, 2006

**B. Elsholz, R. Wörl, L. Blohm, J.  
Albers, T. Grunwald, B. Jürgen, T.  
Schweder, H. Feucht, R. Hintsche:**  
Automated Detection and  
Quantitation of Bacterial RNA by  
using Electrical Microarrays  
Anal. Chem. 78, p. 4794 – 4802,  
2006

**D. Friedrich:**  
Mit Finetuning zu mehr Power.  
Elektronik und Entwicklung, May,  
2006

**P. Gulde:**  
Maßgeschneiderte Lithium-  
Polymer-Akkus – flexibel in Form  
und Größe.  
Design & Elektronik, p. 136 – 138  
October, 2006

**P. Gulde:**  
Tailor-made Lithium Polymer  
Batteries.  
Bodos Power-Systems, p. 44 – 45,  
October, 2006

**A. Heuberger, P. Merz, H. Christ:**  
Angular Rate and Motion Sensing  
with Smart Inertial Measurement  
Units.  
Proceedings of Trends in MEMS  
Congress, Munich, 2006

**H. Jacobsen, H.-J. Quenzer, B.  
Wagner, K. Ortner, Th. Jung:**  
High-Rate Sputtering of Thick PZT  
Layers for MEMS Actuators.  
Proc. Micro Electro Mechanical  
Systems MEMS, p. 214 – 217  
Istanbul, 2006

**B. Laborie, J. Souiller, M.  
Ennahali, M. Torkler, C. Huth, T.  
Lisec, G. Zwicker:**  
Development of a Custom-  
Designed Copper Slurry for the  
Fabrication of a RF-MEMS device.  
International Conference on  
Planarization/CMP Technology ICPT,  
Foster City, CA, USA, October,  
2006

**M. März, M.-H. Poech, E.  
Schimanek, A. Schletz:**  
Mechatronic Integration into the  
Hybrid Powertrain – The Thermal  
Challenge.  
International Conference AUTO-  
MOTIVE POWER ELECTRONICS –  
APE 2006, Paris, France,  
June 21 – June 22, 2006

**P. Merz:**  
Angular Rate and Motion MEMS  
Sensors for Smart Inertial  
Measurement Units.  
Proceedings of Electronica  
Automotive Congress, Munich,  
2006

**M. Moraja, G. Longoni, W.  
Reinert:**  
The role of the getter film in her-  
metically packaged MEMS resonant  
structures.  
2nd International Workshop on  
Wafer Bonding for MEMS  
Technologies, Halle, April 9 –  
April 11, 2006

**K. Ortner, D. Koeßler, T. Jung, H.  
Jacobsen, H.-J. Quenzer:**  
Influence of Bias Voltage on the  
Structure of Lead Zirconate  
Titanate Piezoelectric Films  
Prepared by Gas Flow Sputtering.  
10th Int. Conf. On Plasma Surface  
Engineering, Garmisch, 2006

**M.-H. Poech:**  
Volumeneffekte und technische  
Zuverlässigkeit bleifreier Lötstellen.  
Tagungsband FED Konferenz,  
Kassel, September 21 –  
September 23, 2006

**W. Reinert:**  
Vakuum-Bonding-Technologie für  
langzeitstabile Drehratensensoren.  
MST Mikrosystemtechnik 01,  
p. 30-32, April, 2006

**W. Reinert:**  
Vacuum Bonding Creates stable  
IMU's.  
Advanced Packaging, p. 24 – 26  
March, 2006

**W. Reinert:**  
Industrial Wafer Level Vacuum  
Encapsulation of Resonating MEMS  
Devices.  
DTIP 2006, Stresa, Italy, April 26 –  
April 28, 2006

**W. Reinert, D. Kähler, P. Merz:**  
Critical Leak Rate Screen on Wafer  
Level for the Vacuum Lifetime  
Prediction in Nano Liter MEMS  
Packages.  
KGD Workshop Packaging & Test  
Workshop, Nappa (CA),  
September 10 – September 13,  
2006

**C.G.J. Schabmüller, D. Loppow,  
G. Piechotta, B. Schütze, J.  
Albers, R. Hintsche:**  
Micromachined Sensor for Lactate  
Monitoring in Saliva.  
Biosensors and Bioelectronics 21,  
p. 1770 – 1776, 2006

**R. Schmidt, U. Pape, T. Ahrens:**  
Oberflächeneffekte von  
Komponenten zum bleifreien  
Löten. Schweißen und Schneiden  
58, 11/06, p. 620, 2006

## Talks and Poster Presentations

- T. Ahrens:**  
Lötqualität – Lötmetallurgie, Lötfläche, Flussmittel.  
Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen  
ISIT, Itzehoe, February 21 and October 10, 2006
- T. Ahrens:**  
Baugruppen- und Fehlerbewertung – Inspektionskriterien, bleifreie Lötstellen.  
Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen  
ISIT, Itzehoe, February 22 and October 11, 2006
- T. Ahrens:**  
Fertigungsgerechtes Design – Passmarken, Pads, Freiräume, Symmetrien.  
Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen  
ISIT, Itzehoe, February 23, 2006
- T. Ahrens:**  
Was wird anders durch bleifreies Löten.  
Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen  
ISIT, Itzehoe, February 23, 2006
- T. Ahrens:**  
Neue Trainingslinie für bleifreie/RoHS-konforme Elektronikfertigung in Itzehoe.  
Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, March 1, 2006
- T. Ahrens:**  
DfX: Designprinzipien – Null-Fehler-Strategie, Bauteil-Verfügbarkeit: Chancen durch Redesign & Bleifrei.  
Seminar: Produktgestaltung: Design for Excellence, ISIT, Itzehoe, March 15, 2006
- T. Ahrens:**  
Fertigungsgerechtes Baugruppen-Design – Standards für Padlayout, Lotpastendruck, Bestückung, Lötwärmebedarf, Bleifrei.  
Seminar: Produktgestaltung: Design for Excellence, ISIT, Itzehoe, March 15, 2006
- T. Ahrens:**  
Verantwortung im Design – Einbau der Zuverlässigkeit, Betriebsbelastung, Materialkombinationen, Anforderungen an Bauteile und Leiterplatten, Entwärmung.  
Seminar: Produktgestaltung: Design for Excellence, ISIT, Itzehoe, March 15, 2006
- T. Ahrens:**  
Bleifrei Reparaturlöten – Lote, Flussmittel, Löttemperatur und Wärmebeständigkeit der Materialien.  
Seminar: Manuelles Löten von SMT-Bauelementen auch mit bleifreien Loten,  
ISIT, Itzehoe, March, 20 and November 6, 2006
- T. Ahrens:**  
Baugruppen- und Fehlerbewertung – Inspektion, Röntgenverfahren, Querschleife.  
Seminar: Manuelles Löten von SMT-Bauelementen auch mit bleifreien Loten.  
ISIT, Itzehoe, March 20, and November 6, 2006
- T. Ahrens:**  
Bleifreies Handlöten.  
9. Europäisches Elektroniktechnologie-Kolleg, Colonia de Sant Jordi, March 22 – March 26, 2006
- T. Ahrens:**  
Implementation of European Environmental Legislation in SME, or Demonstration and Training Lead-Free Soldering for European Industry in Order to Promote Environmental Friendly Electronic Production.  
IPC/Soldertec Global 4th International Electronics Conference and Exhibition "RoHS Compliance and Beyond", Malmo, Sweden, April 25 – April 27 April, 2006
- T. Ahrens:**  
Exploring the RoHS Directive and the Impact of Lead-Free Soldering Requirements on Polymer Selection.  
Automotive Electronics & Electrical Systems, Stuttgart, May 16 – May 17, 2006
- T. Ahrens:**  
RoHS-konforme Baugruppen fehlerfrei und produktiv produzieren.  
14. FED-Konferenz, Kassel, September 21 – September 23, 2006
- T. Ahrens:**  
Equipment, Procedures and Process Limits for Leadfree Soldering.  
17th ESREF, Wuppertal, October 3 – October 6, 2006
- T. Ahrens:**  
Handlöten.  
Seminar: Weichlöten – die wichtigste Verbindungstechnologie in der Elektronik, Würzburg, November 27 – November 28, 2006
- T. Ahrens:**  
Fallstudien bleifreies Löten – Konstruktion, Prozess und Materialauswahl.  
Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen,  
ISIT, Itzehoe, October 12, 2006
- L. Blohm:**  
Neue Analysegeräte für die elektrische Biochiptechnologie.  
Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, June 07, 2006
- W. H. Brünger:**  
Ion Projection Direct Structuring at Surfaces.  
Seminar Talk at IBM – Almaden Res. Center, San José, October 6, 2006
- W. H. Brünger:**  
Ion Projection Direct Treatment of Surfaces.  
Talk at MRS-Fall-Meeting, Boston (Ma.), USA, November 27 – December 1, 2006
- R. Dudde, G. Piechotta, R. Hintsche:**  
Micromachined Amperometric Cells for Continuous Monitoring of Glucose and Lactate.  
1st Distributed Diagnoses and Home Healthcare (D2H2) Conference, Arlington, Virginia, USA, 2006
- J. Eichholz:**  
Microsensors and User Interfaces for Mobile Services and Applications.  
MIMOSA/ECUBES Workshop as Satellite of ESSDERC, ESSCIRC, Montreux, September 22, 2006
- J. Eichholz:**  
Entwicklung eines programmierbaren Apertur Platten Systems zur Verwendung in maskenlosen 45 nm e-Beam Lithographiegeräten.  
Microelectronics Workshop at IMTEK, Freiburg, December 19, 2006
- D. Friedrich:**  
Neuartige Verfahren für die Herstellung dünner Leistungsbaulemente.  
Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, April 05, 2006
- D. Friedrich:**  
From Discrete Power Devices to Power Systems.  
10. Jahrestag Fraunhofer-Mikroelektronik-Verbund, CNT, Dresden, June, 2006
- H. Jacobsen:**  
Integration von piezoelektrischen Keramiksichten in den Herstellungsablauf der Silizium-Mikrosystemtechnik.  
Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, March, 1, 2006
- J. Janes:**  
Weisslicht-Interferometrie an Poly-Si Strukturen.  
Fraunhofer-IWM, Halle, March 2, 2006
- J. Janes:**  
Indicators for Waferlevel MEMS Tests: Workshop Fraunhofer-IWM, Halle, March 14, 2006
- J. Janes:**  
Gyro Function Control.  
Anwendertreffen Partest, X-Fab, Erfurt, October 5, 2006
- J. Janes:**  
MEMS Development & Function Control.  
Fraunhofer-IZM, Chemnitz, November 8, 2006

## Diploma Theses

- Y. Karade, K. Graf, W.H. Brünger, A. Dietzel, R. Berger:**  
Controlled Sub-Micrometer Surface Morphologies by Thermal Relaxation of Locally Crosslinked Stretched Polymers.  
MNE, Barcelona, September 17 – September 20, 2006
- B. Laborie, J. Souiller, M. Ennahali, M. Torkler, C. Huth, T. Lisec, G. Zwicker:**  
Development of a Custom-Designed Copper Slurry for the Fabrication of a RF-MEMS Device.  
17. CMP User Meeting, Fraunhofer IZM, Chemnitz, October 27, 2006
- P. Lange:**  
Massenfluss-Sensoren in verschiedenen Anwendungen.  
Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, December 6, 2006
- T. Lisec:**  
Mikrosysteme für Hochfrequenz-Anwendungen und mobile Kommunikation.  
Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, September 6, 2006
- M.-H. Poech:**  
Das Reflow-Lötprofil – Temperaturverteilung in der Baugruppe.  
Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, February 21 and October 10, 2006
- M.-H. Poech:**  
Zuverlässigkeit von Lötstellen – Schadensmechanismen, beschleunigte Tests.  
Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, February 23 and October 12, 2006
- M.-H. Poech:**  
Thermomechanik der Baugruppe – Ergebnisse aus dem AiF Projekt "Volumeneffekte".  
EUREKA Workshop, ISIT, Itzehoe, February 6 - February 7, 2006 and EUREKA Treffen, ISIT, Itzehoe, April 11, 2006
- M.-H. Poech:**  
Temperaturmessungen und -Profile.  
Rehm Technologietag, Blaubeuren, March 9, 2006
- M.-H. Poech:**  
Schädigungsmechanismen in bleifreien und bleihaltigen Lötverbindungen bei erhöhter Temperatur.  
1st Reliability Convention, RMCtech, Hamburg, March 23, 2006
- M.-H. Poech:**  
Mechanisches Verhalten bleifreier Lötstellen.  
Arbeitskreis Pb-frei, Fraunhofer IZM, Berlin, September 5, 2006
- M.-H. Poech:**  
Matching Soldering Method and Thermal Design.  
ECPE Seminar and Training "LEADFREE Soldering for Power Electronics Manufacturing", ISIT, Itzehoe, September 14 – September 15, 2006
- M.-H. Poech:**  
Solder Joint Reliability.  
ECPE Seminar and Training "LEADFREE Soldering for Power Electronics Manufacturing" ISIT, Itzehoe, September 14 – September 15, 2006
- M.-H. Poech:**  
Volumeneffekte und technische Zuverlässigkeit bleifreier Lötstellen.  
FED-Konferenz, Kassel, September 21 – September 23, 2006
- M.-H. Poech, J. Adam:**  
Simulation der Leiterplatte im Reflow-Ofen.  
FED-Konferenz, Kassel, September 21 – September 23, 2006
- H.-J. Quenzer:**  
Innovative Verfahren zur Strukturierung mikrooptischer Elemente aus Glas.  
Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, November, 1, 2006
- K. Reiter, M. Reiter:**  
GRÜNE ELEKTRONIK: Material- und Fehleranalyse an bleifreien Lötverbindungen.  
Metallographietagung, Leoben, September 27 – September 29, 2006
- M. Reiter:**  
Bewertung bleifreier Baugruppen.  
Erstes Seminar für aktuelle Trends in der Aufbau- und Verbindungstechnologie (Zevac, Speedline, Koenen), Eisenach, March 30 – March 31, 2006
- H. Schimanski:**  
Qualitätsfaktor Leiterplatten – Prüfmethode, -standards, Ausfallbeispiele.  
Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen ISIT, Itzehoe, February 22 and October 11, 2006
- H. Schimanski:**  
Rework-Strategien für bleifreies Löten.  
OTTI Profiforum, Produktion bleifreier elektronischer Baugruppen, Regensburg, April 5 – April 6, 2006
- H. Schimanski:**  
Einsatz, Rework und Zuverlässigkeit bleifreier BGA in der Übergangsphase.  
14. FED-Konferenz, Kassel, September 21 – September 23, 2006
- H. Schimanski:**  
Reparatur bleifreier BGAs in der Übergangsphase.  
International User Meeting, Finetech GmbH & Co. KG, Berlin, September 28, 2006
- G. Zwicker:**  
MEMS Fabrication by Using CMP-Activities at Fraunhofer ISIT.  
VTT, Espoo, Finland, October 19, 2006
- K. Baum:**  
Aufbau eines Twyman-Green Interferometers zur Vermessung von Mikrolinsen.  
Fachhochschule Köln, July, 2006
- K. Dannenberg:**  
Weiterentwicklung eines halbautomatischen Vakuumprobiermessplatzes zur Charakterisierung von Drehratensensoren auf Waferebene.  
Fachhochschule Wedel, February, 2006
- M. Melzer:**  
Untersuchungen zur Fine Pitch Lotaufbringung für die Flip-Chip Montage durch Bekugelung und Lotpastendruck.  
Fachhochschule Anhalt, July, 2006
- V. Nörenberg:**  
Entwicklung einer Softwareanwendung und Aufbau einer relationalen Datenbank zur automatischen Archivierung umfangreicher Messdaten von Drehratensensoren.  
Hochschule für Angewandte Wissenschaften, Hamburg, August, 2006
- B. Thun:**  
Standardisierung und Optimierung von Mikroarrays basierend auf elektrischen Biochips.  
Fachhochschule Flensburg, February, 2006
- V. Viertel:**  
Optimierung von Assays auf elektrischen Biochips mit Trockenchemikalien.  
Fachhochschule Flensburg, February, 2006
- T. Weber:**  
Untersuchung der dynamischen elektrischen Eigenschaften von Trench-IGBTs in Abhängigkeit von unterschiedlichen Messbedingungen.  
Technische Universität Hamburg-Harburg, March, 2006

## Overview of Projects

- Stand-Off Development for RF High Precision Capacitors
- Development and fabrication of RF High Precision Capacitors
- Process Development for Electrostatic Carriers
- Engineering and Developments for a WLCSP Production
- Support for Build Up a 0,8 µm CMOS Technology
- Support for Build Up a 0,35 µm CMOS Technology
- Development of a Lead Free Sn-Ag Galvanic for WLCSP
- Feedthrough and Wrap Around for Power Devices
- Super Junction PowerMOS
- Ultrathin Trench IGBTs on sub-100 µm Si-Substrates
- Carbon Nanotube Devices for Integrated Circuit Engineering
- BCB evaluation for PowerMOS devices
- Entwicklung von Post-CMP-Reinigungsprozessen für die Fertigung von zukünftigen integrierten Schaltkreisen in der Si-Technologie
- Evaluierung von Slurries zum chemisch-mechanischen Polieren von SiO<sub>2</sub>
- Untersuchung der Poliereigenschaften verschiedener TiO<sub>2</sub>-Dispersionen für Oxid-CMP (STI) und mono-Si-CMP
- Untersuchung von Ceroxid-Dispersionen für CMP
- Untersuchung an mikromechanischen Drehraten-Sensoren
- Entwicklung von kapazitiven HF-Schaltern
- Entwicklung von piezoelektrischen Schichten für Si-Mikroaktuatoren
- Herstellung mikrooptischer Linsenarrays aus Glas
- Microsystems Platform for Mobile Service and Applications – MIMOSA
- AMICOM: Advanced MEMS for RF and Millimeter Wave Communications, Network of Excellence
- P-ML 2, Projection Maskless Lithography; Development of an Aperture Plate System
- Entwicklung von Messstrategien zur Evaluierung von Parametern für MEMS Design
- Mikroskann-Systeme für Display Anwendungen
- Mikrotechnische Fabrikation von Laserresonator Spiegeln
- Charged Particle Nanotech, CHARPAN
- Radical Innovation Maskless Nanolithography, RIMANA
- Mikrosystemtechnische Laserprojektion zur informativischen Fahrerassistenz, MICLAS
- Study on Silicon MEMS Force Sensors, SMErobot
- Probebased terabit memory. PROTEM
- Generic Manufacturing and Design Technology Platforms Based on Novel RF Technologies, RF-PLATFORM
- Customer Support and Design Centre for Physical Measurement Systems, EURO PRACTICE CCMesys
- Microactuator Competence Centre, EURO PRACTICE CCMicro
- Innovative Measures for Protection against CBRN Terrorism, IMPACT
- Electrical Bio Sensor Arrays for Analyses of Harmful Micro Organisms and Microbial Toxins, eBiosense
- Genotype-Specific Hepatitis C Diagnostic Chip, HCV
- Entwicklung biochemischer Erkennungssysteme für portable elektrische Detektionssysteme von Biowaffen-Toxinen
- Elektrischer DBD-ISIT-eBS-Array-Immundetektor: Beratung, Bereitstellung und Spotten von Mikrochips für den Toxin-nachweis, Service
- Analysesystem für die markergestützte intraoperative Tumordiagnostik
- Chipkartenbestückung mit Grautonblenden
- Ultra-Thin Packaging Solutions using Thin Silicon
- Flip Chip Die Bonder for Ultra-Thin Silicon
- Stressoptimierte Montage und Gehäusetechnik für mikro-mechanisch hergestellte Silizium-Drehratensensoren
- Glassfritt Vacuum Wafer Bonding
- Glaslotbonden mit strukturierten Capwafern und Musterwafern
- Assembly Test on PCB
- Automotives Mikrokamerasystem für Fahrzeugumfelderfassung, µ-CAM
- Downscaled Assembly of Vertically Interconnected Devices, DAVID
- Pan-Mobile Erfassung mit optimierten Smart-Labels zur Effizienzsteigerung von Logistikprozessen, PESEL
- Wafer Level Packaging
- Wafer Level Balling for 100 µm up to 500 µm Spheres
- Customer specified test wafers
- Neon ultra fine leak test for resonant micro sensors
- Volumeneffekte und technische Zuverlässigkeit von bleifreien Lötstellen
- Bewertung von Aufbaukonzepten für ein Leistungsmodul
- Qualitätsbewertung an bleifreien Baugruppen
- Demonstration and Training Lead-Free Soldering for European Industrie, LIFE
- Hearing – Aids with Rechargeable Power Supply, HARPOS
- Micro-Nano Integrated Platform for Transverse Ambient Intelligence Applications, MINAMI

## Patents

**P. Birke, G. Neumann**

Pastöse Massen mit nanokristallinen Materialien für elektrochemische Bauelemente und daraus hergestellte Schichten und elektrochemische Bauelemente  
DE 199 48 548 B4

**P. Birke, G. Neumann**

Paste-like mass with inorganic, liquid conductors and layers and electrochemical elements  
ID 0 015 473

**P. Birke, F. Salam**

Films for electrochemical components and a method for production thereof  
ZL 00816413.4

**J. Eichholz**

Control Circuit for Controlling an Electron-Emitting Device  
US 7,095,186 B2

**H. Futscher, G. Neumann**

Verfahren zur Herstellung von beschichteten Streckmetallen und Verwendung solcher Metalle als Stromableiter in elektrochemischen Bauelementen  
EP 1 570 113 B1

**R. Hintsche**

Sensor für die Detektion von Inhaltsstoffen von Flüssigkeiten, insbesondere biologischer Materialien, und diesen Sensor enthaltene Detektionsvorrichtung  
DE 10 2004 020 829 B4

**U. Hofmann, M. Witt,  
B. Wagner, S. Mühlmann**

Verfahren zur Herstellung eines Mikroaktorbauteils  
DE 199 41 363 B4

**T. Lisec, H.-J. Quenzer, B. Wagner**

Mikrosensoranordnung zur Positionsmessung von Flüssigkeiten in Kapillaren  
DE 199 44 331

**T. Lisec, P. Merz**

Sensorchip für einen Differenzdrucksensor mit beidseitigem Überlastungsschutz  
DE 102 49 238 B4

**G. Neumann, P. Birke**

Pastöse Massen mit nanokristallinen Materialien für elektrochemische Bauelemente und daraus hergestellte Schichten und elektrochemische Bauelemente  
EP 1 194 963 B1

**H.-J. Quenzer, W. Reinert**

Strahlformungselement für optische Strahlung sowie Verfahren zur Herstellung  
EP 1 407 520

**H.-J. Quenzer, P. Merz, M. Oldsen, W. Reinert**

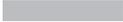
Verfahren zum Erzeugen eines vorgegebenen Innendrucks in einem Hohlraum eines Halbleiterelements  
DE 10 2005 001 449 B3

**R. Sittig, D. Nagel, R. Dudde,  
B. Wagner, K. Reimer**

Optimierter Randabschluss von Halbleiter-Bauelementen  
DE 198 81 806

**B. Wagner, H.-J. Quenzer, X. Tuo**

Tuneable High-Frequency Capacitor  
ZL 00817102.5

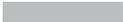


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