

FRAUNHOFER-INSTITUT FÜR SILIZIUMTECHNOLOGIE ISIT

**Achievements  
and Results  
Annual Report**

**2008**



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and Results  
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*ISIT's new Managing Director Prof. W. Benecke*

***Dear business partners,  
friends of the ISIT and colleagues,***

System solutions attain a new quality by combining existing and new technologies. Following this principle of “More than Moore” the ISIT has been able to further expand and strengthen its position in the Institute's core areas of activity. Despite particular and unusual challenges, including the global credit crunch, the ISIT closed the fiscal year with a very pleasing positive result.

**This annual report can only provide an overview of the Institute's activities and not all the results achieved and work performed can be properly depicted.**

The general need for intelligent and efficient use of electricity has led to numerous new projects and project initiatives at the ISIT in the areas of power electronics and energy storage. In the SuperpowerMOS project, new types of energy-efficient power electronic components are being developed in the voltage range up to 400 V. In cooperation with universities and local industry in Schleswig-Holstein, the power electronic expert group is working on innovative converter concepts for the low voltage range. Cooperation with Vishay Siliconix Itzehoe GmbH continues to take a very positive course and has also been contractually secured for the long term. The development of Li-Ion accumulators is currently progressing at a rapid pace, with electromobility and electric vehicle technologies in the forefront. Numerous projects have been contracted with prominent industrial partners. The procurement of a film coating unit for battery development is being prepared in connection with the current federal economic stimulus programs 1 and 2, so that professional prototype series production of Li-Ion rechargeable batteries will be possible in future.

The constantly growing demand for MEMS-based sensors and actuators has opened up interesting cooperation opportunities

for the Microsystems Technology Department, which are also important for the Institute as a whole. In collaboration with SensorDynamics AG Itzehoe, the processes for the production of high-precision inertial sensors have been further stabilized and successfully transferred to 200-mm wafer technology.

More progress has been made in the wafer level packaging (WLP) projects, which are being conducted with significant input from the Module Integration Department, and as a result this technology can be regarded as leading the way worldwide. WLP technology has been successfully deployed for the production of RF-MEMS components. The first thin wafer stacks with a total thickness of 400  $\mu\text{m}$  were successfully qualified. Transfer of the process to 200-mm wafer technology and process qualification have advanced so far that the customer is already preparing for high-volume production.

A new generation of micromirror scanners has been created, with which new functionalities have been achieved using a vacuum packaging process through the consistent use of WLP technologies. The work contributed by the IC Design Department is also proving very successful as it is providing important input for the development of complete systems and modules.

For the production of IR sensor arrays, a WLP process has been successfully deployed on the 150-mm wafer technology platform and preparations are now starting for pilot production at the ISIT. In the area of module integration, significant new developments have begun for embedding in chips on printed circuit boards. They create the basis for generations of innovative intelligent PCBs. In addition to the aforementioned collaborative projects with Vishay and SensorDynamics, cooperation with the firm of Peter Wolters in the field of CMP



*Dr. Gustav Sauer, Director Dpt. „Technologie und Entwicklung“, Ministry of Economy, Kiel, discussing with Fraunhofer Board Member Prof. Ulrich Buller at ISIT, 26.6.08*

has also been further strengthened and expanded. The same is the case for business relations with the companies Plan Optik and AJ eBiochip. All these companies maintain permanent working groups at the site, which cooperate closely with the ISIT's departments.

Particular strategic importance for future technological capabilities of ISIT attaches to the expansion of the Institute and the technology switchover to a 200-mm (8") wafer platform. In the project set up to create a center of expertise

for large wafers, € 10.4 million is being invested by the state of Schleswig-Holstein (75 %) and the Fraunhofer-Gesellschaft to convert the existing technology and buy new plant and equipment. Progress has been made with the planning of ISIT expansion through construction of a further cleanroom, laboratory and office building, which represents the consistent advancement of the previously described project. Through the positive decisions taken by the Executive Board of the Fraunhofer-Gesellschaft, the Fraunhofer Senate and the Fraunhofer Committee of the Federal and State Governments

*ISIT-Organigramm*





*ISIT-Deputy Director Dr. Wolfgang Windbracke*

in October and November, the project is progressing well. The plans for implementation have now been started in concrete terms. About € 37 million will be invested in the new building and equipment for the expansion of the Institute. The state of Schleswig-Holstein is contributing the biggest share, meeting more than € 27 million of the expenditure. Around € 9 million is being provided from central funds of the Fraunhofer-Gesellschaft. At this point I would like to express my thanks to Mr. Austermann in particular for his efforts towards the expansion of the technological base at Itzehoe.

With its expanded facilities and access to 200-mm wafer technology, the ISIT will further strengthen its position in the field of micro/nanosystems. In important segments the ISIT will also achieve a unique position in global competition. The expansion measures will be conducted in such a way that the technology will be oriented to industrial standards and as a result research and development will take place in an environment similar to industrial production. Given the long-term nature of pre-competitive research, the ISIT will be working even more closely with universities and colleges in the state of Schleswig-Holstein.

Active cooperation is already underway in many projects. Collaborative efforts are being further strengthened in particular with the University of Kiel (Christian-Albrechts-Universität, CAU) and especially with its Faculty of Engineering. An excellent basis for cooperation has already been established through my joint responsibilities as institute director and chair-holder at CAU and the great interest shown by colleagues at the university. There are wide-ranging areas of common interest in electrical engineering and the materials sciences, which will be additionally supported by the creation of a permanent ISIT working group at the university's engineering faculty.

I became director of the ISIT on October 1 and I would like to take the opportunity at this point to express my sincere thanks to all staff and colleagues for their very open and kind reception. I would also like to thank the Executive Board of the Fraunhofer-Gesellschaft, the Institute's supervisor Dr. Gerd Wöhl, the governing board of the University of Kiel and my colleagues in the university's Faculty of Engineering for the confidence they have shown me and the constructive and efficient appointment procedure. My special thanks go to Dr. Wolfgang Windbracke who acted with utmost commitment as interim director of the ISIT and thus laid the foundations for the success of the Institute. I am delighted that he will continue to shape the development of the Institute together with me in future. I would also like to express my gratitude to Dr. Bernd Wagner in the same respect, and also to Prof. Heuberger, who did so much to pave the way for the present standing of the ISIT.

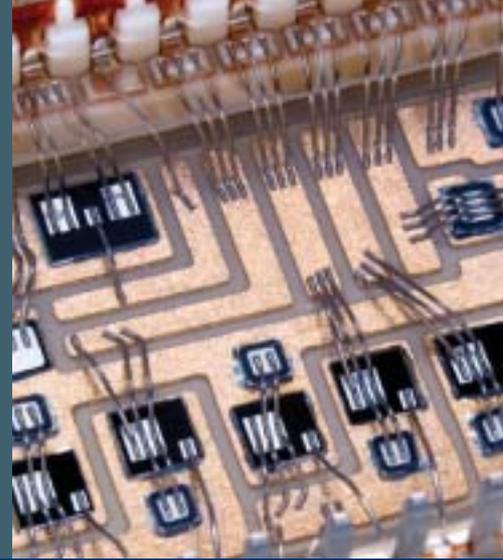
In conclusion, I would like to thank all cooperation partners for their trust and confidence. All representatives of the state of Schleswig-Holstein, the federal government, the Fraunhofer-Gesellschaft and the Board of Trustees of the ISIT have my gratitude for their benevolent, frank and constructive support in the various measures and projects. The employees of the Institute deserve special mention for the excellent commitment and motivation they display in their daily work in order to present optimal results to customers.

The ISIT is in a good position to face the challenges of the future. Please do not hesitate to get in touch with us.

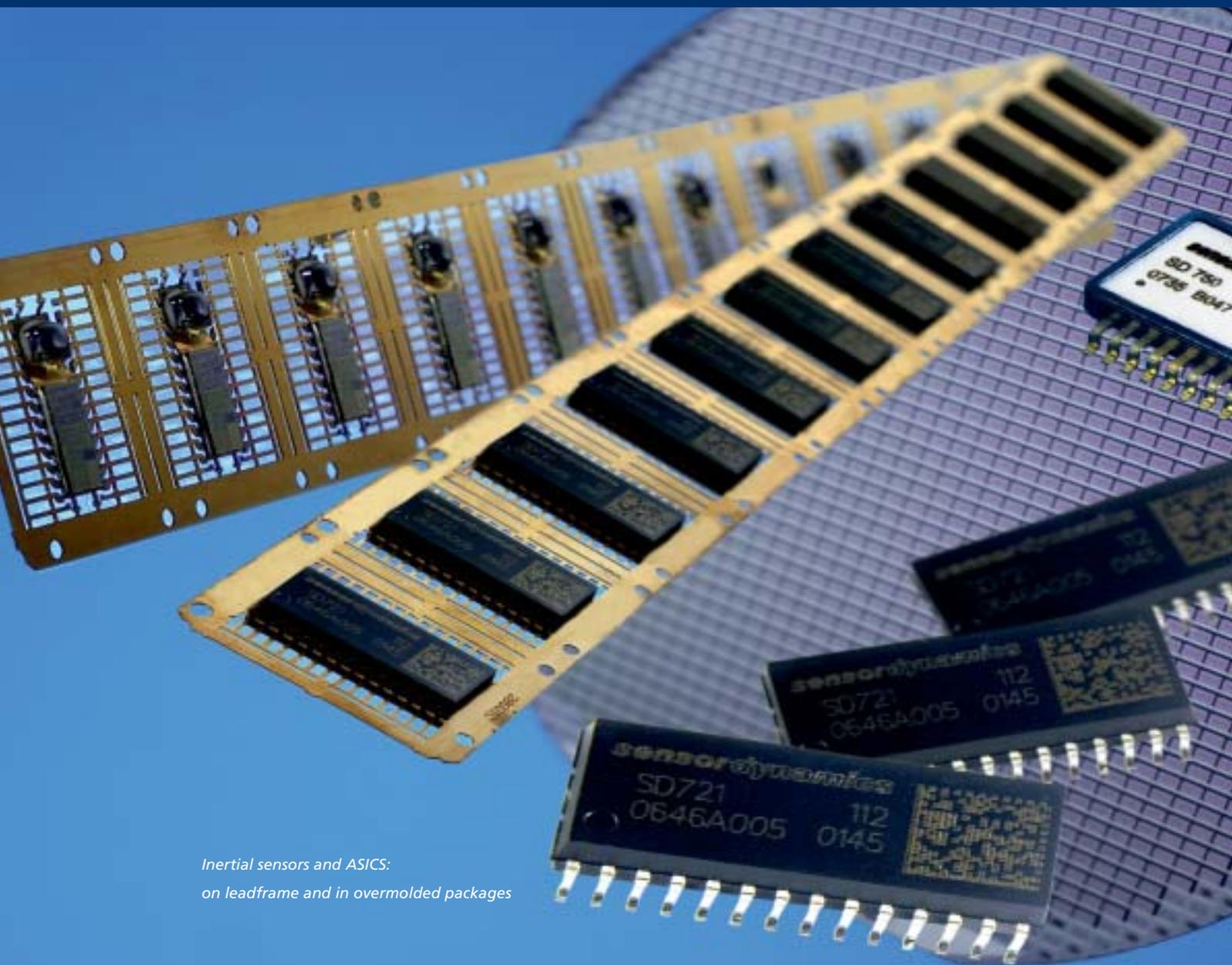
**We will listen to your wishes and ideas and provide straightforward, expert advice. We look forward to your visit and to working with you.**



*ISIT cleanroom: CMP section*



*Power module with IGBTs and diodes*



*Inertial sensors and ASICs:  
on leadframe and in overmolded packages*



*Fraunhofer ISIT in Itzehoe:  
cleanroom and office building*

## FRAUNHOFER-INSTITUT FÜR SILIZIUMTECHNOLOGIE (ISIT)

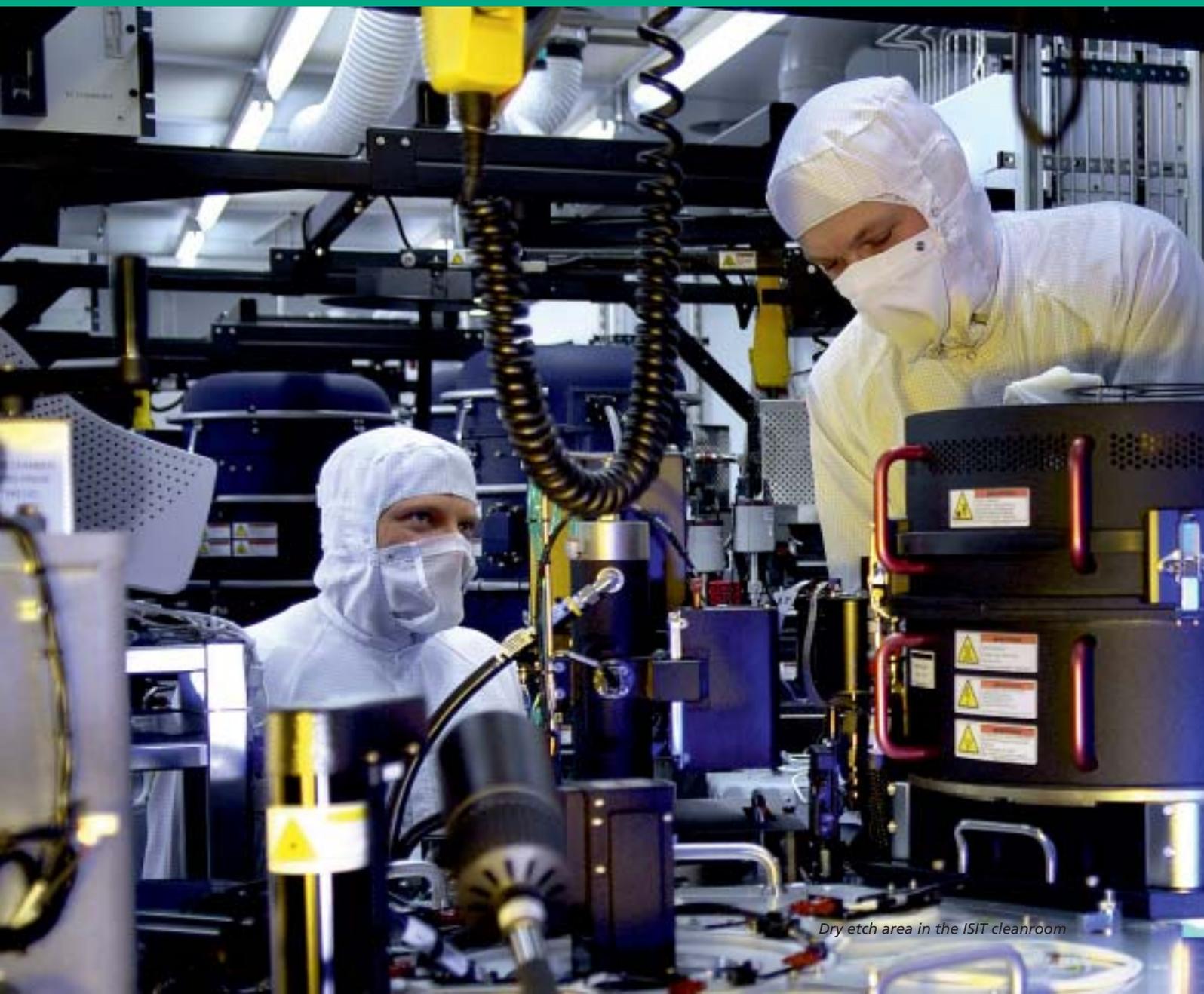
### Research and Production at one Location

Fraunhofer ISIT develops and manufactures components in microelectronics and microsystems technology, from the design phase – including system simulation – to prototyping and fabrication of samples, up to series production. Even though components, manufactured at Fraunhofer ISIT such as acceleration sensors, valves, and deflection mirrors often measure just a fraction of a millimeter in size, there is a wide range of applications: the devices are implemented in areas like medical care, environmental and traffic engineering, communication systems, automotive industry, and mechanical engineering. Working under contract, ISIT develops these types of components in accordance with customer requirements, also creating the applicationspecific integrated circuits (ASICs) needed for the operation of sensors and actuators. Included in this service is the system integration using miniaturized assembly and interconnection technology.

Together with Vishay Siliconix Itzehoe GmbH, the institute operates a professional semiconductor production line which is up-to-date in all required quality certifications (e. g. ISO 9001, TS 16949). This line is used in parallel for PowerMOS and microsystem production and for R&D projects developing new devices and technological processes.

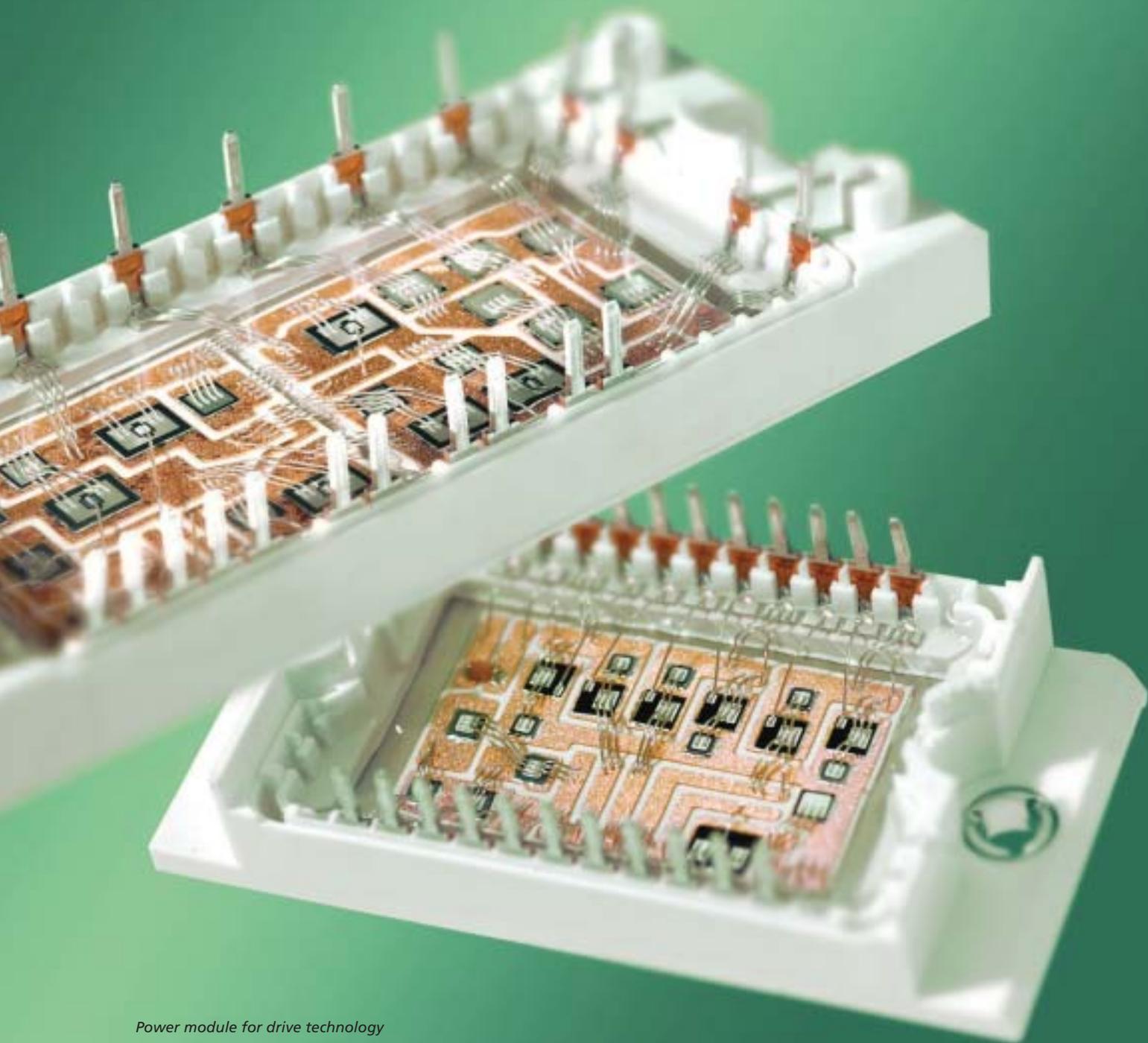
Other fields of activity at ISIT focus on assembly and packaging techniques for microsystems, analysis of the quality and reliability of electronic components, and development of advanced power-supply components for electronic systems. The institute employs a staff of around 150 people.

## MAIN FIELDS OF ACTIVITY

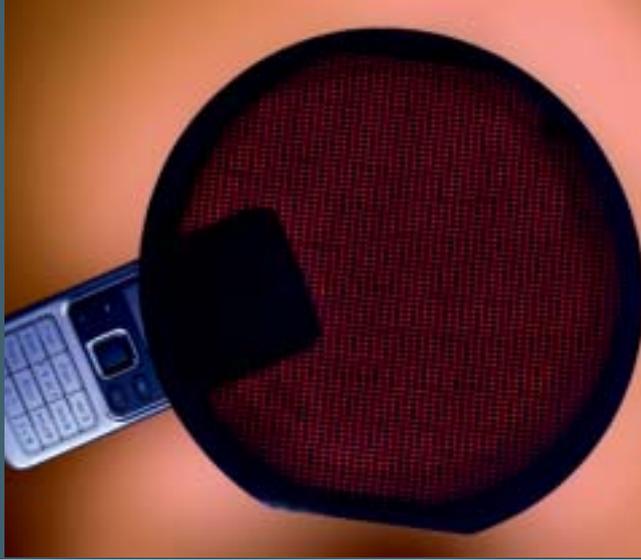


*Dry etch area in the ISIT cleanroom*

## MAIN FIELDS OF ACTIVITY



*Power module for drive technology  
(Danfoss Silicon Power)*



*PowerMOS wafer thinned by  
TAIKO process to 20  $\mu\text{m}$*



*IGBT power module assembly  
based on power balling*

## IC TECHNOLOGY AND POWER ELECTRONICS

The power electronics and IC technology group develops and manufactures active integrated circuits as well as discrete passive components. Among the active components the emphasis lies on power devices such as smart power chips, IGBTs, bi-directional components, PowerMOS circuits and diodes. Thereby ISIT primarily uses Vishay's customized, individual production sequences. Additional support for work in this area is provided by a number of tools for simulation, design and testing. ISIT also benefits from years of experience in the design and manufacturing of CMOS circuits. The development of new processes for advanced power device assembly is a further important research topic.

The passive components developed and fabricated at ISIT are primarily chip capacitors, precision resistors and inductors. Materials development and the integration of new materials and alloys into existing manufacturing processes play an important role in the development process.

ISIT develops individual processes, process modules and complete process flows for diverse applications. The institute also offers customer-specific silicon components processing in small to medium-sized quantities on the basis of a qualified semiconductor process technology.

To support the development of new semiconductor production techniques, production equipment of particular interest is selected for testing and optimization. This practice provides the institute with specialized expertise in challenges related to etching, deposition, lithography, and planarization methods.

Planarization using chemical-mechanical polishing (CMP) in particular is a key technology for manufacturing advanced integrated circuits and microsystems. The intensive work done

by ISIT in this area is supported by a corresponding infrastructure. A special emphasis lies in the application of CMP for the manufacturing of MEMS devices and microsystems.

The institute's CMP application lab is equipped with CMP cluster tools, single- and double-sided polishers and post-CMP cleaning equipment for wafers with 100 to 300 mm in diameter. The CMP group at ISIT works in close relationship to Peter Wolters AG since many years, as well as other semiconductor fabrication equipment manufacturers, producers of consumables, CMP users and chip and wafer manufacturers.

The CMP group's work encompasses the following areas:

- Testing of CMP systems and CMP cleaning equipment
- Development of CMP processes for
  - Dielectrics ( $\text{SiO}_2$ , TEOS, BPSG, low-k, etc.)
  - Metals (W, Cu, Ni, etc.)
  - Silicon (wafers, poly-Si)
- Testing of slurries and pads for CMP
- Post-CMP cleaning
- CMP-related metrology
- Implementation of customer-specific polishing processes for ICs and microsystems.

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## MAIN FIELDS OF ACTIVITY



*Wafer-level vacuum packaged  
MEMS scanning mirrors*

# MICROSYSTEMS TECHNOLOGY (MEMS) AND IC DESIGN

Microsystems technology is a core activity at the institute, an area which ISIT has pioneered in Germany. For over 20 years ISIT scientists have been working on the development of micromechanical sensors and actuators, micro-optics, and components for radio-frequency applications (RF-MEMS). Their work in this area also includes integrating these components with microelectronics to create small-size systems of high functionality. A multitude of components and systems have originated at ISIT.

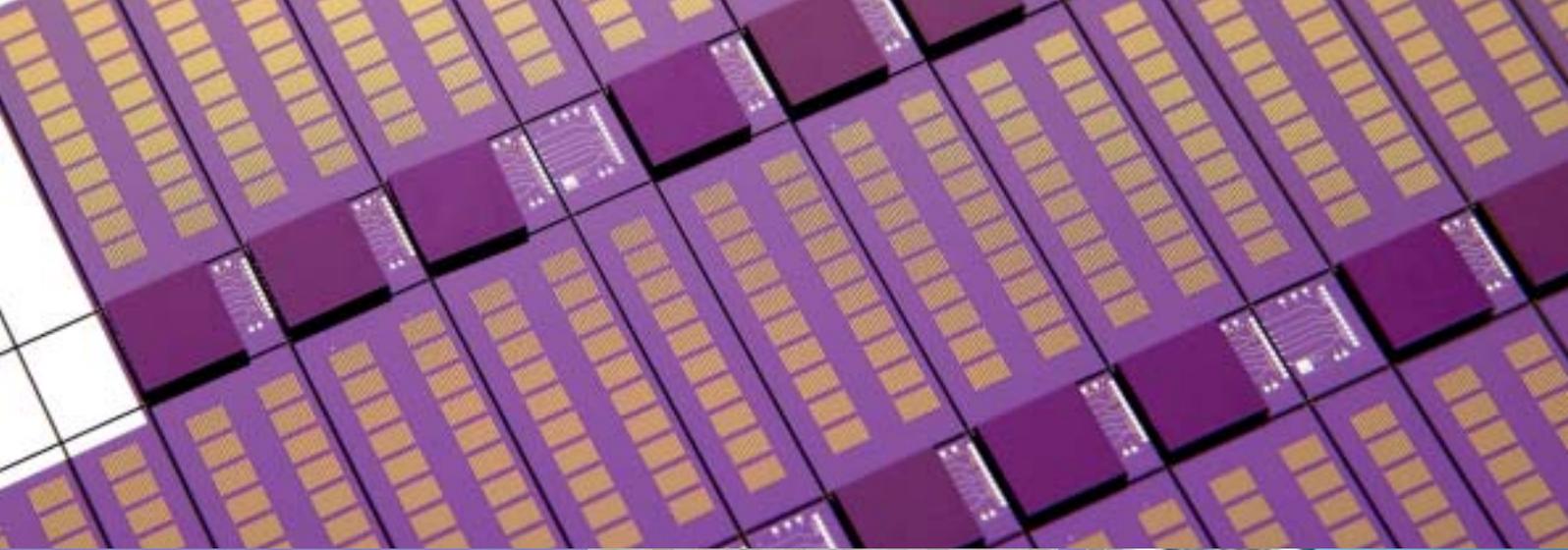
The current emphasis in the area of sensor technology is on inertial sensor technology (acceleration, angular rate, inertial measurement units), pressure, and flow sensors, all with integrated electronics (ASICs). A microsensor core technology using thick polysilicon structural layers and waferlevel hermetic sealing is available.

The development of customized integration concepts, ranging from simple, cost-effective assembly in a common package to complete monolithic integration, represents the core of ISIT's offers in this area. One integration technique is the ability to process microsystems on the surface of a fully processed ASIC wafer using low-temperature processes such as electroplating.

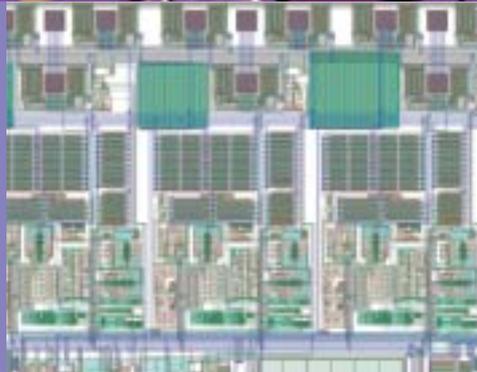
ISIT also develops optical microsystems, primarily for optical instrumentation, consumer products and communication. Examples include micromirrors for laser projection displays, laser scanners and analog or digital light modulators, and passive optical elements such as refractive and diffractive lenses, prisms, or aperture systems.

Radio-frequency microsystems developed at ISIT, designed primarily for use in reconfigurable wireless communication devices, include, RF-MEMS switches, tunable capacitors and ohmic switches.

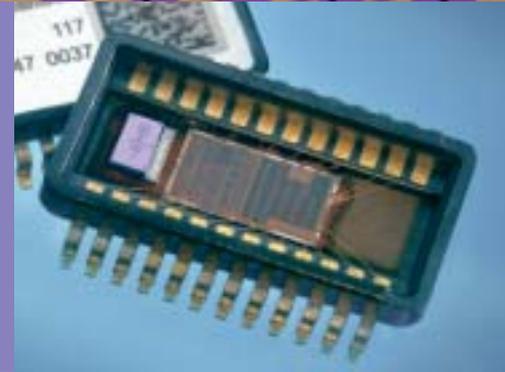
On-chip integrated microactuator systems are especially challenging in order to meet the specific requirements in the micro- and nanometer scale. In this field ISIT has a high expertise and implements electrostatic, thermal and – more recently – high-speed high-force piezoelectric actuation principles on silicon wafers.



*Integration test wafer for chip to wafer bonding of MEMS on CMOS*



*Layout of IC to drive a DC brushless motor*



*Gyroscope module; sensorchip and ASIC in open cavity*

The service approach enables ISIT to offer its customers all of these components as prototypes and also to manufacture them in series according to the customer's specific needs, utilizing the quality and capacity of the institute's in-house semiconductor and MEMS production line. The services provided also include application-specific microsystem packaging at wafer level, including thin wafer and vertical feedthrough capabilities.

Should a customer's requirements fall outside the scope of the institute's technological capabilities, ISIT can utilize a European network to gain access to other manufacturers and processes, like production lines at Bosch, SensoNor, HL Planar, ST and Tronic's. ISIT organizes the production as a foundry service for interested customers.

One of the requirements for developing microsystems and microelectronic components is a highly capable ASIC design group. The staff at ISIT are specialists in the design of analog/digital circuits, which enable the electronic analysis of signals from silicon sensors. The designers at ISIT also model micromechanical and micro optic elements and test their functionality in advance using FEM and behavioral modeling simulation tools.

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*Silicon wafer with electrical biochips*



*Spotting process of different liquids on biochips*

## BIOTECHNICAL MICROSYSTEMS

ISIT is a worldwide leader in electrical biochip technology and holds a variety of patents in relevant fields of application. The electrical biochips offer intrinsic advantages to optical biochips because of its particle tolerance and mechanical robustness by the direct transduction of biochemical reactions into current measurements. The use of nanometer scaled interdigital electrodes combined with integrated reference and auxiliary electrodes together with a sensitive and selective measurement technique ("redox cycling") enables powerful sensor microarrays. These arrays are useful for the detection of a variety of analytes simultaneously. User-friendly operability is realized by packaging the biochips into cartridges called "Chip-Sticks". In combination with micro-fluidic components and integrated electronics, these electrical microarrays represent a rapid and cost-effective analytical basis. It can be used to identify and quantify DNA, RNA and proteins.

ISIT works closely with the Itzehoe based company AJ eBiochip GmbH ([www.ebiochip.com](http://www.ebiochip.com)), an ISIT spin-off, to facilitate the marketing of these new technologies. AJ eBiochip GmbH develops a variety of smart and portable instruments, from devices for educational and demonstration purposes to fully automated microarray analyzers. The successful application of the electrical biochip technology in different fields like the identification and quantification of proteins and pathogenic biowarfare agents as well as the detection of bacterial DNA has been established in several labs in Europe and has been partially supported by EU projects.

### *Biotechnical Microsystems*

*Dr. Eric Nebling*

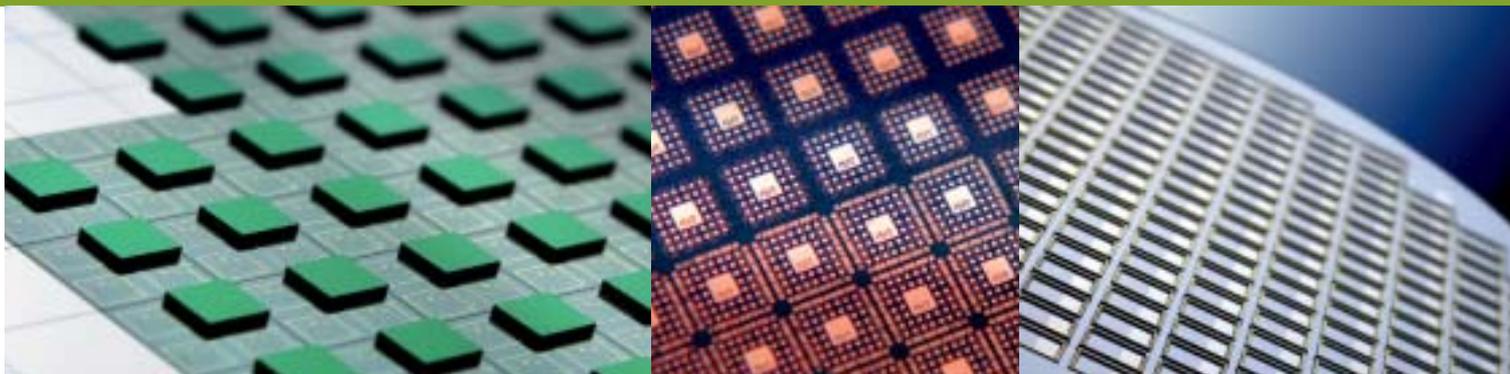
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*Process dummy assembly for chip bonding on substrate wafer*

*Through silicon vias in a process dummy vehicle*

*Cap wafer with getter layers for vacuum packaging*



## PACKAGING TECHNOLOGY FOR MICROELECTRONICS AND MICROSYSTEMS

The assembly and interconnection technology group offers customers a broad range of services, including precision assembly of microstructured components and development and qualification of customer-specific packaging. Work in this area includes hermetic housing and material compatibility tests for assemblies that have to work in aggressive environmental conditions or development of microsystem packages intended for in vivo use in medical technology.

Another focal area is miniaturization of chip and sensor assemblies and packages, which includes direct assembly of bare silicon chips. The institute possesses capabilities in all of the essential technical stages for chip-on-board (COB) technology, from designing the circuit boards to qualified COB assemblies. The bare ICs and microsensors are mounted using the Chip & Wire or Flip-Chip techniques.

The group also develops processes for assembling, through via generation and packaging chips and sensors/actuators while still on the wafer. Due to the increasing global trend among chip manufacturers to implement this special packaging process, Wafer Level Packaging (WLP) has become a central focus of the group's work. WLP technology can also be applied for packaging sensors under vacuum, such as angular rate or acceleration sensors. ISIT has successfully integrated thin film getter layers for high-Q microresonators and improved vacuum lifetime.

The institute is active in this area not only as a technology developer, but also as a manufacturer of assemblies for its customers using the available Chip-Size-Packaging pilot production line. The group also develops ultra-thin electronic assemblies, which involves stacked mounting flexible silicon chips as thin as 50 µm on flexible substrates.

These techniques will ultimately lead to further miniaturization of components in existing systems, such as laptops, hand held PCs or mobile phones, but will also enable the development of new products like intelligent flexible product labels or smart clothes.

*Packaging Technology for Microelectronics and Microsystems*

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## MAIN FIELDS OF ACTIVITY



*ISIT test board for soldering process evaluation*

*Fatigue crack in solder joint*

*Tombstoning of capacitors (C0201)*

## QUALITY AND RELIABILITY OF ELECTRONIC ASSEMBLIES

Quality evaluation – in particular for the soldering work done in pre-production, pilot and main series lots – represents a continuous challenge for ISIT, for example whenever new technologies such as lead-free soldering are introduced, when increased error rates are discovered, or to achieve competitive advantages through continuous product improvement. To reveal potential weak points, ISIT employs both destructive and non-destructive analysis methods, such as x-ray transmission radiography and scanning acoustic microscopy. Working from a requirements matrix, ISIT scientists also evaluate long-term behavior of lead-free and lead-containing assemblies alike. They then formulate prognoses on the basis of model calculations, environmental and time-lapse load tests, and failure analysis.

In anticipation of a conversion to lead-free electronics manufacturing, Fraunhofer ISIT is undertaking design, material selection and process modification projects for industrial partners. To effect a further optimization of manufacturing processes, the institute applies process models and produces samples on industry-compatible equipment. The group also addresses issues related to thermal management and reliability for customer-specific power modules.

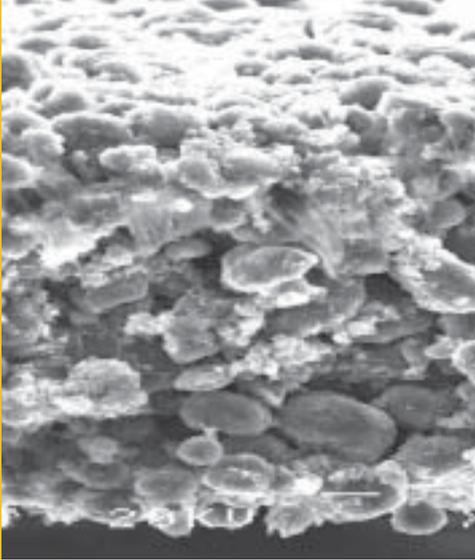
In addition to these technological activities, the group regularly holds training sessions, including multi-day classes, at the institute or at company sites.

*Quality and Reliability of  
Electronic Assemblies*

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*Cross section of a cathode film of a rechargeable Lithium battery filled with nano particles*



*Foils for electrodes, current collectors and the housing are the basic material for the production of Lithium polymer rechargeable batteries*

## INTEGRATED POWER SYSTEMS

Secondary Lithium batteries as a powerful storage medium for electrical energy are rapidly capturing new fields of application outside of the market of portable electronic equipment. Among these new application fields are automotive and medical devices, stationary electric storage units, aerospace, etc. Therefore this type of rechargeable batteries has to meet a variety of new requirements. This covers not only electrical performance but also design and safety features. The Lithium polymer technology developed at ISIT is characterized by an extensive adaptability to specific application profiles like extended temperature range, high power rating, long shelf and/or cycle life, increased safety requirements, etc. Also included is the development of application adapted housings.

In the Lithium polymer technology all components of the cell from electrodes to housing are made from tapes. At ISIT the complete process chain starting with the slurry preparation over the tape casting process and the assembly and packaging of complete cells in customized designs is available including also the electrical and thermomechanical characterization. This allows access to all relevant parameters necessary for an optimization process. The electrode and the electrolyte composition up to the cell design can be modified.

In addition to the development of prototypes limited-lot manufacturing of optimized cells on a pilot production line at ISIT for batteries with storage capacities of up to several ampere-hours is possible. Specific consideration in process development is addressed to the transferability of development results in a subsequent industrial production.

ISIT offers in the field of secondary lithium batteries a wide portfolio of services:

- Manufacturing and characterization of battery raw materials by half cell as well as full cell testing
- Selection of appropriate combinations of materials and design of cells to fulfil customer requirements
- Application driven housing development
- Test panel
- Prototyping and limited-lot manufacturing of cells

Additional services are:

- Preparation of studies
- Failure analysis
- Testing (electrical, mechanical, reliability etc.)

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## OFFERS FOR RESEARCH AND SERVICE



## FACILITIES AND EQUIPMENT

The facilities at Fraunhofer ISIT provide an ideal environment for research & development work as well as for production. In addition to its 150-/200-mm silicon technology line with 2500 m<sup>2</sup> clean-room (class 1), the institute has a further 450 m<sup>2</sup> clean-room area (class 100) for specific microsystem processes, including: wet-etching processes, high-rate plasma etching, deposition of non-IC-compatible materials, lithography of thick resist layers, gray-scale lithography, electroplating, microshaping and wafer bonding. Another 200 m<sup>2</sup> clean-room (class 10-100) is equipped for chemical mechanical polishing (CMP) and post-CMP cleaning. ISIT also offers non cleanroom labs (1500 m<sup>2</sup>) for working groups which develop chemical, biological and thermal processes, electrical and mechanical component characterization, and processes for assembly and interconnection technology. The ISIT facility also operates a pilot production line for Lithium-polymer rechargeable batteries.

## SPECTRUM OF SERVICES

The institute offers its services to companies with a wide range of applications, for example medical technology, communication systems, automotive industry, and industrial electronics, based on the specific requirements of the industrial customers for their components or systems. ISIT engineers work in close cooperation with them to design, simulate and produce the components and systems with the specific manufacturing processes. In this context, ISIT follows the technology platforms concept, which entails defining standard process flows that can be used to manufacture a large group of components simply by varying certain design parameters. Applying this modular technology concept is the optimal way to ensure that ISIT continues to offer competitive prices to its customers. ISIT services have attractive implications for small and medium-sized enterprises, which can take advantage of the institute's facilities and expertise in realizing technological innovations up to products.

## CUSTOMERS

ISIT cooperates with companies of different sectors and sizes.  
In the following some companies are presented as a reference:

**Aardex**, Zug, Switzerland

**ABB**, Västerås, Sweden

**ABB**, Ladenburg

**Ablestik**, Cambridge, England

**Accretech Tokyo-Seimitsu**, Japan

**Accretech Europe GmbH**, München

**Adaptive Photonics**, Hamburg

**ADC Systems GmbH**, Lindau

**ADT German Technology**, Köln

**Advanced PANMOBIL systems**, Köln

**AEMtec**, Berlin

**Airbus-Systeme**, Buxtehude

**AJ eBiochip Systems GmbH**, Itzehoe-Berlin

**Alcatel Vacuum Technology**, Annecy, France

**Alma**, Lyon, France

**Amic**, Uppsala, Sweden

**Andus electronic GmbH**, Berlin

**Applied Materials**, ICT, München

**ARC Seibersdorf Research GmbH**, Seibersdorf, Austria

**ASE**, Seoul, Korea

**Atmel Germany GmbH**, Heilbronn

**Atos Origin**, Madrid, Spanien

**Atotech Deutschland GmbH**, Berlin

**Audi Electronics Venture GmbH**, Ingolstadt

**BASF AG**, Ludwigshafen

**Basler Vision Technologies**, Ahrensburg

**Biont**, Bratislava, Slovakia

**Bosch**, Reutlingen

**B. Braun**, Melsungen

**Bruker Daltonic GmbH**, Leipzig

**Bundeswehr WTD**, Eckernförde

**Cardi plus**, Sevilla, Spain

**CDTA**, Algier, Algerien

**Comau S.p.A.**, Milano, Italy

**Condias GmbH**, Itzehoe

**Conti Temic**, Karben

**Conti Temic microelectronic GmbH**, Nürnberg

**DancoTech A/S**, Ballerup, Denmark

**Danfoss Drives**, Graasten, Denmark

**Danfoss Silicon Power GmbH**, Schleswig

**Datacon Technology AG**, Radfeld/Tirol, Austria

**Evonik Degussa GmbH**, Hanau

**Delong Instruments a.s.**, Brno, Czech Republic

**Diehl Avionik Systeme GmbH**, Überlingen

**Digisound-Electronic GmbH**, Norderstedt

**Dräger Systemtechnik**, Lübeck

**EADS Deutschland GmbH**, Corporate Research Germany

**München and Ulm**

**EN Electronic Network**, Bad Hersfeld

**Engineering Center for Power Electronics GmbH**, Nürnberg

**EPCOS**, Nijmegen, Netherlands

**ESCD**, Brunsbüttel

**ESRF**, Grenoble, France

**ESW-Extel Systems GmbH**, Wedel

**EVGroup**, Schärding, Austria

**EZH GmbH**, Bad Hersfeld

**FICO B.V.**, Duiven, The Netherlands

**Flextronics**, Althofen

**FOS Messtechnik GmbH**, Schacht-Audorf

**Freudenberg & Co. KG**, Weinheim

**Fujitsu Siemens Computers GmbH**, Augsburg

**GE Healthcare**, Finland

**GPS GmbH**, Stuttgart

**Güdel AG**, Langenthal, Switzerland

**Hannusch Industrie-elektronik**, Laichingen

**Harman & Becker**, Karlsbad

**Hasenkamp Internationale Transporte GmbH**, Köln

**Heidenhain**, Traunreut

**Hella KG**, Lippestadt

**Honeywell GmbH**, Schönaich

**HPL S.A.**, Lausanne, Switzerland

**Hymite GmbH**, Berlin

**Ifm electronic GmbH**, Essen

**Imbera Electronics**, Espoo, Finland

**IMS AG**, Wien, Austria

**Institut Virion\Serion GmbH**, Würzburg

**Intecs**, Boeblingen

**Integral Research & Production Corporation**, Minsk, Republic of Belarus

**Jauch Quartz GmbH**, Villingen-Schwenningen

**Jungheinrich AG**, Norderstedt

**Kaco Gerätetechnik GmbH**, Kassel

**Kavlico GmbH**, Minden

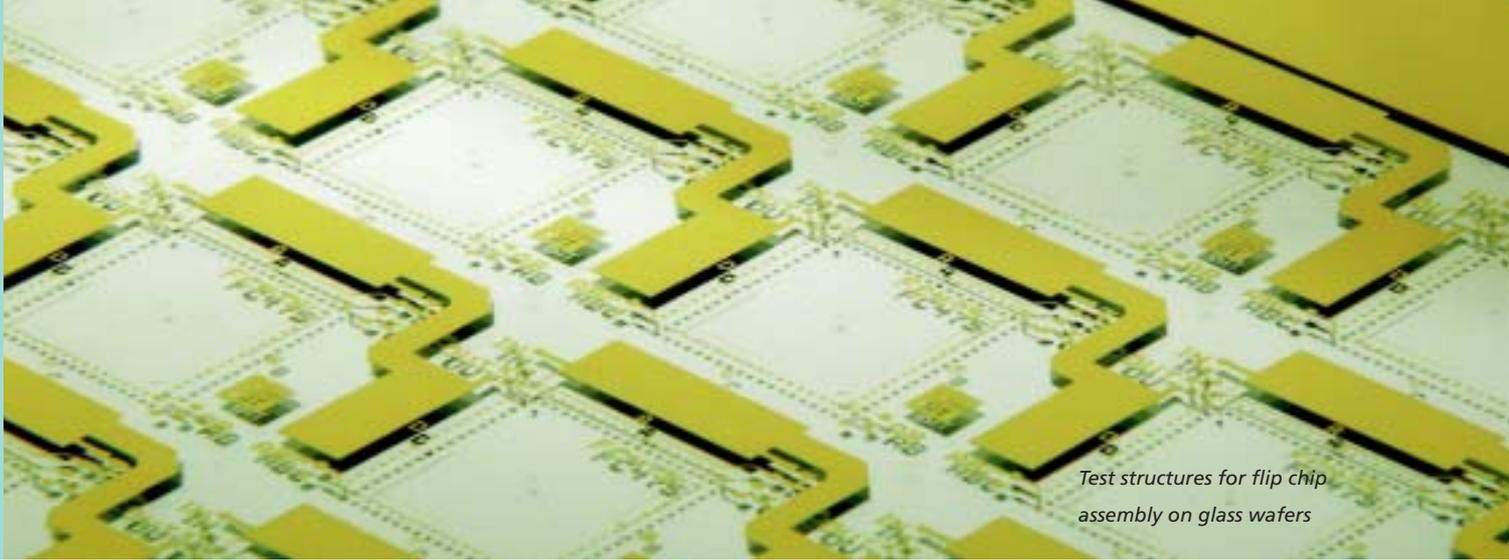
**Kristronics GmbH**, Harrislee-Flensburg

**Kuhnke GmbH**, Malente

**Kunstsammlung Nordrhein Westfalen**, Düsseldorf

**Lam Research**, Fremont, USA

**Leclanché Lithium GmbH**, Willstätt



Test structures for flip chip assembly on glass wafers

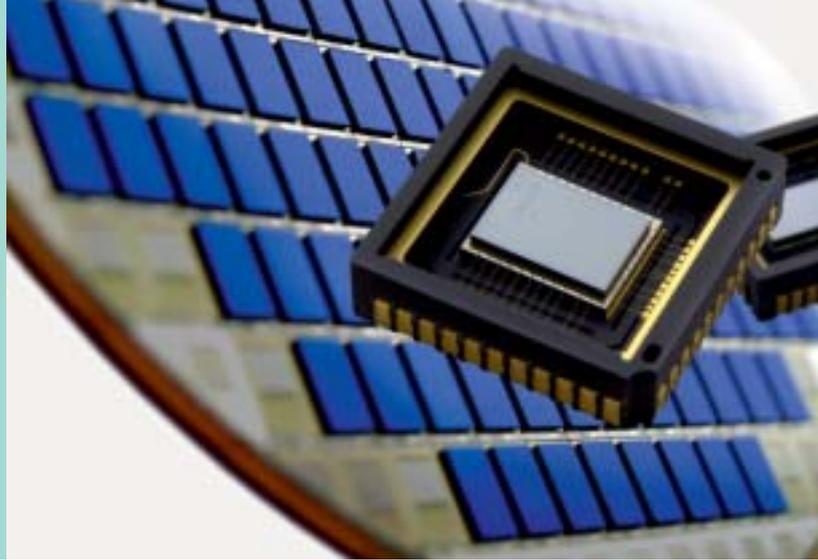
<b>Lenze Drive Systems GmbH,</b> <i>Hameln</i>	<b>Panasonic Factory Solutions Europe GmbH,</b> <i>München</i>	<b>SAES Getters S.p.A.,</b> <i>Lainatel Milan, Italy</i>	<b>Tesat Spacecom,</b> <i>Backnang</i>
<b>Liebherr Elektronik,</b> <i>Lindau</i>	<b>Panasonic,</b> <i>Neumünster</i>	<b>Sartorius Hamburg GmbH</b> <i>Research &amp; Development, Hamburg</i>	<b>Thales,</b> <i>Paris, France</i>
<b>Litef,</b> <i>Freiburg</i>	<b>PAV Card GmbH,</b> <i>Lütjensee</i>	<b>Sauer, Danfoss,</b> <i>Nordborg, Denmark</i>	<b>Treichel Elektronik GmbH,</b> <i>Springe</i>
<b>Lumio Ltd,</b> <i>Jerusalem, Israel</i>	<b>Peter Wolters GmbH,</b> <i>Rendsburg</i>	<b>Schott AG,</b> <i>Mainz</i>	<b>TR-Elektronik,</b> <i>Trossingen</i>
<b>Mair Elektronik GmbH,</b> <i>Neufahrn</i>	<b>PlanOptik AG,</b> <i>Elsoff</i>	<b>SEF GmbH,</b> <i>Scharnebek</i>	<b>Trinamic,</b> <i>Hamburg</i>
<b>Meder electronic AG,</b> <i>Engen-Welschingen</i>	<b>Plath Eft GmbH,</b> <i>Norderstedt</i>	<b>Sensys Traffic AB,</b> <i>Upsala, Sweden</i>	<b>Tyndall National Institute,</b> <i>Cork, Ireland</i>
<b>MELZER maschinenbau GmbH,</b> <i>Schwelm</i>	<b>PMDTec,</b> <i>Siegen</i>	<b>Siemens AG,</b> <i>Erlangen</i>	<b>Umicore AG &amp; Co.,</b> <i>Hanau</i>
<b>MEMS-TC,</b> <i>Schoorl, The Netherlands</i>	<b>Polytec PT GmbH,</b> <i>Waldbronn</i>	<b>Siemens AG,</b> <i>Amberg</i>	<b>Vectron International GmbH &amp; Co. KG,</b> <i>Neckarbischofsheim</i>
<b>Microdrop technologies GmbH,</b> <i>Norderstedt</i>	<b>Preh GmbH,</b> <i>Neustadt a.d.S.</i>	<b>SMA Regelsysteme GmbH,</b> <i>Niestetal</i>	<b>Via Electronic GmbH,</b> <i>Hermsdorf</i>
<b>Microelectronics Packaging,</b> <i>Dresden</i>	<b>Prettl Elektronik Lübeck GmbH,</b> <i>Lübeck</i>	<b>Smart Material GmbH,</b> <i>Dresden</i>	<b>Vishay Beyschlag,</b> <i>Heide</i>
<b>Micronas GmbH,</b> <i>Freiburg</i>	<b>Prospektiv Gesellschaft für betriebliche Zukunftsgestaltung GmbH,</b> <i>Dortmund</i>	<b>SMI,</b> <i>Milpitas, USA</i>	<b>Vishay, Dimona and Holon,</b> <i>Israel</i>
<b>Miele &amp; Cie.,</b> <i>Gütersloh</i>	<b>Protec Process Systems GmbH,</b> <i>Siegen</i>	<b>Smyczek,</b> <i>Verl</i>	<b>Vishay Siliconix Itzehoe GmbH,</b> <i>Itzehoe</i>
<b>Museum Ludwig,</b> <i>Köln</i>	<b>Pulse Engineering, Inc.,</b> <i>Lyngby, Denmark</i>	<b>Solon Laboratories,</b> <i>Berlin</i>	<b>Vishay Siliconix,</b> <i>Santa Clara, USA</i>
<b>Nokia Research Center,</b> <i>Nokia Group, Helsinki, Finland</i>	<b>Qimonda AG,</b> <i>Neubiberg</i>	<b>Sonion A/S,</b> <i>Roskilde, Denmark</i>	<b>Vistec Electron Beam GmbH,</b> <i>Jena</i>
<b>NU-Tech GmbH,</b> <i>Neumünster</i>	<b>Raytheon Anschutz GmbH,</b> <i>Kiel</i>	<b>Sony Deutschland GmbH,</b> <i>Stuttgart</i>	<b>Volkswagen AG,</b> <i>Wolfsburg</i>
<b>NXP Semiconductors,</b> <i>Hamburg</i>	<b>Rehm Anlagenbau GmbH,</b> <i>Blaubeuren-Seissen</i>	<b>ST Microelectronics,</b> <i>Crolles, France</i>	<b>Wabco Fahrzeugbremsen,</b> <i>Hannover</i>
<b>Océ-Technologies B.V.,</b> <i>Venlo, Netherlands</i>	<b>Reis Robotics GmbH &amp; Co,</b> <i>Obernburg</i>	<b>ST Microelectronics Srl,</b> <i>Mailand, Italy</i>	<b>Wintershall AG,</b> <i>Kassel</i>
<b>Omicron Laserage GmbH,</b> <i>Rodgau</i>	<b>Rena Sondermaschinen GmbH,</b> <i>Gütenbach</i>	<b>Still GmbH,</b> <i>Hamburg</i>	<b>Würth Elektronik GmbH,</b> <i>Schopfheim</i>
<b>Imron GmbH,</b> <i>Stuttgart</i>	<b>Robert Bosch GmbH,</b> <i>Salzgitter</i>	<b>SÜSS Microtec AG,</b> <i>Garching</i>	
<b>Osram Opto Semiconductors GmbH,</b> <i>Regensburg</i>	<b>Robert Bosch GmbH,</b> <i>Schwieberdingen</i>	<b>Technolas,</b> <i>München</i>	
<b>Oticon A/S,</b> <i>Hellerup, Denmark</i>	<b>Rutronik Elektrische Bauelemente GmbH,</b> <i>Ispringen/Pforzheim</i>	<b>Telefonica,</b> <i>Madrid, Spain</i>	

# INNOVATION CATALOGUE

ISIT offers its customers various products and services already developed for market introduction. The following table presents a summary of the essential products and services. Beyond that the utilisation of patents and licences is included in the service.

Product / Service	Market	Contact Person
Testing of semiconductor manufacturing equipment	Semiconductor equipment manufacturers	<b>Dr. Gerfried Zwicker</b> + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
Chemical-mechanical polishing (CMP), planarization	Semiconductor device manufacturers	<b>Dr. Gerfried Zwicker</b> + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
Wafer polishing, single and double side	Si substrates for device manufacturers	<b>Dr. Gerfried Zwicker</b> + 49 (0) 4821/17-4309 gerfried.zwicker@isit.fraunhofer.de
IC processes and power devices CMOS, PowerMOS, IGBTs	Semiconductor industry IC-users	<b>Detlef Friedrich</b> + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Single processes and process module development	Semiconductor industry semiconductor equipment manufacturers	<b>Detlef Friedrich</b> + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Customer specific processing	Semiconductor industry semiconductor equipment manufacturers	<b>Detlef Friedrich</b> + 49 (0) 4821/17-4301 detlef.friedrich@isit.fraunhofer.de
Microsystem Products	Electronic industry	<b>Dr. Ralf Dudde</b> + 49 (0) 4821/17-4212 ralf.dudde@isit.fraunhofer.de
Inertial sensors	Motorvehicle technology, navigation systems, measurements	<b>Dr. Klaus Reimer</b> + 49 (0) 4821/17-4233 klaus.reimer@isit.fraunhofer.de
Thick epi poly MEMS processing	Sensors and actuators	<b>Dr. Peter Merz</b> + 49 (0) 4821/17-4513 peter.merz@isit.fraunhofer.de
Piezoelectric microsystems	Sensors and actuators	<b>Hans-Joachim Quenzer</b> + 49 (0 ) 4821/17-4643 hans-joachim.quenzer@isit.fraunhofer.de
Microoptical scanners and projectors	Biomedical technology, optical measurement industry, telecommunication	<b>Ulrich Hofmann</b> + 49 (0) 4821/17-4553 ulrich.hofmann@isit.fraunhofer.de
Flow sensors	Automotive, fuel cells	<b>Dr. Peter Lange</b> +49 (0) 4821/17-4220 peter.lange@isit.fraunhofer.de
Microoptical components	Optical measurement	<b>Hans Joachim Quenzer</b> + 49 (0) 4821/17-4643 hans-joachim.quenzer@isit.fraunhofer.de
RF-MEMS	Telecommunication	<b>Thomas Lisec</b> + 49 (0) 4821/17-4512 thomas.lisec@isit.fraunhofer.de
Design and test of analogue and mixed-signal ASICs	Measurement, automatic control industry	<b>Jörg Eichholz</b> + 49 (0) 4821/17-4253 joerg.eichholz@isit.fraunhofer.de

Hermetically capped infrared  
radiation sensor on wafer



Product / Service	Market	Contact Person
Design Kits	MST foundries	<b>Jörg Eichholz</b> + 49 (0) 4821117-4253 joerg.eichholz@isit.fraunhofer.de
MST Design and behavioural modelling	Measurement, automatic control industry	<b>Jörg Eichholz</b> + 49 (0) 4821117-4253 joerg.eichholz@isit.fraunhofer.de
Electrodeposition of microstructure	Surface micromachining	<b>Martin Witt</b> + 49 (0) 4821117-4613 martin.witt@isit.fraunhofer.de
Digital micromirror devices	Communication technology	<b>Dr. Klaus Reimer</b> + 49 (0) 4821117-4233 klaus.reimer@isit.fraunhofer.de
Electrical biochip technology (proteins, nucleic acids, haptens)	Biotechnology, related electronics microfluidics, environmental analysis, Si-Chipprocessing, packaging, chip loading	<b>Dr. Eric Nebling</b> + 49 (0) 4821117-4312 eric.nebling@isit.fraunhofer.de
Secondary lithium batteries based on solid state ionic conductors	Mobile electronic equipment, medical applications, automotive, smart cards, labels, tags	<b>Dr. Peter Gulde</b> +49 (0) 4821117-4307 peter.gulde@isit.fraunhofer.de
Battery test service, electrical parameters, climate impact, reliability, quality	Mobile electronic equipment medical applications automotive, smart cards labels, tags	<b>Dr. Peter Gulde</b> +49 (0) 4821117-4307 peter.gulde@isit.fraunhofer.de
Quality and reliability of electronic assemblies ( <a href="http://www.isit.fraunhofer.de">http://www.isit.fraunhofer.de</a> )	Microelectronic and power electronic industry	<b>Karin Pape</b> + 49 (0) 4821117-4229 karin.pape@isit.fraunhofer.de
Material and damage analysis	Microelectronic and power electronic industry	<b>Helge Schimanski</b> +49 (0) 4821117-4639 helge.schimanski@isit.fraunhofer.de
Thermal measurement and simulation	Microelectronic and power electronic industry	<b>Dr. M. H. Poech</b> + 49 (0) 4821117-4607 max.poech@isit.fraunhofer.de
Leadfree / RoHS transformation in electronic assembly	Electronic industry	<b>Helge Schimanski</b> +49 (0) 4821117-4639 helge.schimanski@isit.fraunhofer.de
Packaging for microsystems, sensors, multichip modules ( <a href="http://www.isit.fraunhofer.de">http://www.isit.fraunhofer.de</a> )	Microelectronic, sensoric and medical industry	<b>Karin Pape</b> + 49 (0) 4821117-4229 karin.pape@isit.fraunhofer.de
Wafer level packaging, ultra thin Si packaging and direct chip attach techniques	Microelectronic, sensoric and medical industry, automotive industry	<b>Dr. Wolfgang Reinert</b> + 49 (0) 4821117-4617 wolfgang.reinert@isit.fraunhofer.de
Vacuum wafer bonding technology	Microelectronic, sensoric and medical industry, automotive industry	<b>Dr. Wolfgang Reinert</b> + 49 (0) 4821117-4617 wolfgang.reinert@isit.fraunhofer.de

# REPRESENTATIVE FIGURES

## EXPENDITURE

In 2008 the operating expenditure of Fraunhofer ISIT amounted to 18.695,79 T€. Salaries and wages were 6.987,8 T€, material costs and different other running costs were 11.707,9 T€.

## INCOME

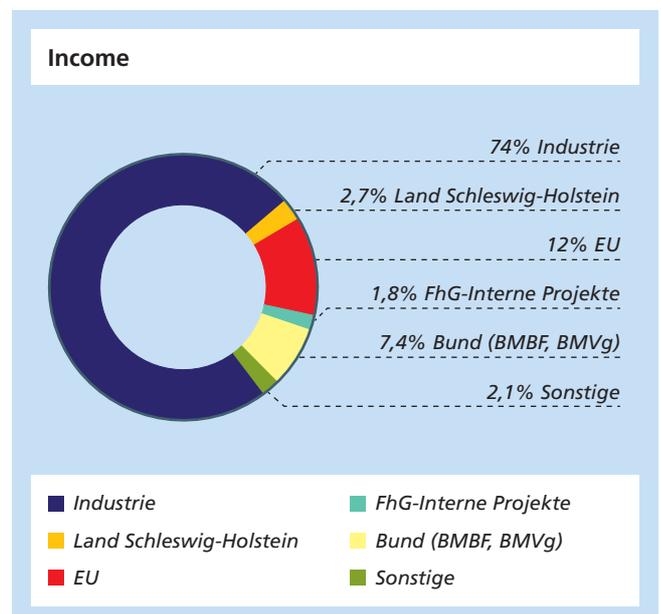
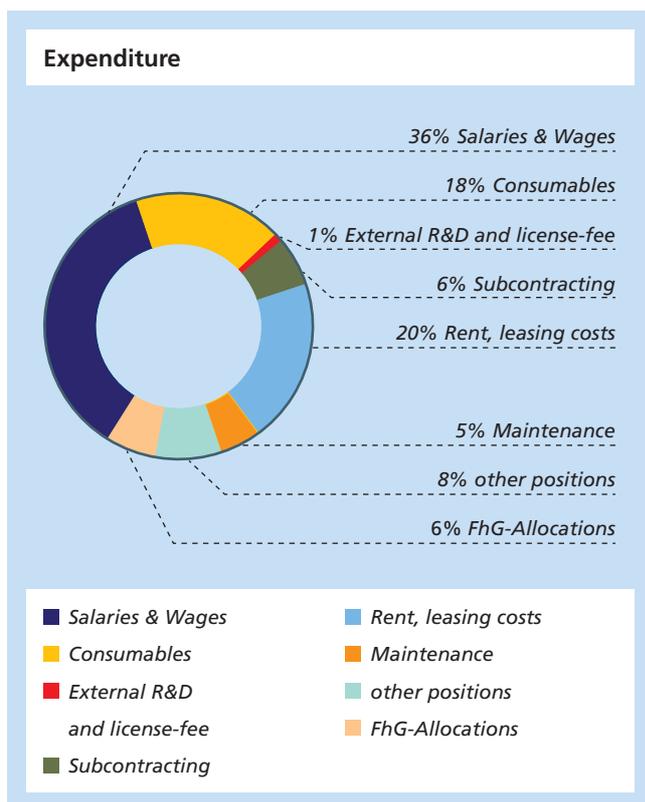
The budget was financed by proceeds of projects of industry/ industrial federations/small and medium sized companies amounting to 12.134,0 T€, of government/project sponsors/ federal states amounting to 1.661,4 T€ and of European Union/others amounting to 2.605,1 T€.

## CAPITAL INVESTMENT

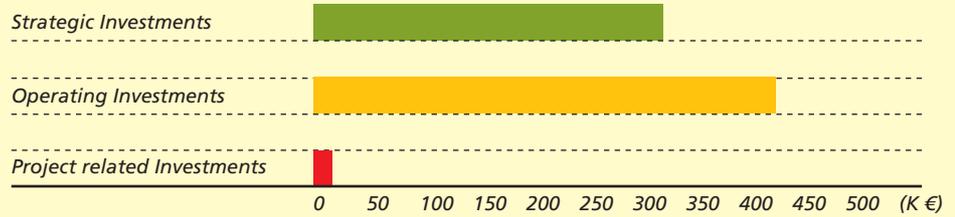
In 2008 the institutional budget of capital investment was 726,6 T€. The amount of strategic investment was 308,4 the operating investment was 407,5 T€ and project related investments were amounted to 10,7 T€.

## STAFF DEVELOPMENT

In 2008, on annual average, the staff consisted of 111 employees. 53 were employed as scientific personnel, 45 as graduated/technical personnel and 13 worked within organisation and administration. The employees were assisted through 27 scientific assistants, 4 apprentices and 7 others.

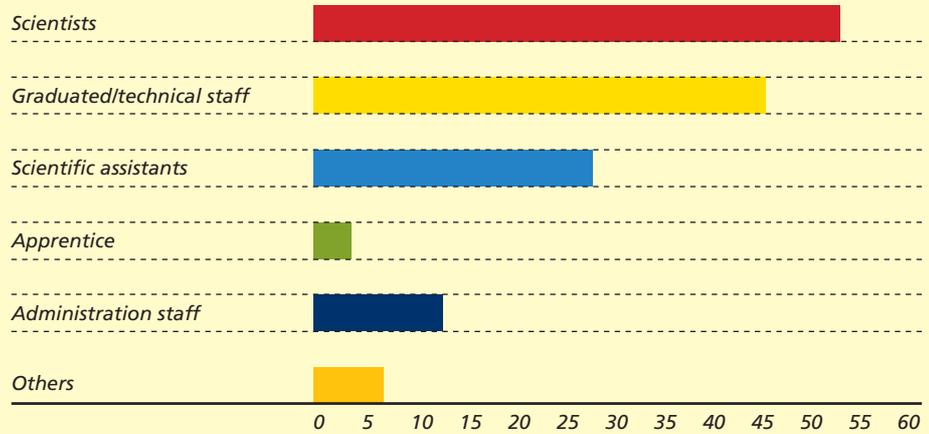


### Capital Investment



- Strategic Investments
- Operating Investments
- Project related Investments

### Staff Development



- Scientists
- Graduated/technical staff
- Scientific assistants
- Apprentice
- Administration staff
- Others

# THE FRAUNHOFER-GESELLSCHAFT

Research of practical utility lies at the heart of all activities pursued by the Fraunhofer-Gesellschaft. Founded in 1949, the research organization undertakes applied research that drives economic development and serves the wider benefit of society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration.

At present, the Fraunhofer-Gesellschaft maintains more than 80 research units in Germany, including 57 Fraunhofer Institutes. The majority of the 15,000 staff are qualified scientists and engineers, who work with an annual research budget of €1.4 billion. Of this sum, more than €1.2 billion is generated through contract research. Two thirds of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. Only one third is contributed by the German federal and Länder governments in the form of base funding, enabling the institutes to work ahead on solutions to problems that will not become acutely relevant to industry and society until five or ten years from now.

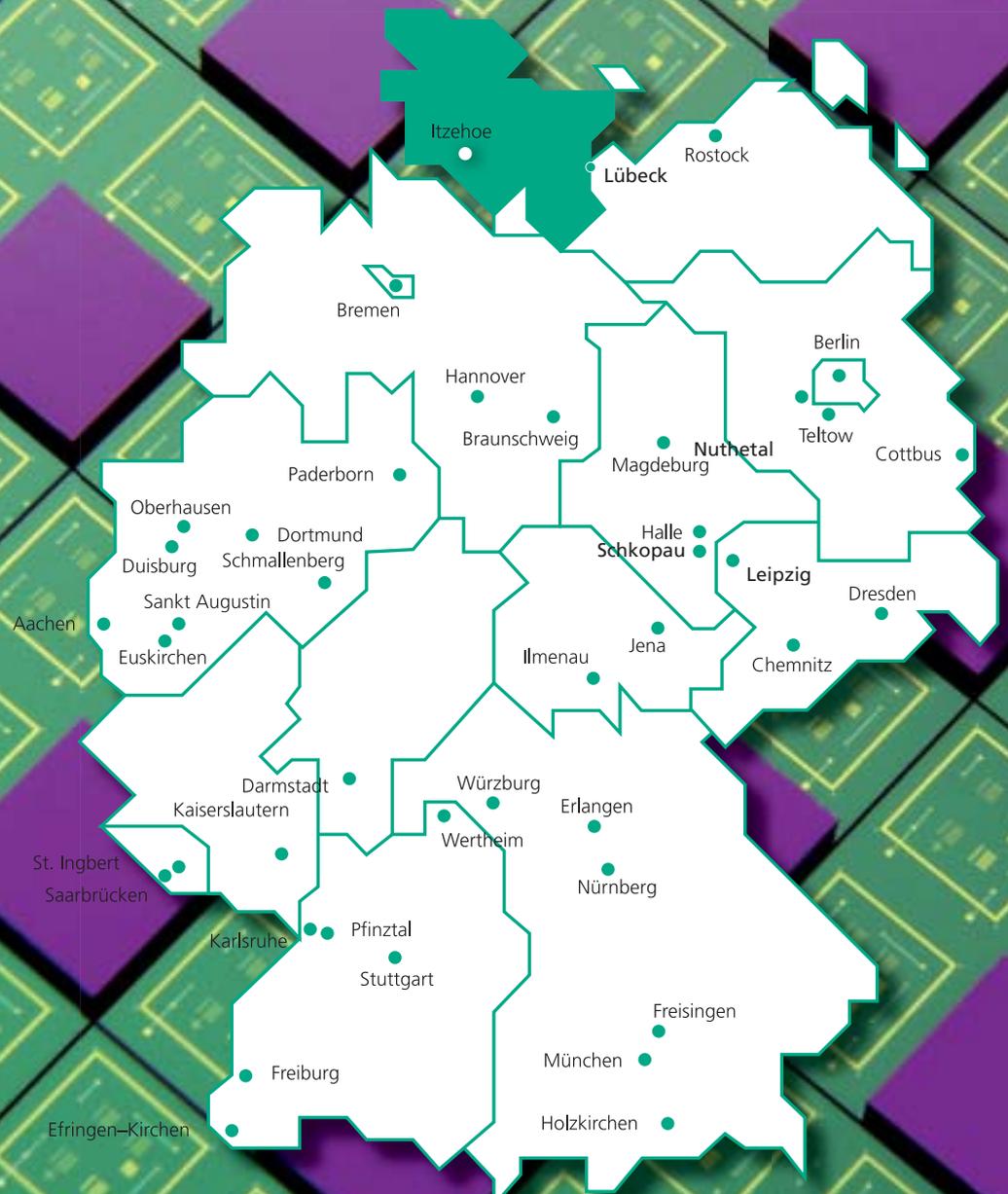
Affiliated research centers and representative offices in Europe, the USA and Asia provide contact with the regions of greatest importance to present and future scientific progress and economic development.

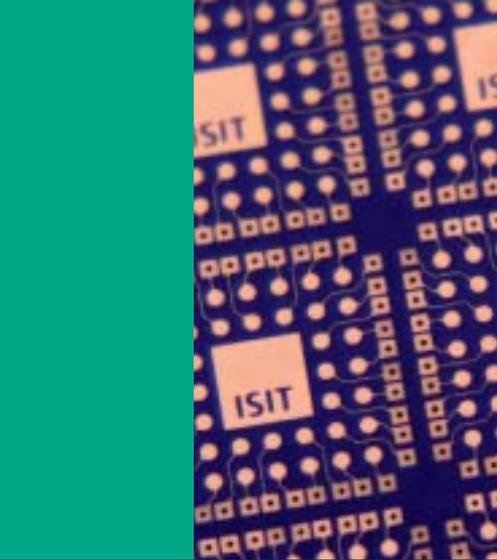
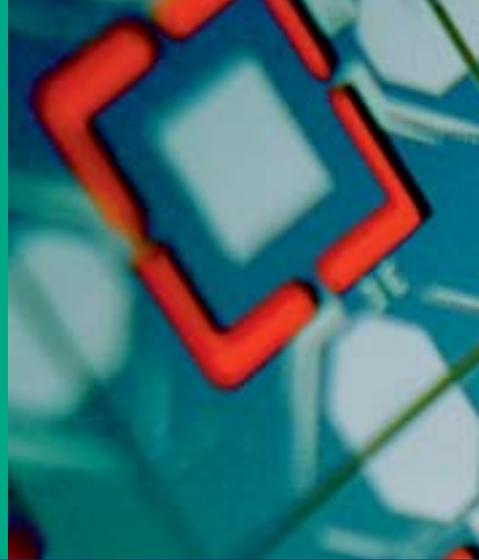
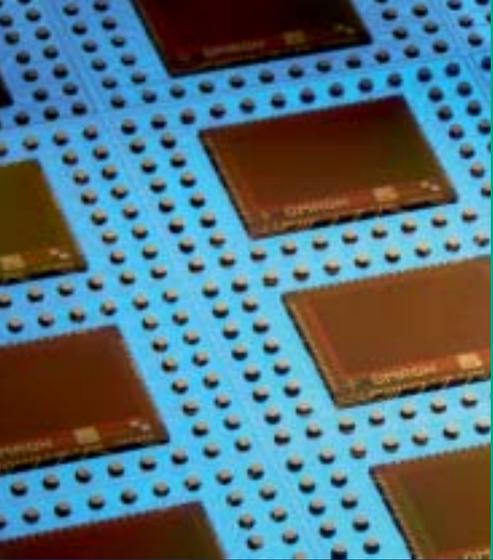
With its clearly defined mission of application-oriented research and its focus on key technologies of relevance to the future, the Fraunhofer-Gesellschaft plays a prominent role in the German and European innovation process. Applied research has a knock-on effect that extends beyond the direct benefits perceived by the customer: Through their research and development work, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. They do so by promoting innovation, strengthening the technological base, improving the acceptance of new technologies, and helping to train the urgently needed future generation of scientists and engineers.

As an employer, the Fraunhofer-Gesellschaft offers its staff the opportunity to develop the professional and personal skills that will allow them to take up positions of responsibility within their institute, at universities, in industry and in society. Students who choose to work on projects at the Fraunhofer Institutes have excellent prospects of starting and developing a career in industry by virtue of the practical training and experience they have acquired.

The Fraunhofer-Gesellschaft is a recognized non-profit organization that takes its name from Joseph von Fraunhofer (1787–1826), the illustrious Munich researcher, inventor and entrepreneur.

# LOCATIONS OF THE RESEARCH ESTABLISHMENT





# REPRESENTATIVE RESULTS OF WORK



# MICROSYSTEMS TECHNOLOGY AND IC-DESIGN

## PROTEM - PROBE-BASED TERABIT MEMORY

### Introduction

Data storage technology is at a critical point in its development. A combination of two very strong driving forces is emerging:

- on one side there is a strong demand towards smaller, lower-power, higher-capacity yet reliable memories for a plethora of multimedia, communication and digital archiving applications.
- while on the other side the conventional storage techniques faces more and more problems since they approach formidable barriers towards continuous improvements (see figure 1): like the superparamagnetic limit for magnetic storage, the diffraction limit for optical storage, and device scaling limits in solid state (Flash) storage.

**Aim** - to develop probe storage micro-nano techniques and systems for ultra-high-capacity, low power, small form-factor memories with a particular focus on archival and back-up applications

**Vision** - Ultra-high storage densities (1 to 10 Tbit/sq.in.), ultra-high capacities (20 TBytes in CD-sized area), media and system lifetimes and data rates suitable for archival and backup storage

**Partners** - IBM Zurich GmbH, CEA-LETI, ST Microelectronics, RWTH-Aachen, Plasmon Data, Systems Ltd, Arithmatica Ltd, University of Twente, Fraunhofer ISIT, University of Exeter, ALMA Consulting Group

**Co-ordinator** - Professor C. David Wright, University of Exeter (David.Wright@exeter.ac.uk)

**Project Funding** - 5,298,510 € **Project Budget** - 9,627,544 €

**Project start date** - 1st October 2006 **Project Duration** - 4 years

**Project number** - FP6-2005-IST-5-34719

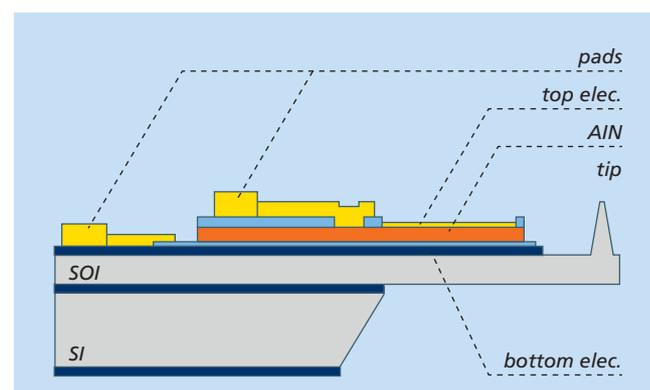
**Website** [www.protem-fp6.org](http://www.protem-fp6.org)

For these reasons new technologies must be studied for their potential in storage applications. One such emerging technology is probe storage, which has enormous potential to satisfy future needs for ultra-high-capacity, non-volatile, low-power, low-cost, write-once and re-writable memories.

Therefore ProTeM aims at developing probe storage micro-nano techniques and systems for very high-density mass storage in a small size and with high performance.

A key requirement for any viable ultra-high density mass storage device or system is the ability to reduce the interaction volume between the 'head', used for writing and reading of data, and the storage medium. Probe-storage meets this requirement by using techniques adapted from scanning probe microscopy (SPM) to detect and modify on the nanoscale various material properties. The relatively slow write/read process of such a SPM system, which depends on the scanning speed, can be compensated to some extent for storage applications

Figure 1: Sketch of the piezoelectric driven AFM tip. Beneath the AlN layer a bottom electrode made from Molybdenum is used, while the top layer consists of Chromium and Gold.



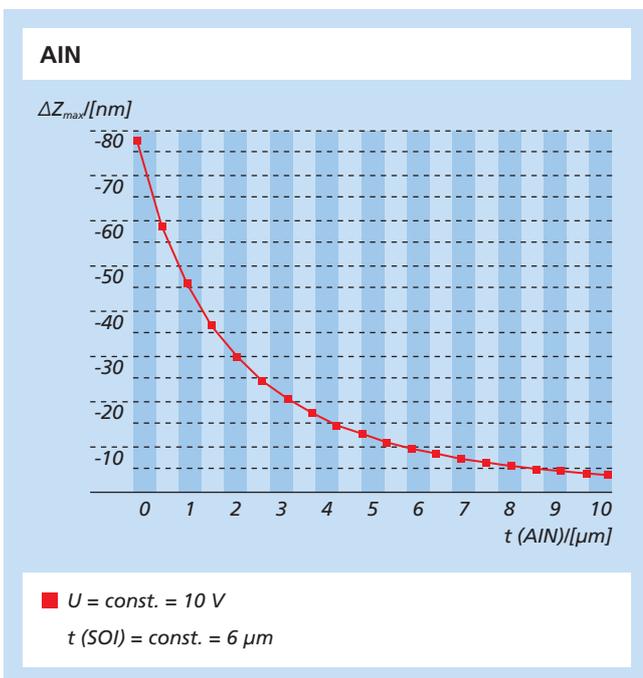


Figure 2: Calculated tip deflection of cantilever structure using various AIN thicknesses as an actuator material.

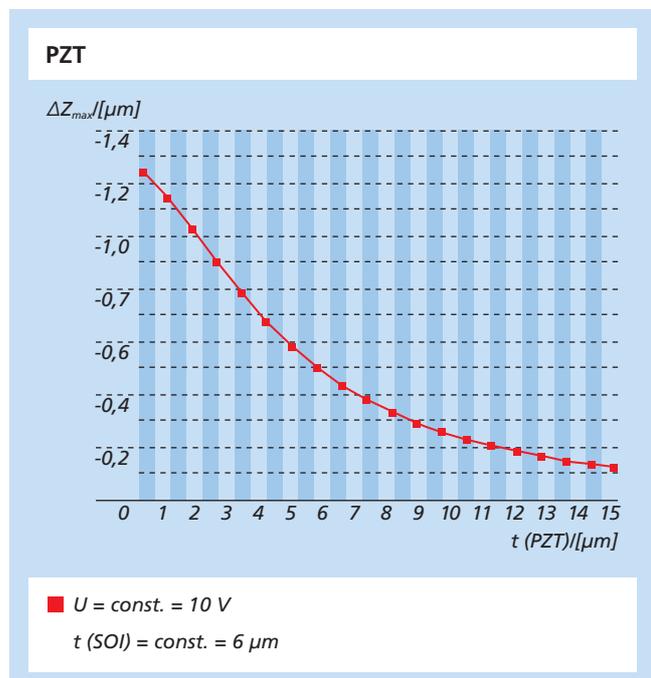


Figure 3: In this FEA the same model was used as in figure 2. Only the material AIN was replaced by PZT.

by the parallel operation of a two-dimensional array of tips. The objective of the work of Fraunhofer ISIT within ProTem is the development of advanced microprobe technologies with high endurance, high speed, high sensitivity and low-power consumption for polymer and phase-change media. Therefore, it is planned to develop a piezoelectric driven AFM cantilever with read/ write function. Because of its CMOS compatibility and earlier availability at Fraunhofer ISIT, Aluminumnitride (AIN) has been selected as the piezoelectric material for the first demonstrator. Moreover, processes including the bottom electrode, required for the AIN growth by sputtering method, and the patterning of the AIN film are meanwhile available.

Nevertheless Lead Zirconium Titanate (PZT) is also a very attractive material due to its much higher piezoelectric coefficients. For comparison in finite element analysis (FEA) a cantilever structure (silicon, 200  $\mu m$  long, thickness 6  $\mu m$ ) covered with a layer of AIN or PZT and driven with a constant voltage of 10 V has been modeled. In both cases standard bulk values are assumed for the material properties of AIN and PZT.

The results showed a drastically increase in the deflection which can be achieved if PZT replaces AIN as an actuator material (see figure 2 and figure 3). It should be emphasized that the enormous difference in the achievable deflection

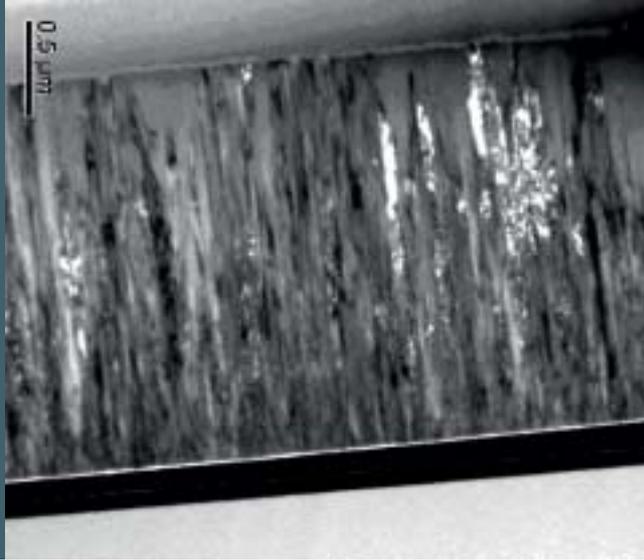


Figure 4: 2  $\mu\text{m}$  thick AlN film sputtered on the Unaxis Clusterline at Fraunhofer ISIT. The textured AlN material oriented perpendicular to the substrate is visible.

using the different piezoelectric materials is only valid using a constant driving voltage. Since the breakdown voltage of AlN is much higher compared to PZT the low piezoelectric coefficient of AlN can be partly compensated using higher driving voltages - if the addressed application allows the usage of those higher voltage levels (up to several 100's Volt). So the breakthrough strength of AlN films is in the range up to 500 V/ $\mu\text{m}$  leading to nearly no limitation in the max. driving voltage while the max. driving voltages in case of PZT thin films are restricted to approx. 20 - 40 V/ $\mu\text{m}$ . In practice for the AFM device the available voltages are restricted to max. 20 V which leads to the situation that using PZT enables much higher tip deflections compared to AlN. Using thinner piezoelectric layers would also increase the achievable deflections. While in case of PZT thin films the minimum thickness should not fall below 1  $\mu\text{m}$  due to its breakdown behavior, very thin AlN layer showed degradation in their piezoelectric properties.

Tests on sputtered c-textured AlN layers (see figure 4) using a commercial  $e_{31,f}$  set-up (see figure 5, figure 6, figure 7) showed a continuous reduction of the piezoelectric parameters for AlN thin films. However, even very thin films (thickness 300 nm) still showed  $e_{31,f}$  values of -0.9 C/m<sup>2</sup> so that tip deflections in the range of 70 nm are expected at driving voltages of 10 V (see figure 8) .

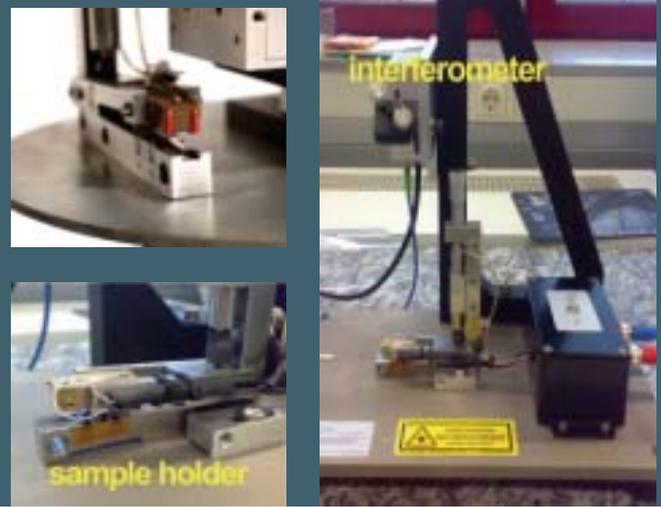


Figure 5: Aixact set-up for measuring  $e_{31,f}$  on piezoelectric samples in the Fraunhofer ISIT lab. The sample is clamped into the holder and periodically bended by an external force. The deflection caused by the bending is measured by the laser interferometer.

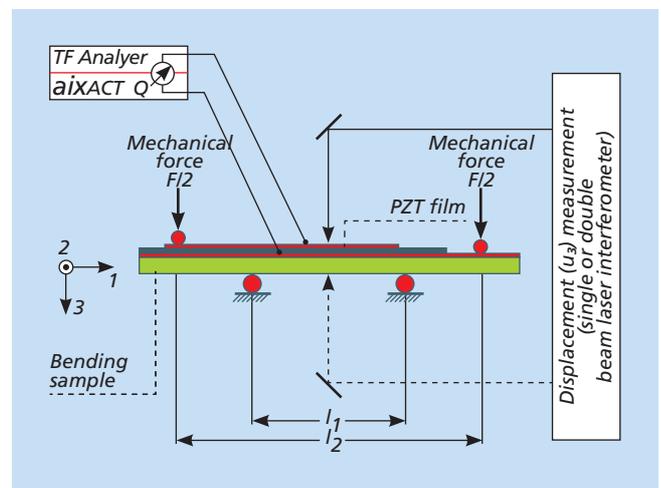


Figure 6: Sketch of the working principle of the  $e_{31,f}$  set-up. The sample is bended in a mechanical holder while the deflection is controlled by a laser interferometer. The electrical charges generated by the stressed piezoelectric material are detected by the electrical analyser.

Therefore, the target specifications for the piezoelectric AFM (min. tip deflection of approx 100 nm at an eigenfrequency of 250 kHz.) can be fulfilled with an AlN layer of approx. 500 nm at driving voltages of 14 V.

The fabrication process of the first demonstrator is meanwhile completed and the fabricated devices are currently in test. The demonstrator chip is designed to replace the standard AFM tips in a commercially available AFM tool. With this test approach the achievable deflection and the possible resolution can be measured in a commercial AFM tool which can be used effectively as a test bench for the AFM chip.

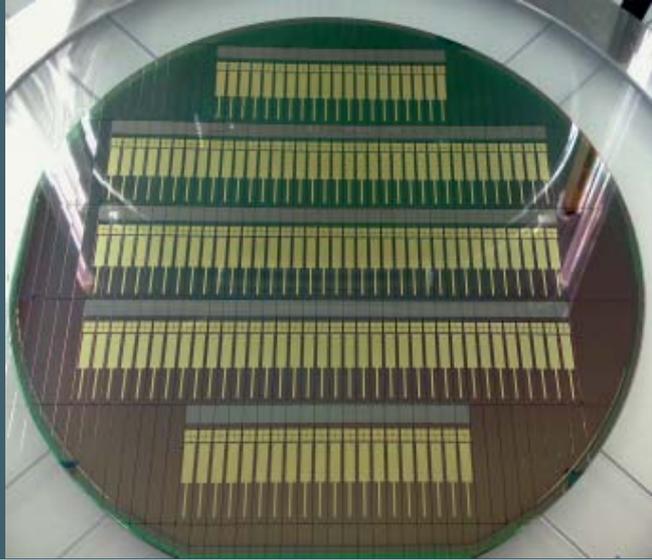


Figure 7: Test samples on the 6 " wafer after dicing. The grey areas are the contacts to the bottom electrode.

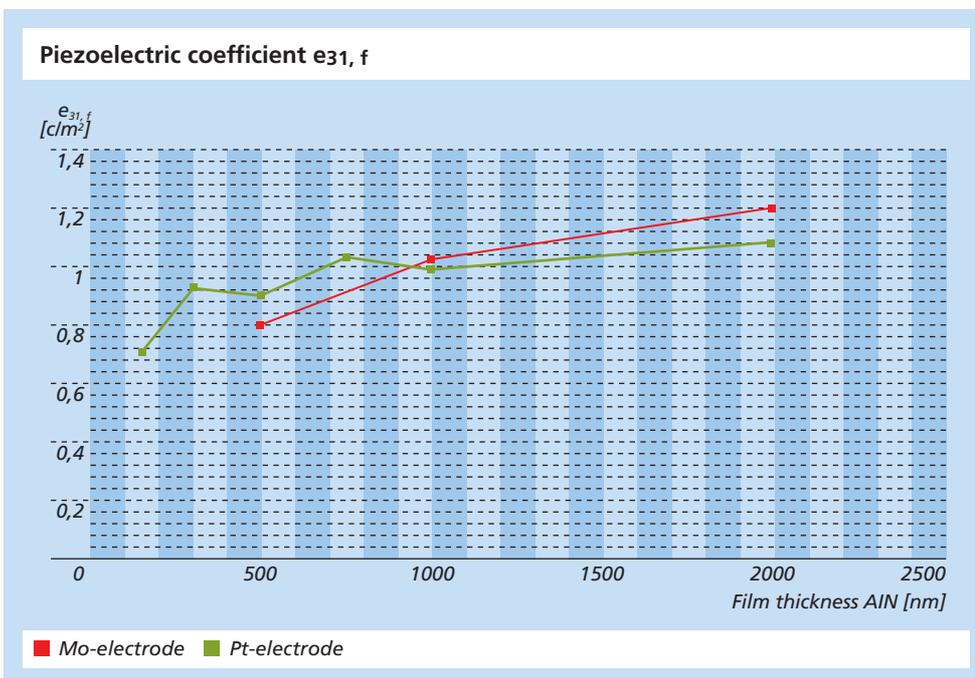


Figure 8: Piezoelectric modulus  $e_{31,f}$  measured as function of the layer thickness of sputtered AlN layers on samples prepared by Fraunhofer ISIT.

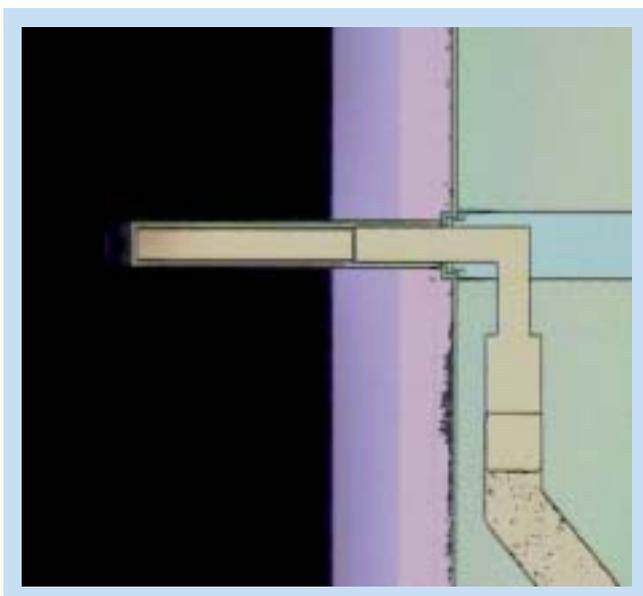


Figure 9: Microscope picture of the demonstrator chip.

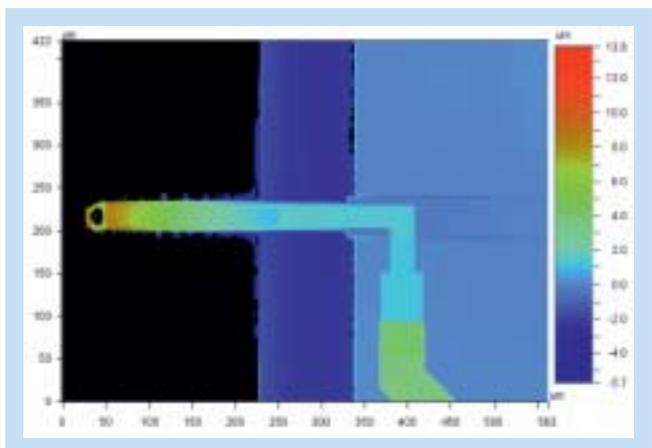


Figure 10: Results of a white light interferometer of the first chip. The tip at the end of the cantilever is due to mechanical stress several  $\mu\text{m}$  deflected.



Figure 1: An inertial measurement unit (IMU) using a combination of accelerometers and gyroscopes. Three SD755 combi sensors mounted on PCBs.



Figure 2: The open cavity OC24 housing includes a combined MEMS Sensor chip (left) and an ASIC (right). The single chip MEMS sensor integrates one accelerometer and one angular rate sensor.

### COMBINED MEMS INERTIAL SENSORS

Micro Electro Mechanical Systems (MEMS) combine small device size with low cost in production and high reliability. This results in an increased application in the automotive industry, where MEMS inertial sensors are used for active and passive safety systems as well as for vehicle body control, e.g. electronic stability program (ESP) and navigation systems, even in cheaper car models. To enhance functionality and reduce size and cost of the sensor modules the development roadmap leads from one axis sensors to multi axis sensors on one chip and further on to a complete inertial measurement unit (IMU) on one chip. 3-axis accelerometers are already in production with high volume, but the combination of accelerometers with angular rate sensors in one chip is more difficult due to different operating conditions. This puts strong effort on sensor design and fabrication technology.

To overcome this challenge Fraunhofer ISIT developed for its industrial partner SensorDynamics the technology platform PSM-X2, which allows to combine the fabrication of accelerometers and angular rate sensors on one chip and open the way to a highly integrated fabrication of IMUs. This new concept is realized now with the new combi sensor SD755, which contains, in a first step, one accelerometer and one angular rate sensor. The SD755 is now available on the market (see figure 1 and figure 2) and fulfills all requirements for automotive qualification based on AEC-Q100.

A cross section of the combi sensor is shown in figure 3. Main functional element of the technology platform PSM-X2 is a low stress 11 µm thick polysilicon layer, which defines the movable structure of the sensor (see figure 4). An additional electrode beneath the polysilicon layer is implemented. This gives the opportunity for out-of-plane signal detection or sensor stimulation. The accelerometer and the angular rate sensor are side by

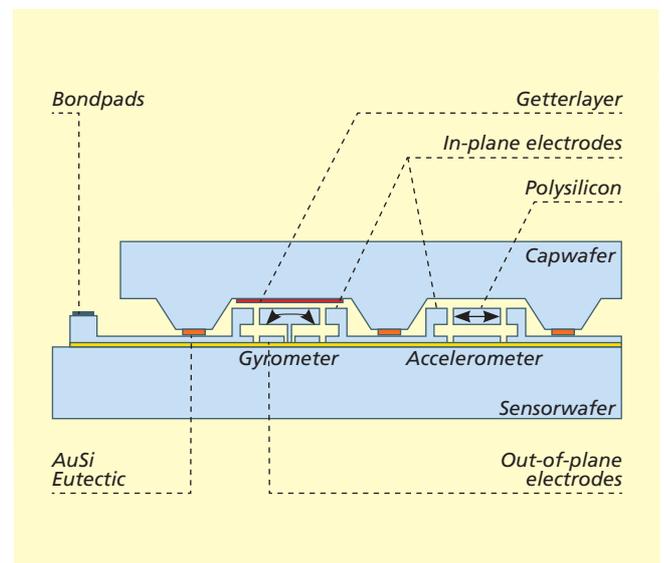


Figure 3: Principle cross section of a PSM-X2 combi sensor. The two neighbored cavities contain movable structures out of 11 µm thick polysilicon. The motion of the structures is detected capacitively.

side on the chip, but gastight separated by individual cavities. The cavities have been prepared with a getter layer to absorb gas molecules out of the cavity volume. Sensor and cavity are prepared on different wafers, the sensorwafer and the capwafer. Bonding of these two wafers is done on waferlevel (Wafer Level Packaging / WLP) by applying a gold silicon eutectic process at about 400 °C. The metallic bondframe induces a hermetic encapsulation of the cavity and the pressure applied during the bond process will persist. By activating the getter layer a cavity pressure up to 10<sup>-6</sup> bar can be assured for the whole lifetime of the sensorelement.

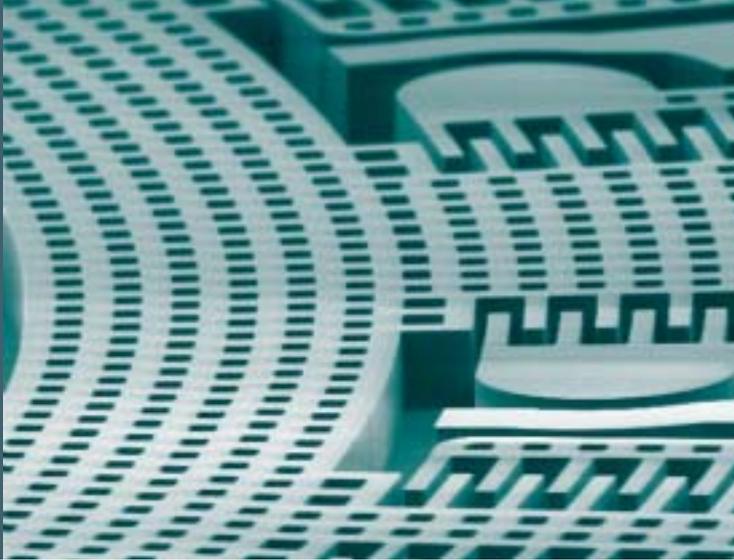


Figure 4: Surface micro machined sensor structure in 11 µm thick polysilicon. The finger electrodes shown in the right are for driving the sensor ring structure. The minimum linewidth of the electrodes is 2 µm.

By combining accelerometers and angular rate sensors on one chip different operating conditions have to be regarded. To guarantee vibration insensitivity and bandwidth for an accelerometer, the cavity pressure has to be in the range of 100-500 mbar, to get a good damping performance of the sensor. The angular rate sensor used at Fraunhofer ISIT is designed like a mechanical decoupled vibrating gyro. To maximize the elongation of the sensor plate by a given stimulation voltage of the ASIC, the drive mode should operate in resonance frequency of the sensor. This will be supported by a cavity pressure of 0,1-1 mbar. It has been shown, that the cavity pressure for optimal operation conditions is quite different for

accelerometers and angular rate sensors and was up to now difficult to realize with one process technology in one chip. The new PSM-X2 process platform offers now the opportunity to fill two adjacent cavities with different pressures on wafer level in such a way, that both sensor types can be run at their optimal operating point. This strategy results in a very compact chipsize of 3.7x 2.7x 1.2 mm<sup>3</sup>.

Based on the described SD755 combi sensor actual multiaxial accelerometers and angular rate sensors are now under development at the Fraunhofer ISIT. A complete highly integrated IMU can be expected on the market in about 1-2 years.

Table 1 shows the important performance data of the combi sensor, which key benefits are mechanical robustness, a wide temperature range and high longtime stability.

**Performance data of combi sensor (LSB: Last Significant Bit; FS: Full Scale)**

Parameter	Angular rate sensor	Acceleration sensor
Measurement range 1	± 100 °/s	± 2 g
Measurement range 2	± 300 °/s	± 5 g
Resolution of measurement range 1	0,0039 °/s/LSB	207,1 µg/LSB
Resolution of measurement range 2	0,0156 °/s/LSB	414,2 µg/LSB
Signal to noise (measurement range 1)	< 0,1 °/s @25 Hz	< 2 mg @40Hz
Sensitivity error	± 2 %	± 2,5 %
Linearity error	± 0,2 % FS	± 0,2 % FS
Offset error @25 °C incl. aging	0,5 °/s	0,03 g
Cross sensitivity against rotation	2 %	-
Cross sensitivity against acceleration	0,1 °/s/g	2 %
Recovery time after 50 g shock	5 ms	
Shock stability in use	1500 g	
Temperature range	-40 °C to +125 °C	
Interface	SPI	



Figure 3: Cross section of a waferlevel packaged 2D microscanner.

### WAFERLEVEL VACUUM PACKAGED MICROCANNERS

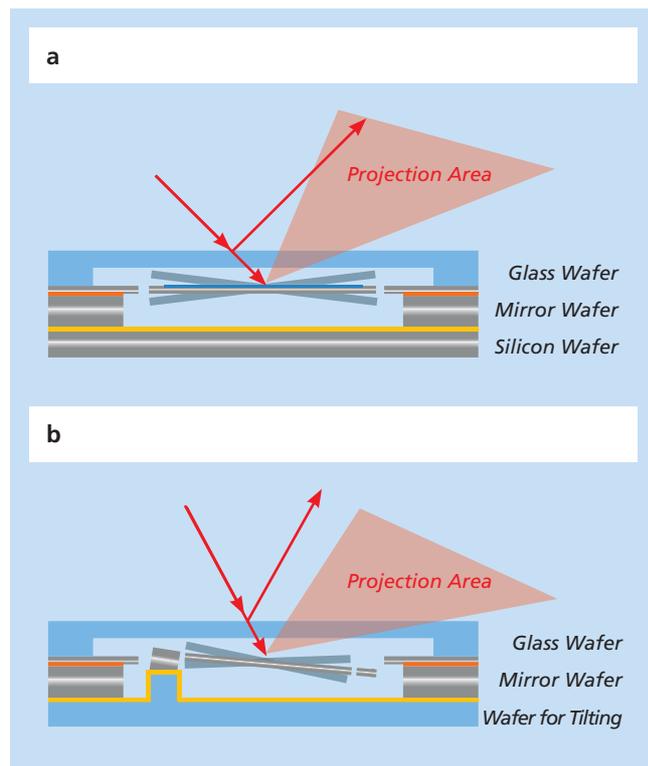
Double-Axis micromirrors are versatile instruments for mobile projection and detection applications. Hermetic packaging is essential to protect the sensitive devices against contamination by particles, fluids or gases during operation. Additionally, mass producibility only becomes feasible by realizing hermetic encapsulation on a waferlevel.

Due to the fact that the scanners are to be used in optical applications the hermetic encapsulation must also meet

high demands in respect to the optical quality. Distortionless transmission of light can only be achieved by perfect optical flatness, low defect rate and wise selection of incorporated materials of the waferlevel package.

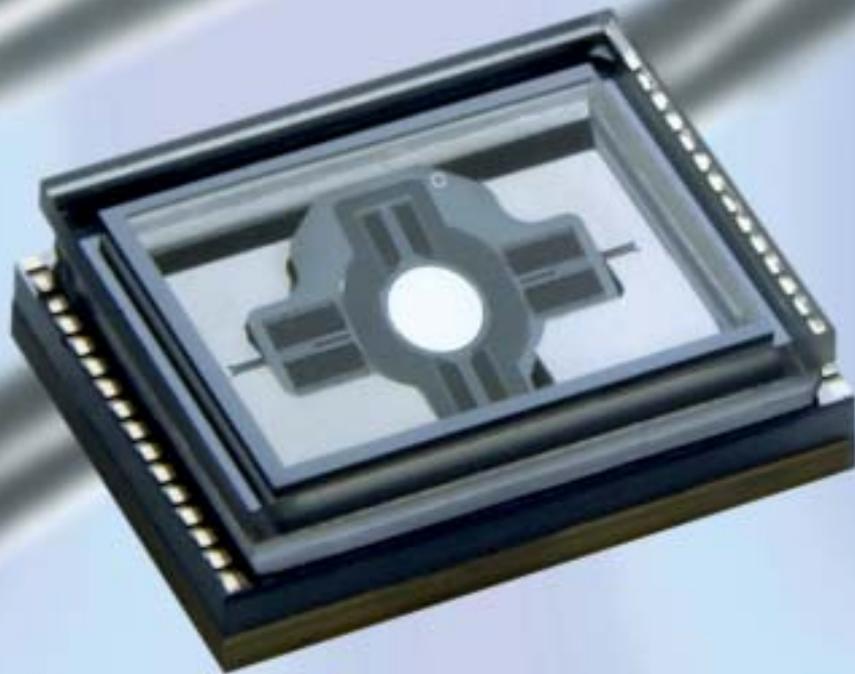
Fraunhofer ISIT has developed a sophisticated manufacturing technology for the production of waferlevel vacuum packaged electrostatic actuated microscanners. It is based on modern surface micromachining with thick polysilicon layers and deep dry etching (DRIE), an unique glass structuring technology and state-of-the-art waferbonding processes. The fabricated scanners feature extraordinary high optical scan angles ( $> 50^\circ$  tot.) at high scan frequencies of up to 100 kHz while their operation requires low driving voltages of only a few volts.

Figure 1: Unwanted reflexes of the laser spot generated by reflection on the package surface (a) and the spatial separation of image and reflected laserspot by static tilting of the mirror plate (b).



Recently, several technological developments have further expanded Fraunhofer ISIT's Know-How in microscanner technology. The optical efficiency of the devices has been enhanced by the integration of protected silver as mirror plate coating and an in-house deposited antireflective coating based on PECVD layers of the cap glass wafer.

However, in case the scanners are used in laser based image projection an always-remaining reflection of the laser spot on the package surfaces disturbs the image (see Figure 1). In order to prevent this effect, the scanners can be statically tilted by an angle of up to  $15^\circ$  mechanical. Therefore, the scanners are surrounded by an auxiliary frame, which is mechanically deflected during waferbonding. Hence, the static inclination of the mirror plate allows the spatial separation of the unwanted reflexes and the image.



*Figure 2: Waferlevel packaged  
2D microscanner with static  
inclination.*

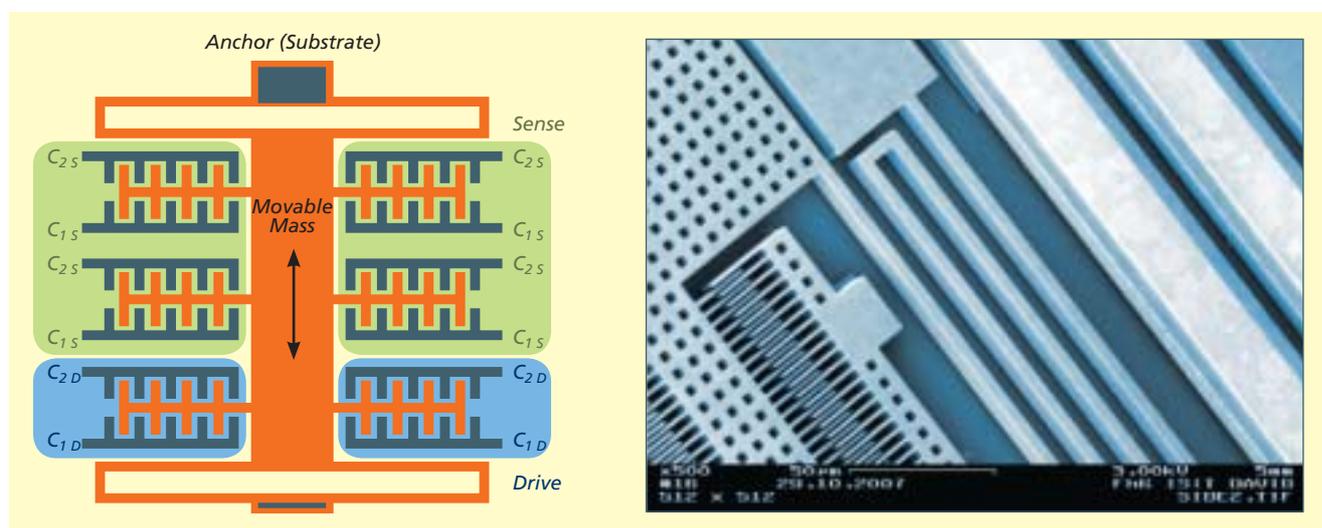
## DICING OF FRAGILE MEMS STRUCTURES

Conventional singulation of MEMS (Micro Electro Mechanical System) devices is carried out after protection of the fragile structure. Particles generated during dicing can block mechanical movements, mechanical load or vibration can deteriorate hyperfragile structures and, for example for bio-MEMS, cutting fluid can interact with sensitive layers. Protection is mostly done either by a capping process or by a resist, both on a wafer level. Membrane sensors for flow and pressure are usually protected by a temporarily layer, which is removed afterwards. However, this procedure can cause significant yield loss. Inertial sensors, micromirrors and rf-MEMS are permanently protected by a capping layer essentially for functional reasons. Devices which have open structures on both sides, generally afford new techniques because sensitive structures cannot be enclosed completely since it could hinder functionality. Mahoh IR laser technology for (stealth) dicing is claiming to be the ultimate separation technology for open and fragile structures.

Separation takes place by generating a polycrystalline area with a high dislocation density within the wafer along the dicing line. Subsequent wafer expansion via tape avoids any particle generation. Typical examples are microphones as well as ink jet printheads, which are already fabricated in mass-production.

Recently a chip to wafer assembly has been proposed in the European project DAVID (Downscaled Assembly of Vertically Interconnected Devices), in which a sensor chip is bonded face down on top of an ASIC wafer (3-D integration of MEMS and ASIC). Therefore, it is needed to singulate before the MEMS chip is placed on the ASIC wafer. This MEMS contains a surface micromachined structure with features in the submicron range which is very sensitive against particle contamination. For a characterization of the dicing process with respect to particle generation, chipping occurrence and environmental conditions, the complete process flow has to be taken in mind: the dicing and the separation of chips by expansion has to be carried out in environments with at least a cleanroom class 100. The further transport to the pick and place tool and the chip placement has to be done also under controlled conditions. In the following a description of the

Figure 1: Schematical view of the test structure in surface micromachining technology (left side). On the right side a close up of the real structure taken with an SEM is shown.



test structure for the evaluation of the stealth dicing method is given. The mechanism of heat generation inside the silicon wafer while leaving the surface unattached will be explained. The subsequent method of separation and wafer conditions therefore will also be commented.

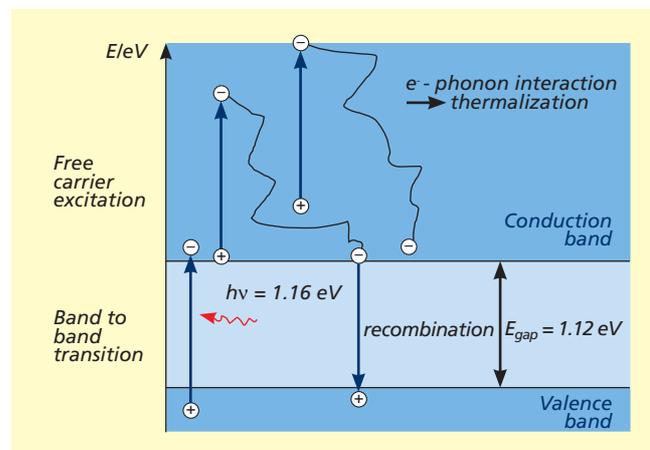
### Description of the Test Structure

The demonstrator is shown in figure 1 in a schematical view (left) and in a close up of the processed structure (right). This MEMS contains among some test structures a surface micromachined resonator with minimum linewidth of  $0.8 \mu\text{m}$  in a comb structure. This features the Fraunhofer ISIT epitoly-Si process with a thickness of  $11 \mu\text{m}$ . The aspect ratio of this device is up to 1:14 and extraordinarily sensitive to any particle contamination and thus appropriate for evaluation purpose. In the scope of the DAVID project the MEMS chips have to be separated before they could be bonded on an ASIC wafer. It is assumed that only stealth dicing showed the potential to solve this ambitious task. The stealth dicing method, however, is a relative new separation method and mostly not well understood. Therefore the mechanism of separation is explained in a phenomenological view. It will be focused on the optical processes which generate the heat for the conversion of the crystalline to a highly distorted polycrystalline phase of the material, which acts as a precursor for the separation.

### Stealth Dicing

A laser beam is focused inside the bulk Si material and introduces in the dicing lanes a high density of dislocations without any material ablation. Subsequent the wafer is mounted on a tape which by expansion leads to controlled fracturing along these lanes. This so called stealth dicing is a singulation method, separating chips from a wafer without generating particles, damage, or heat in the device area. Local laser absorption is induced in the vicinity of a focal point inside the wafer bulk using the temperature dependence of the absorption coefficient. Only the neighbourhood of a focal

Figure 2: Schematic view of the excitation mechanisms for the photon – electron interaction



point is heated and reaches higher temperature than the melting point. By rapid cooling, cracks are generated which act as precursor for subsequent singulation by expansion of the wafer. To explain the question how the melting process is started, some remarks are addressed concerning the interaction of light (photons) with matter. Laser ablation processes mostly are done with wavelength below  $1 \mu\text{m}$ . The cross-section for absorption is high in this area, respectively the transmission goes down to zero. (The transmission of light is the inverse of absorption, neglecting reflectance.) In the range above  $1 \mu\text{m}$  the transmission increases strongly. For the stealth dicing a short pulsed IR laser with a wavelength of  $1.064 \mu\text{m}$  ( $E=1.16 \text{ eV}$ ) is applied. In the transition range the absorption is low but not zero since it is located in the fundamental edge of the Si semiconductor. This energy is slightly above the bandgap ( $E_{\text{gap}} = 1.12 \text{ eV}$ ) of Si at room temperature. The absorption of photon energy and its conversion to lattice heat is dominated by the creation of electron – hole pairs:

- direct optical absorption of photons with energies higher than the bandgap energy  $E_{\text{gap}}(T)$ . For silicon this is an indirect transition from valence- to conduction band (under the assistance of phonons). The population of the conduction band with electrons makes free carrier absorption possible.

- optical induced free carrier absorption is a transition from conduction band to higher states. For Si and laser pulses in the nanosecond scale free carrier generation is more effective as recombination of carriers. The heating of the lattice by thermalization of excited electrons through collisions with phonons and other carriers is dominant as compared to carrier recombination. The excitation steps are illustrated in figure 2, showing the band to band transition, free carrier excitation, thermalisation and recombination of electrons. For the onset of heating up it is therefore necessary that the generation of electron-hole pairs is higher than recombination and thermalisation effects. According to these requirements the appropriate laser parameters have to be chosen. The laser power controls the number of initially excited electrons. The right pulse length of the laser is important for the limited diffusion of the thermal wave, which extends to a few  $\mu\text{m}$  for pulses in the ns range. The appropriate power and a focus point at the diffraction limit (smallest possible extension of laser beam) are determining the photon density. After the heat is generated locally, the absorption probability increases exponentially with temperature thus creating a nonlinear heating effect, which in result provides enough energy for local melting and evaporation processes. Once this highly distorted area is created, then after rapid cooling the distribution of compressive and tensile stress enables the development of vertical cracks. However, the surface remains unattached since the photon density aside the focus area is too low to create an excitation rate higher than the recombination rate. This

is the extraordinary difference to laser ablation processes, in which material is removed from the wafer surface down to the bottom, thus generating debris along the dicing line.

### Separation of Chips

After laser treatment the unseparated wafer has to be fixed on a dicing tape. This tape is then expanded by a cylindrical stage in order to singulate the chips. This process is shown here schematically in figure 3. However, in the real world difficulties have to be recognized. The wafer thickness, the doping level and, very important, the residual layers on the surface of a wafer can cause severe problems for the separation process. During the design of the MEMS devices the designers have not always been aware of the problems of dicing. In the case of stealth dicing we need to consider some elements of “design for manufacturing”.

### Design for Manufacturing

The DAVID project is a development project in which the process flow was improved from run to run. In first loops some areas on the wafer, not used for active devices, were covered with aluminum (see figure 4 a). A singulation by tape expansion was not possible. After a mask redesign and subsequent processing this error was corrected. Afterwards it appeared that the whole wafer surface was covered with thick epipoly-Si with a thickness of  $11\ \mu\text{m}$ . As an outcome the crack propagation in mono-crystalline Silicon (the substrate) is interrupted when it approaches the poly-Si region. Strong deviations from

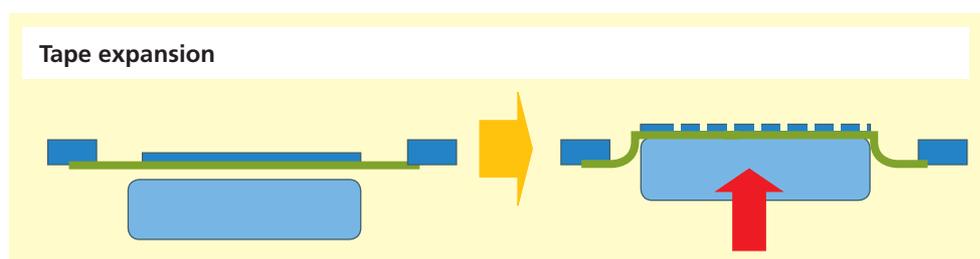


Figure 3: Schematic view of the chip separation by tape expansion.

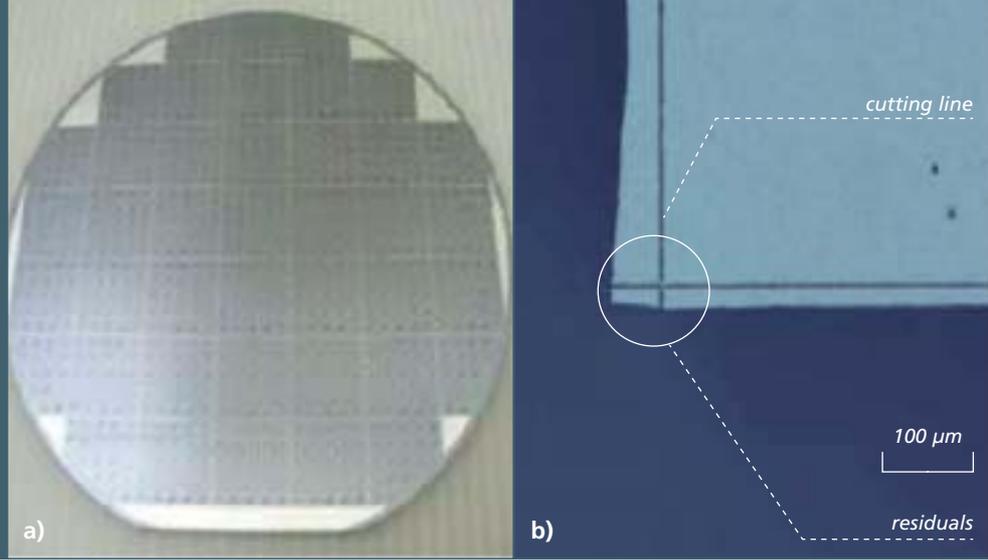


Figure 4: MEMS wafer with aluminum residuals (a) and with displaced cutting lines due to thick (11  $\mu\text{m}$ ) epipoly-Si on the surface (b).

the cutting line are the results, as shown in figure 4 b. The mask for the appliance of the DRIE process for structuring the thick epipoly-Si film had to be redesigned considering these experiences. The aluminum and epipoly-Si removal enabled a successful separation of the chips. From this experience it can be recommended, that in the dicing lines:

- no aluminum, in general no metals, are allowed. Strong absorption effects prevent a successful focusing of the laser beam inside the wafer.
- no active layers, in particular, thick layers for surface micro-machining, are allowed, because linear crack propagation is hindered.

Considering all the aforementioned details, first results were achieved for the stealth dicing of open surface micromechanical structures. Performing an optical inspection of the separated chips on the tape, no significance of particle/debris on the wafer front side were detected. For the inspection in a scanning electron microscope (SEM), a commercial pick and place tool was used. This lifts the chips with a tiny vacuum nozzle and transferred them under controlled atmosphere. Some damage appeared on the chip surfaces due to an arbitrary touch down of the pick and place tool, which have to be prevented in future. For the inspection a statistical probing of the chips from different places on the tape was performed. All of them have been found to be in an excellent condition.

Two SEM photographs are shown in figure 5 as representatives for the different investigated samples. There was no chipping, peeling and the cutting quality appeared perfect, although some thin layers remained on the backside of the wafer. Due to the process flow these are a sacrificial layer (silicon oxide) and a buried poly (Silicon), all together in a range of about 2  $\mu\text{m}$  thickness.

### Summary

The demonstrator, the DAVID device, is fabricated in an R&D project and reveals some drawbacks: design for manufacturing has not been considered. Nevertheless the results from stealth dicing of these devices look very promising. The results from optical and SEM control show no particles and chipping effects. Therefore stealth dicing is viewed as the ultimate solution for singulation of open MEMS chips. In addition a short explanation of the heating process during laser processing has been given on the basis of the interaction of light with matter.

### Acknowledgements

We would like to acknowledge very gratefully the support by Accretech, Tokyo which performed the Mahoh (stealth)-dicing. The presented work is part of the DAVID project, which is funded by the European Commission within the Sixth Framework Programme (ref. IST-027240).

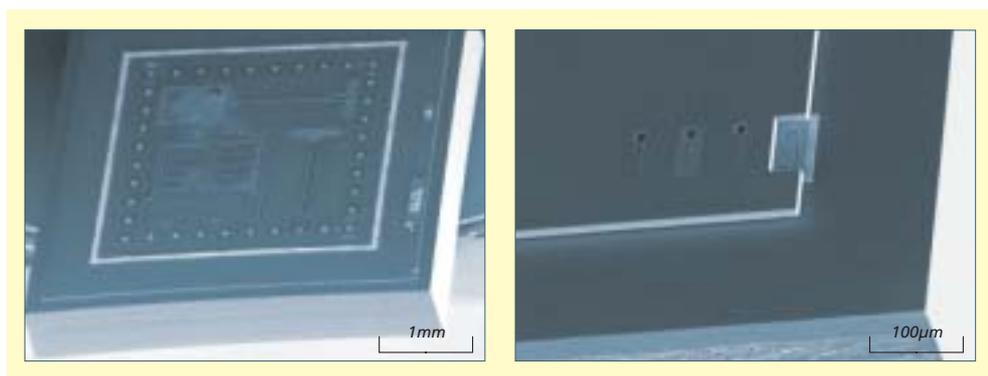


Figure 5: SEM micrograph of a singulated MEMS chip after successful stealth dicing (left), a close up of this chip is shown also (right).

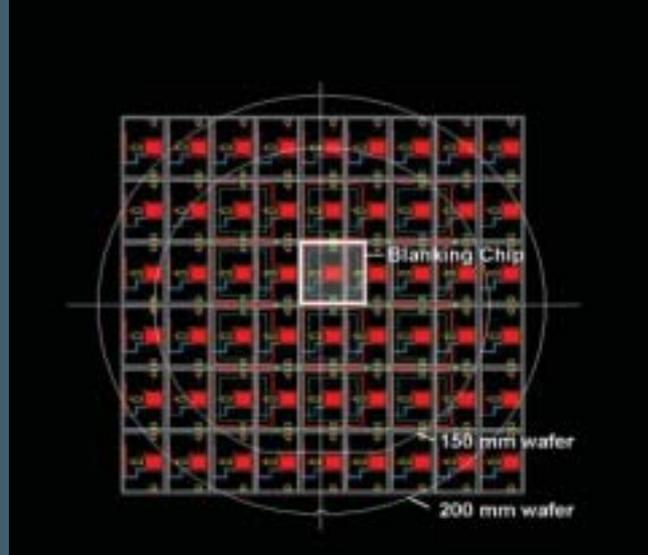


Figure 2: Wafermapping of 200 mm and 150 mm wafer.

### PROJECTION MASKLESS LITHOGRAPHY (PML2): FABRICATION OF A PROGRAMMABLE APERTURE PLATE SYSTEM WITH MONOLITHICALLY INTEGRATED DRIVING ELECTRONICS

Optical lithography has provided the semiconductor industry with ever-finer features. Most recently, resolution-enhancement techniques for optical masks, especially proximity correction and phase shifters, allowed 193 nm-wavelength optical lithography to meet the demand of the 45 nm-half-pitch (hp) technology node.

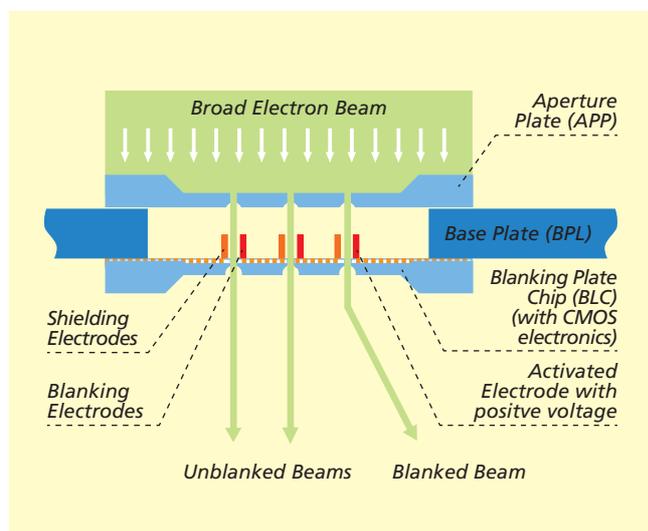
For smaller features in the future, the International Technology Roadmap for Semiconductors predicts that 193 nm water-immersion lithography – most likely combined with double patterning – will be used for 32 nm-hp device production starting in 2010. But for the 22 nm-hp node, to be in production in 2012, several methods are still candidates: 193 nm water-

immersion with double exposure and patterning, 193 nm immersion lithography using-high-index fluid (193 i+), extreme ultraviolet lithography (EUV), nano-imprint lithography (NIL), and projection maskless lithography (PML2) using electron or ion irradiation. Main advantages of maskless lithography are the avoidance of expensive and time consuming mask fabrication and a fast and flexible realisation of pattern layouts especially in the development phase.

PML2 is a potentially cost-effective multi electron-beam solution for the 32 nm-node and beyond. PML2 is targeted on using hundreds of thousands of individually addressable electron-beams working in parallel, thereby pushing the potential throughput into the wafers per hour regime. With resolution limits of less than 10 nm, PML2 is designed to meet the requirements of several upcoming tool generations.

A PML2 proof-of-concept setup was realized by IMS Nanofabrication, Vienna, Austria, within the framework of the European RIMANA (Radical Innovation MASKless NANolithography) project. It contains all crucial components of a full-fledged PML2 tool and unambiguously demonstrates the operability of multi electron-beam projection optics with 200x reduction. In the PML2 proof-of-concept system a programmable aperture plate system (APS) is used to generate more than 43,000 switchable beams of micrometer size which are guided through electrostatic- and magnetic-lens optics with 200x demagnification. Thus, thousands of demagnified electron beams are projected in parallel onto the resist-coated wafer.

Figure 1: Principle of aperture plate system.



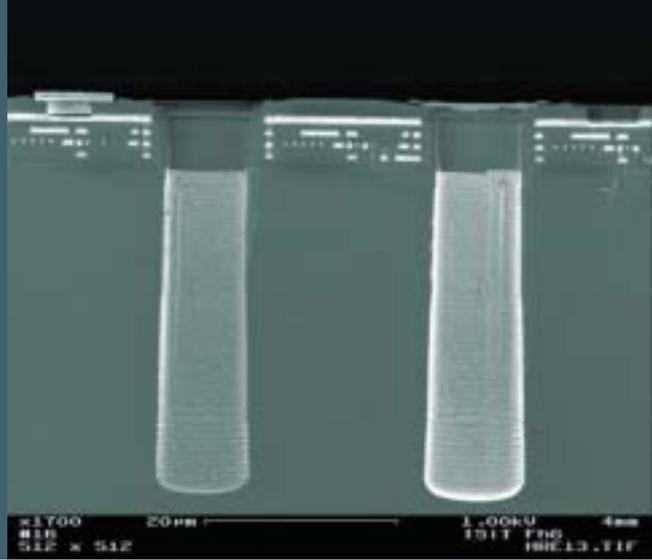


Figure 4: Cross section of the blanking chip with etched apertures close to the CMOS circuit.

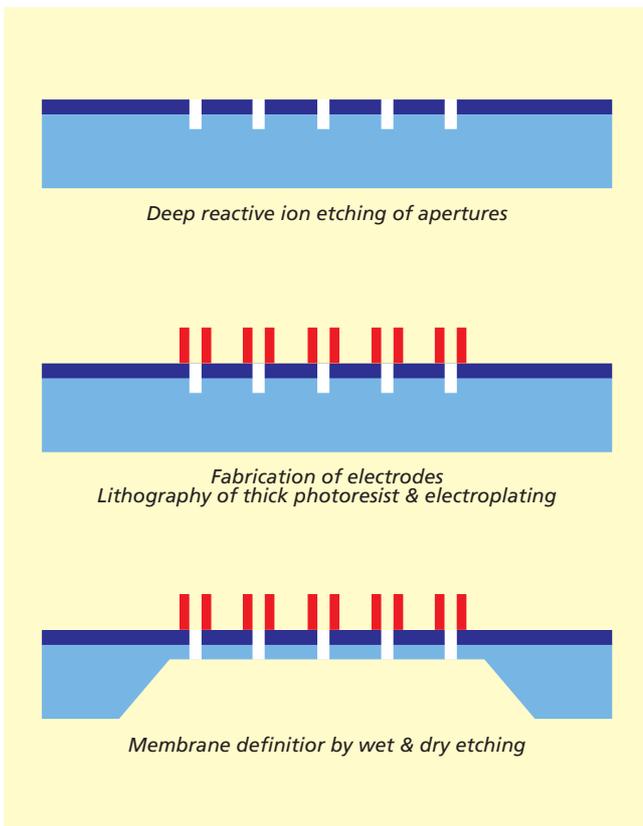


Figure 3: Key MEMS processes for the blanking plate fabrication.

### Aperture Plate System (APS)

One central part of the projection maskless lithography tool is the programmable aperture plate system. The APS replaces the mask of a conventional lithography tool. Within the RIMANA project ISIT has evaluated and developed the fundamentals of a MEMS fabrication process for the compact aperture plate system. The APS constitutes the object in the imaging electron optics. It consists of two silicon plates which exhibit a periodic staggered array of apertures. Individual beamlets are formed by the aperture plate (APP) while dynamic structuring is realised by the blanking plate (BLC) below. Deflection electrodes at every aperture allow for individual control of each beamlet. The deflected beams are blocked at a stopping plate further down the electron optical column; only undeflected beams reach the wafer surface. The principle of the aperture plate system is given in figure 1.

The blanking plate is driven by a stream of pixel data prepared off-line in advance and transmitted via a high speed data path from an outside storage equipment onto the plate. Using specific driving electronics for each aperture every beam can be individually switched on and off. The switching of the individual beamlets, i.e. in the range of nano seconds, requires a high precision. The exposure concept foresees that the APS is able to switch 43,000 electron beams in parallel while the exposed wafer moves continuously. Thus, the amount of data to handle is in the range of several Tbit per second. The large amount of electrodes on the APS cannot be controlled by outside electronics which is connected to the MEMS-chip by wire or by flip-chip bonding because it is impossible to directly connect more than several hundred electrical contacts. Therefore only monolithically integrated driving electronics next to the deflection electrodes are able to fulfill this challenge.



Figure 5: Top view of electroplated blanking and shielding electrodes close to apertures.

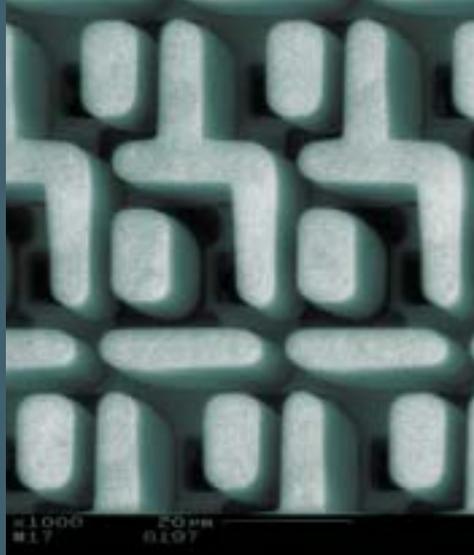


Figure 6: Detail of electrode arrangement.

In close cooperation with the RIMANA project partner IMS Chips, Stuttgart, Germany, ISIT has designed an electronics concept which considers the specific layout of the aperture cells. The layout of the electronics is based on the geometrical specifications and the electrical requirements of the blanking chip. The area of each aperture cell is  $30 \times 30 \mu\text{m}$  and contains the electronics for the blanker activation. It has been elaborated that a  $0.25 \mu\text{m}$  CMOS technology with four metal layers is suitable for the electronics realisation supplying a maximum tolerable voltage of 3.3 V. For the fabrication of the chips the foundry service of the United Microelectronics Corporation (UMC) Taiwan was chosen.

In order to fit the different technologies (CMOS at UMC and MEMS technology at ISIT) the design work had to consider the position of the chips on the wafer, the critical dimensions of the patterns, the overlay accuracy of the different exposure tools at UMC and ISIT, a homogeneous distribution of metal layers over the wafer and the implementation of specific alignment marks for the mix and match lithography and test structures.



The CMOS fabrication at UMC has been performed on 200 mm silicon wafers. After electrical and functional testing of the processed wafers a sawing from 200 mm diameter to 150 mm was necessary for further processing by means of MEMS technology of the apertures, electrodes and membrane definition at ISIT. Figure 2 shows the arrangement of the blanking chips on the 200 mm and 150 mm wafer.

In principle the MEMS fabrication of the blanking plate chip comprises three main processing parts (figure 3): (i) deep reactive ion etching of high aspect ratio apertures, (ii) fabrication of  $32 \mu\text{m}$  high blanking and shielding electrodes by electroplating and (iii) anisotropic silicon wet etching and reactive ion etching for the realisation of the membrane with a thickness of  $40 \mu\text{m}$ .

In figure 4 a cross section of the CMOS blanking chip plate is shown. The upper part depicts the CMOS electronics with four metal layers. Apertures with  $7 \mu\text{m}$  openings and the required retrograde profile have been performed by means of deep reactive ion etching prior to electroplating of the metal electrodes and prior to membrane etching.

The blanking of the pre-formed electron beams is done by electrostatic deflection. The available deflection voltage from the monolithically integrated CMOS driving electronics is limi-



Figure 7: Assembled aperture plate system.

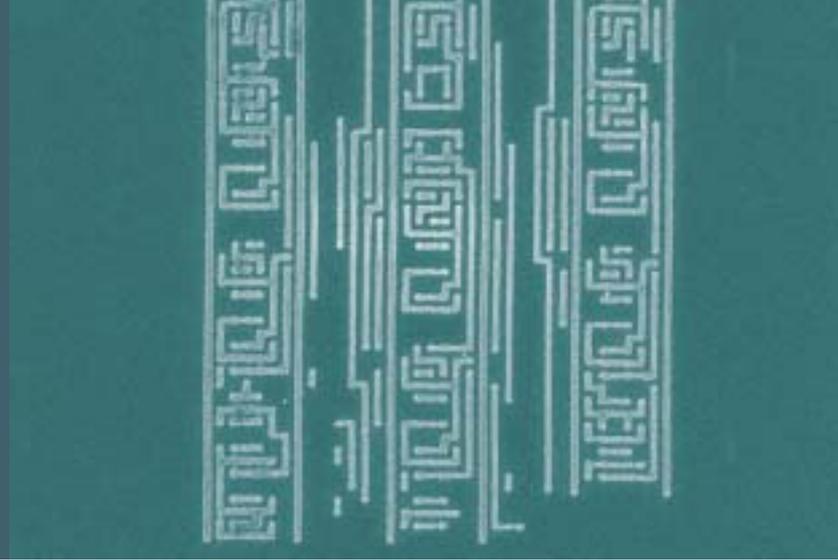


Figure 8: HSQ resist structures of down to 50 nm linewidth.

ted to 3.3 V. In combination with a required deflection angle of nearly 0.5 mrad the height of the blanking electrodes has been calculated to be in the range of 30  $\mu\text{m}$ . Based on an AZ type photoresist a sequence of lithography and electroplating processes has been established which results in a precise fabrication of the metal electrodes fulfilling all requirements regarding the high aspect ratio, vertical and smooth sidewalls and robustness during further processing of the blanking chip. Figure 5 and 6 show the arrangement of electroplated blanking and shielding electrodes after resist removal.

The pre-assembled compact programmable aperture plate system is shown in figure 7. The integration technology for the APS plates covers the assembly and interconnection of (i) the blanking plate chip on a base plate, (ii) the plug connection and wire bonding (not shown in figure 7), and (iii) the precise alignment of the beam forming aperture plate (compare figure 1).

The characterization of compact aperture plate systems in test benches at IMS Nanofabrication showed full electrical and electron-optical functionality. Applying a voltage of 3.3 V to the electrodes led to a static beamlet deflection of up to

1 mrad which suits well to the blanking demands within the RIMANA tool. Additionally, on/off beam switching frequencies of 1.1 kHz and 4.8 kHz have been investigated leading to a beamlet deflection angle within the measurement accuracy of  $\pm 0.1$  mrad.

A nearly defect-free MEMS fabrication of the blanking plate chip yielded in a functionality of aperture plate systems of up to 99.96 %. Since the writing strategy in the RIMANA tool is performed in a redundant way these few failures are far below the tolerable rate of failures. A result of dynamic patterning performed in this way with the RIMANA tool at IMS Nanofabrication, Vienna with 10 keV beamlets into 50 nm thick negative tone HSQ resist is displayed in figure 8. In first experiments structures down to 50 nm have been demonstrated. Work is in progress to go even lower.

Within the RIMANA project the complex MEMS fabrication process for the blanking plate chip with integrated CMOS electronics has been established with an excellent yield. Further work within the follow-up project MAGIC (MAskless lithoGraphy for IC manufacturing) has a focus on a sophisticated compact aperture plate system with 256,000 individually switchable beamlets in order to prepare for next generation lithography applications.

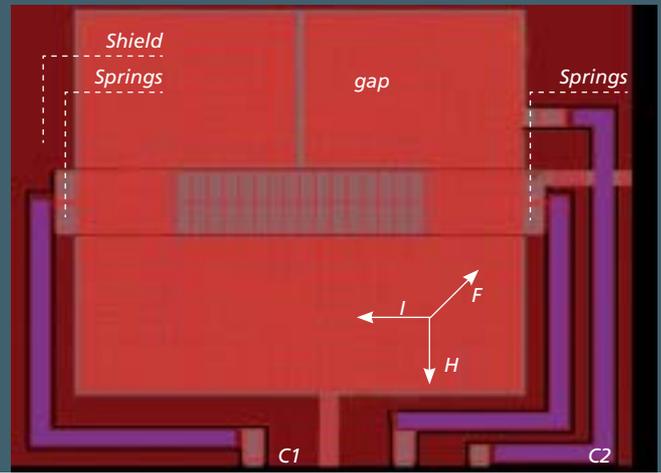


Figure 3: Layout of the magnetometer.

## DEVELOPMENT OF MAGNETOMETER BASED ON MEMS TECHNOLOGY

Magnetic field sensors together with accelerometers and gyroscopes can be used to bridge short times when a GPS-modul is not working, like e.g. in a tunnel, a street canyon or streets through a thick forest. In addition one may think navigation systems integrated in smart phones that have to work in large airports or railway stations too. Here without a working GPS an alternative signal has to be used, inertial sensors and the earth magnetic signal will be taken.

### Working principle

The working principle of a magnetic field sensor can be easily explained based on the following physical experiment (see figure 1). A metallic wire located in a magnetic field is displaced just in the moment when a current flows through it. It can be observed that the amount of displacement is directly

proportional to the density of the magnetic field vector. The displacement force is called "Lorentz-force" and can be described as

$$\vec{F}_L = I \cdot (\vec{l} \times \vec{B})$$

where  $l$  is the length of the wire,  $I$  the amount of current, and  $B$  the magnetic field.

As a result of the small Earth magnetic field ( $B \sim 50 \mu\text{T}$ ), the usable length ( $l \sim 1 \text{ mm}$ ) and the low available current the Lorentz-force is extremely low, so the sensor developed at ISIT takes advantage of the gain effect of a resonant system. Instead of having a static current the flow is modulated at the resonance frequency wres of the sensors spring mass configuration. With the assumption that the vectors are

Figure 1: Principle of Lorentz-force.

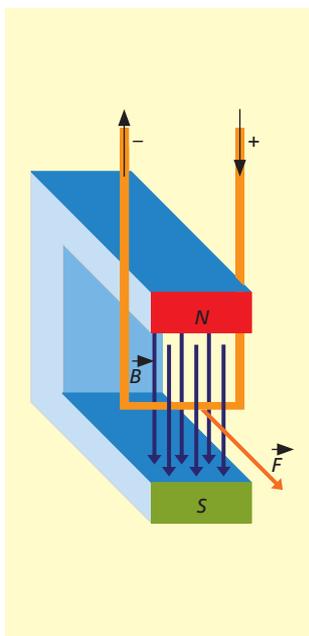
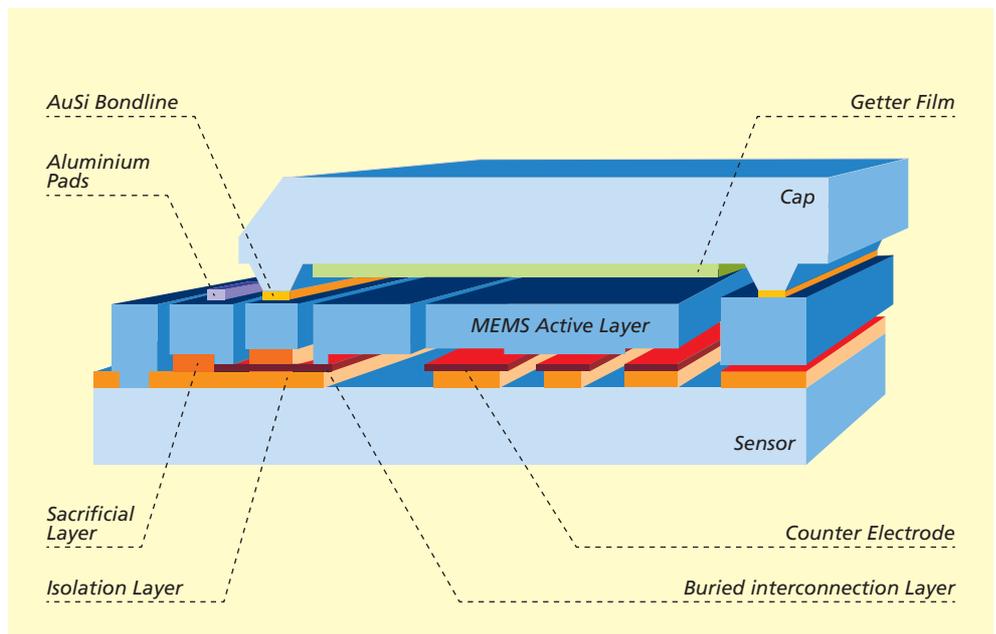


Figure 2: Cross section of a PSM-X2 capped sensor chip.



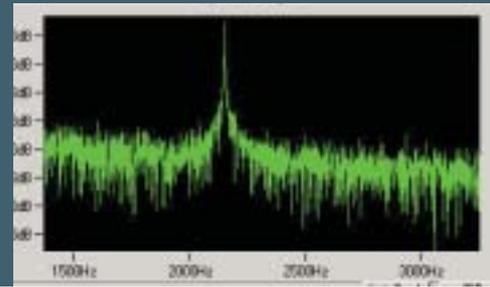
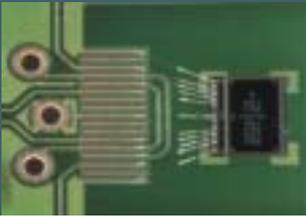


Figure 4:  
a) Magnetometer in test setup  
b) Detail view of the magnetometer

Figure 5: Measurement setup with Helmholtz-coil.

Figure 6: Fourier transformation showing that the magnetometer is working in resonance.

orthogonal to each other the Equation of the Lorentz-force can be reordered as follows:

$$F_L = l \cdot B \cdot \hat{i} \cdot \sin(\omega_{res} \cdot t) = \hat{F}_L \cdot \sin(\omega_{res} \cdot t)$$

The resulting force drives a movable mass to an appropriate oscillation. Driving the structure under vacuum the reduced damping leads to an increased oscillation amplitude with the quality factor (here  $Q \sim 10,000$ ) as a direct multiplier.

### Design

The sensor has been realized with the surface micromachining process platform for vacuum packaged sensors (PSM-X2) developed at ISIT (see figure 2). The current flow is fed on the sensor via two springs along the lower part of the movable mass. Due to the applied B-field the mass is forced to an out-of-plane oscillation. This oscillation can be monitored by reading out the change of the differential-capacitor between the movable mass and the counter-electrodes below.

### Test Setup

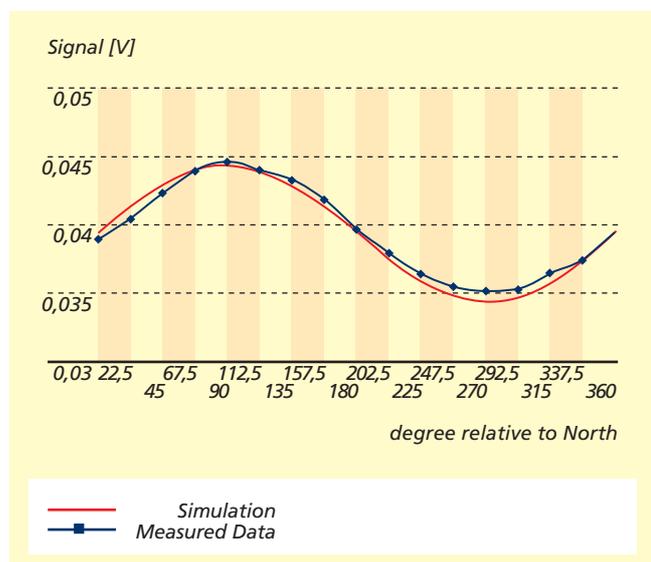
In a first step the sensor has been tested using a simple readout electronic realized on a printed circuit board (PCB) including the sensor that is bonded directly on the PCB (see figure 4). The sensor electronic automatically detects resonance frequency (see figure 6) of the sensor and locks the sinusoidal current flow at this operating point. To test the sensitivity of the sensor on applied magnetic fields the PCB was placed inside a Helmholtz-coil (see figure 5) where the field can be adjusted very precisely to calibrate the appropriate scale factor.

### Results

The demonstrator shows impressively the sensitivity of the sensor system on a change of the applied magnetic field. According to the needs in a targeted navigation system it was possible to resolve the position relative to the magnetic north accurately as figure 7 shows.

The sensor has been developed within the European project MINAMI, an Integrated project in the 6th working programme, as part of a 9D-Inertial measurement unit. (3D Gyro, 3D Accl, 3D Magnetic

Figure 7: Measurement of the earth magnetic field with sensor X1.



# IC-TECHNOLOGY

Efficient use of Electrical Energy  
Innovative Power Systems

- R&D Projects for Power Electronic Applications
- Cooperation between Industry and R&D institutions
- Workshops and Seminars



## CENTER OF COMPETENCE FOR POWER ELECTRONICS IN SCHLESWIG-HOLSTEIN

Power Electronics is one of the key technologies for the next decades by all the well known reasons of energy saving, reduction of CO<sub>2</sub> emission and stepwise substitution of fossil energy by CO<sub>2</sub>-friendly energy. In order to strengthen Power Electronics in Schleswig-Holstein a joint activity was initiated by the Ministry of Economy and the Fraunhofer Society within the frame work of "Zukunftsprogramm Wirtschaft Schleswig-Holstein".

It is the intention of bringing together companies, academia and Fraunhofer ISIT for the purpose of encouragement technical innovation, cooperation between partners and build up of knowledge and human capital in order to enhance the economic development in the field of Power Electronics.

In a first phase a start up project was initiated by ISIT which brought together competent partners for the development of new components to be used in power converters for industrial applications.

Application specific power semiconductor devices, new assembly and module techniques, simulation and reliability testing are the key activities the Center of Competence is focussing on.

The start up consortium is composed of the partners shown in figure 1. In a first phase it was intended to create a complementary team of industries, universities and institutes located in Schleswig-Holstein which are covering the entire value added chain from semiconductor devices up to power electronic systems.

The Center of Competence for Power Electronics will be open up stepwise for further partners with the aim of creation a partner network supporting

- Bilateral and multilateral cooperation
- Definition and accomplishment of R&D projects
- Enhancement of competitiveness
- Transfer of knowledge
- Education by seminars and workshops (diploma and doctoral thesis)
- Job creation

The cooperation with small and medium enterprises will be specially supported by the Center of Competence.



Figure1: Start up consortium for the Center of Competence for Power Electronics Schleswig-Holstein.

## CMOS COMPATIBLE NANO STRUCTURES FOR CNT TRANSISTORS

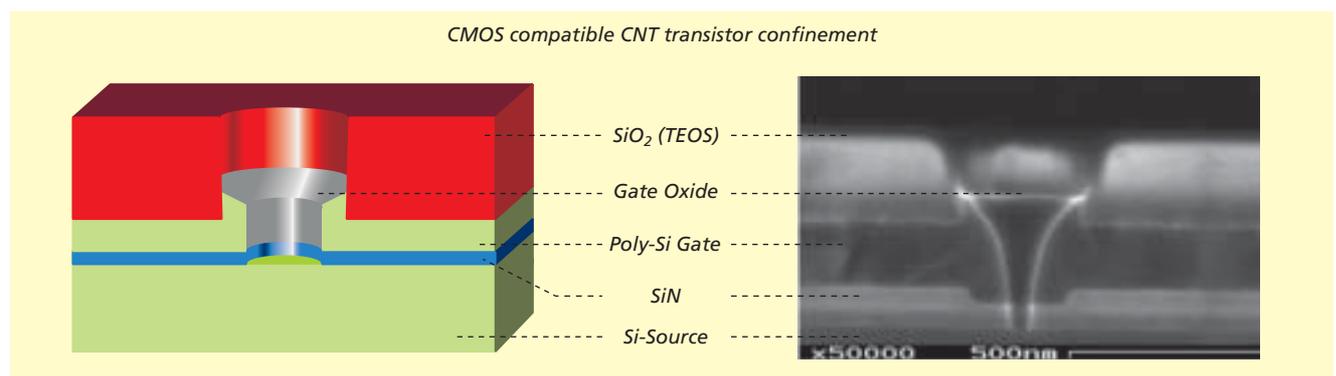
Over the past decades the scaling of transistor geometry was following the Gordon Moore Law by shrinking the minimum dimensions by a factor of 0,7 with every new chip generation. Now, the implementation of ultra high resolution immersion lithography (ArF 193 nm) opens up the path for the next CMOS generations, namely the 32 nm and 20 nm technology node. However, the limits of transistor scaling as it was successfully applied since the early beginning of CMOS technology becomes obvious. Regardless of the new technologies the miniaturisation of Silicon based transistors will reach some fundamental limits probably within the next decade. The prediction of the limits of CMOS scaling was motivating an intense research activity for alternative devices and materials such as Si-nanowires and Carbon Nano Tubes (CNT) as possible candidates for new transistor architectures.

Single Wall Carbon Nano Tubes (SWCNT) consisting of a single graphene layer wrapped up to a tube with a diameter in the nano meter range. Graphene is a one atom thick hexagonal crystal lattice of  $sp^2$ -bonded Carbon atoms. Depending on the

orientation of the wrapped up graphene cylinder (chirality) the CNT can be either metallic or semiconducting. For growth of CNTs CVD and PECVD processes were developed using decomposed hydro carbon. For the nucleation of the growth Ni, Fe or Co catalysts are needed. The alignment of the CNT growth direction is achieved by use of a vertical oriented electric field.

End of the nineties it was shown that SWCNTs can be operated as Field Effect Transistors using the CNT as a nano channel controlled by an insulated Gate electrode. Next to the CNT dimension of less than 5 nm in diameter, which obviously can create new possibilities for high integration purposes, the main interesting aspect of CNT transistors is the extremely high mobility up to several  $10.000 \text{ cm}^2/\text{Vs}$ . This is due to a quasi 1D transport mechanism with electron scattering lengths in the  $\mu\text{m}$  range. Within the European project (CANDICE) ISIT was developing nano holes as a confinement for CNTs or Si nano wire transistors based on CMOS compatible processes. For this purpose nano holes with dimensions below 20 nm have been realized as confinements for the vertical CNTs. Following the architecture for a vertical transistor the structure is build up from bottom to top in a Source, Gate and Drain configuration.

Figure 1: Realization of a CMOS compatible CNT transistor confinement.





Realization of nano holes in the sub 20 nm regime by side wall spacer formation using amorphous Si.

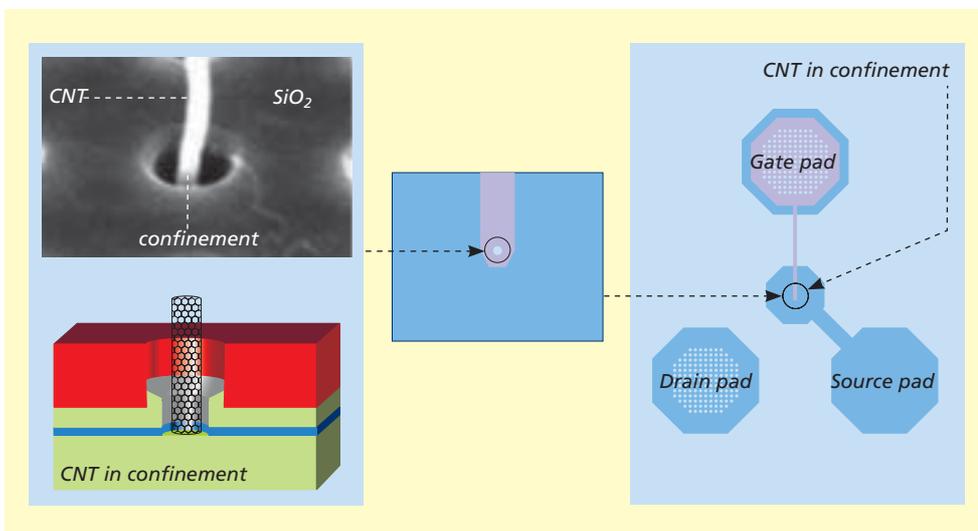


Figure 2: Depiction of a single CNT transistor layout and a SEM picture with a CNT grown out of a nano hole.

In a first step a layer stack is deposited bottom up comprising out of a highly doped Poly-Si Source plate, the SiN Source-Gate isolation, the Poly-Si Gate electrode and the SiO<sub>2</sub> Gate-Drain isolation. Single holes or arrays of holes are then structured into the upper SiO<sub>2</sub> layer (Gate-Drain isolation) and underlying Poly-Si (Gate) with critical dimension in the 0,3 μm range. In a next step a highly doped Poly-Si layer has been deposited for reducing the hole diameter down to the target hole dimension in the nm-range. By anisotropic etching a Poly-Si side wall spacer within the holes is formed which can simply be recessed by Poly-Si overetching. By oxidizing the inner Poly-Si sidewall spacer the later Gate ring electrode will be isolated to the CNT. The last step for finalizing the nano sized confinement is the etching of the SiN bottom layer in order to get access to the Poly-Si Source plate. Then the catalyst is deposited by electroplating inside the hole acting as a nucleation side for the CNT growth. The nano hole approach is illustrated in figure 1 showing a comparison between the principle technology scheme and a real nano hole demonstrated by the SEM cross section. By using this technology approach nano

holes below 20 nm could be realized with the potential for further down scale.

The correlation between the layout of a single vertical transistor, the principal technology scheme and a grown CNT within a nano hole is shown in figure 2. The transistor layout is composed of a 3-terminal structure with single Source, Gate and Drain contacts. For the realisation of the nano transistor four lithography levels are needed (Source Plate, Nano Hole, Contact, Metal). The ring shaped Gate electrode within the single nano hole is placed within the center of the transistor structure and connected by a Poly-Si interconnect with the Gate pad. On the SEM picture a Carbon Nano Tube can be seen grown out of the nano hole confinement which is demonstrating the technological feasibility. The grows of the CNT structures was carried out by the partners CNRS and University of Cambridge. Next to applications of the nano hole approach as a confinement for semiconducting nano channels further utilisations are possible in different technological fields e.g. Bio and Medical purposes.

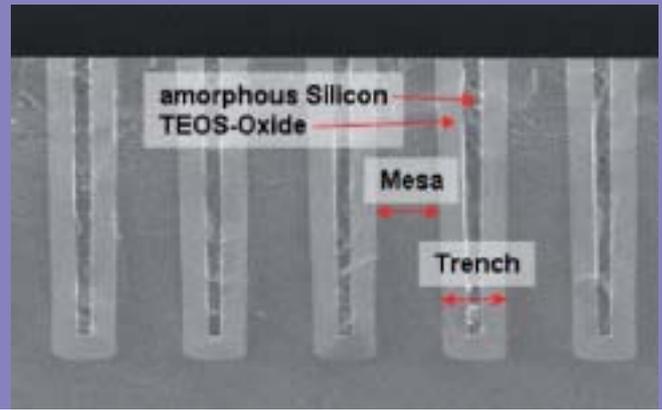
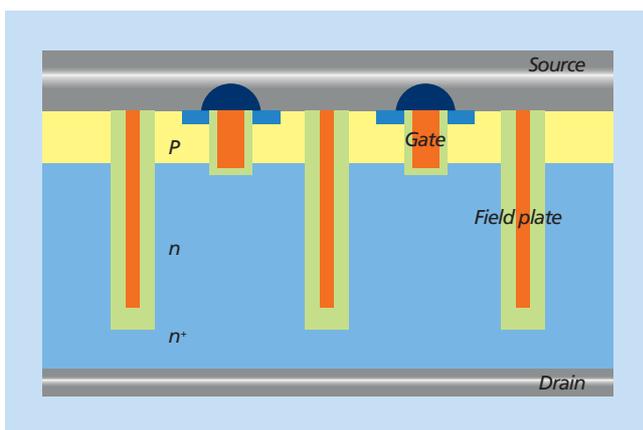


Figure 2: SEM cross section of a trench based compensation structure.

## DEVELOPMENT OF NEW ENERGY EFFICIENT SEMICONDUCTOR POWER DEVICES

Fraunhofer ISIT is investigating new high voltage compensation PowerMOS devices with improved energy efficiency. For PowerMOS transistors the reduction of the On-state resistance  $R_{DSon}$  is the most important R&D topic for minimizing the conduction losses. The value of  $R_{DSon}$  depends on the maximum blocking voltage  $V_{BR}$  of the transistor and is increasing according to a  $V_{BR}^{2.5}$  dependency. The main contribution to  $R_{DSon}$  is the serial resistance of the transistor driftzone  $R_{DZ}$  which is defining the so called Si-limit. The most striking feature of all compensation devices is its capability to overcome this Si limit being imposed on conventional devices. The transistor architecture ISIT is investigating is based on deep Si trenches being used as compensation structures for field plate or pn-junction type of compensation. The principle of a field plate device is depicted in figure 1. The deep compensation structure showing an isolation layer along the deep trench edges with a conductive field plate being embedded. The

Figure 1: Principle schematic of a trench based PowerMOS device with field plate compensation structures.

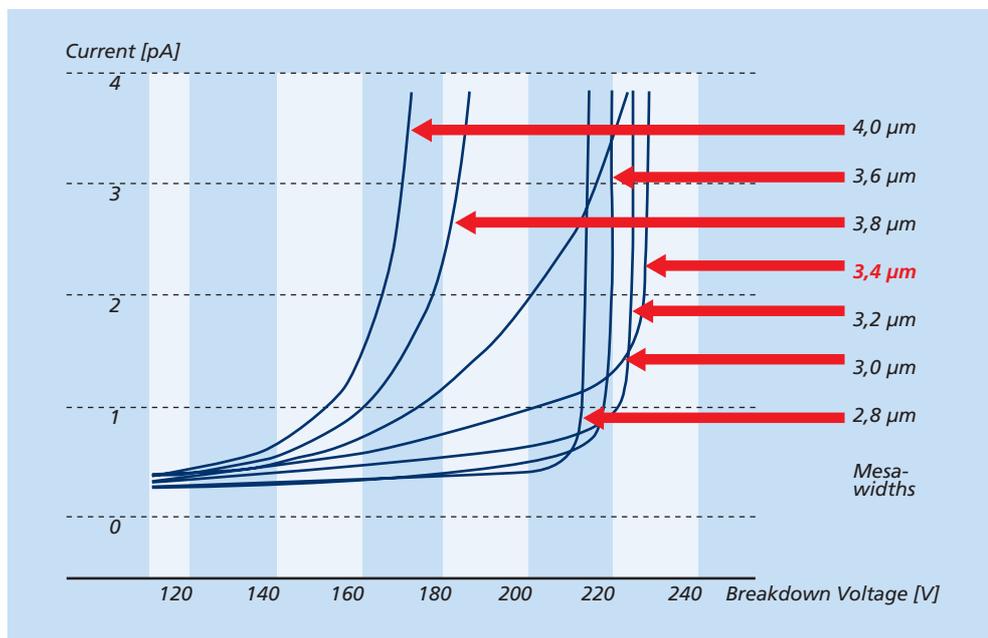


PowerMOS transistor cell is located in between the compensation trenches. In the Off-state of the PowerMOS device the vertical field plates allowing 2-dimensional depletion of the drift zone even at higher doping concentrations. This increased doping concentration of the drift zone by e.g. a factor of 10 compared to standard devices is the reason for the reduction of  $R_{DSon}$  in the On-state of the compensation device.

The technological realization of the field plate based compensation structure is illustrated in figure 2. A new developed deep trench etching process with a special trench profile for void free trench filling was implemented. Chemical Mechanical Polishing (CMP) was used for the planarization of the trenches which is prerequisite for further PowerMOS processing. Special doping profiles are required to ensure a complete depletion over the entire drift zone region in between the compensation trenches. The distance of the deep trenches (mesa width) has to be correlated with the doping concentration to allow for a perfect charge compensation for the nominal breakdown voltage.

Fraunhofer ISIT has fabricated high voltage diodes with the novel trench field plate concept in order to demonstrate the charge compensation effect. The proposed structure has been simulated by use of a commercial process and device simulator (ATHENA and ATLAS) and the findings are compared with measurement results. As shown in figure 3 I-V blocking characteristics have been simulated for varying distances of compensation structures (mesa widths) between 2,8  $\mu\text{m}$  and 4,0  $\mu\text{m}$ . Under the condition of having used optimized technological parameters it was the goal to define the best mesa width for charge compensation at 200 V breakdown voltage. It was found out that complete charge compensation is ensured at a mesa width of 3,4  $\mu\text{m}$  which is resulting in the highest breakdown voltage of 230 V.

Figure 3: Simulation results of reverse biased I-V characteristics calculated for different mesa widths.



A comparison between simulation and measurement results is depicted in figure 4 showing the dependence of the normalized breakdown voltages on the mesa widths. The measured breakdown voltages exhibit an optimum at a mesa width of  $d = 3,4 \mu\text{m}$  which is well correlated to the simulation results. However, a difference in the maximum breakdown voltage of about 20% can be observed. This effect is supposed to be due to non optimal charge compensation within the device area. By geometrical reasons the edge area of the chip is preferential for over compensation effects (3D-effect). This 3D effect could not be considered in the 2D simulation. Based on those results layout modifications of a new chip design have been taken into account.

The R&D work was carried out within the BMBF (Federal Ministry of Education and Research) project "Energie-effiziente Leistungsbaulemente für den Spannungsbereich bis 400 V".

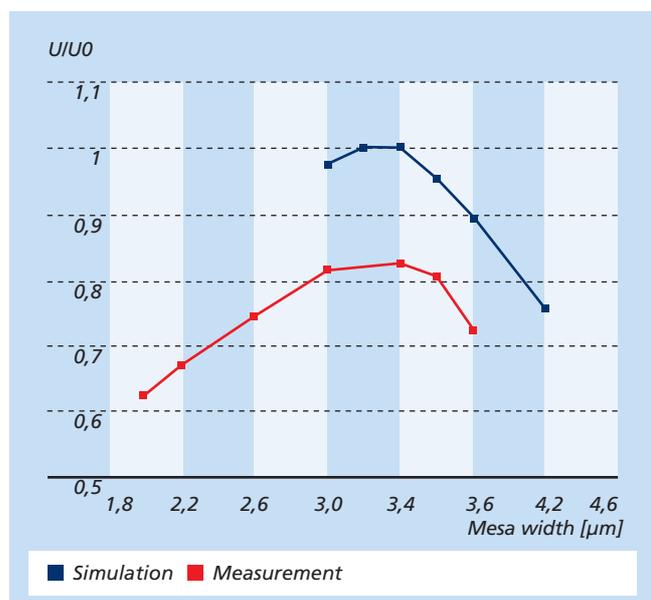


Figure 4: Normalized breakdown voltage versus mesa width: Comparison of simulation and measurement results.

### CHEMICAL-MECHANICAL POLISHING FOR THE FABRICATION OF FIELD PLATES FOR SUPER POWERMOS DEVICES

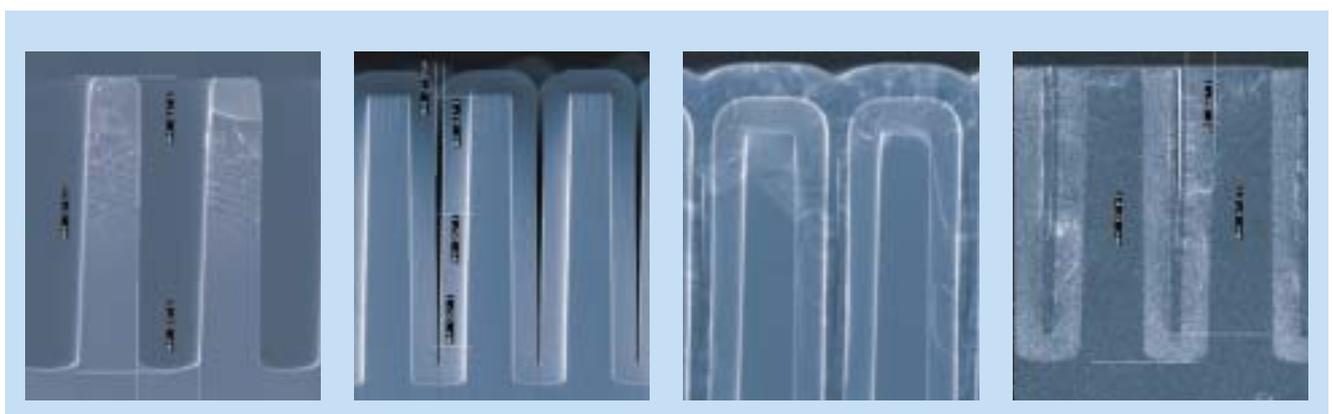
Planarization by means of chemical-mechanical polishing (CMP) plays a key role in the manufacturing of today's advanced micro- and nanoelectronic devices like  $\mu$ -processors, ASICs and memory chips. CMP processes are available for a wide variety of materials like silicon oxide, silicon nitride, poly-Si or various metals (Cu, W, Ni, etc.). It is common for all processes that, according to Moore's Law, structures with ever decreasing linewidth and film thickness have to be polished with extremely high precision.

Since several years CMP processes are also employed for the manufacturing of micro-electro mechanical systems (MEMS) and devices with additional non-digital functionalities like e.g. powerMOS devices („More Than Moore“). The differences to „main-stream CMP“ are larger structures, thicker layers, other layer materials, and very specific planarization requirements depending on application. Other distinguishing features are smaller substrate sizes and materials and, as of today, reduced production volumes, which all lead to specific consequences for the successful execution of the CMP processes.

By using the example of the fabrication of field plates for novel Super PowerMOS transistors, occurring challenges and problems during the development of appropriate CMP processes will be discussed. As described in detail in the report (page 54, "Development of New Energy Efficient Semiconductor Power Devices"), the manufacturing flow of the field plates consists of etching 15  $\mu\text{m}$  deep and 3.5  $\mu\text{m}$  wide trenches, followed by the deposition of 1.5  $\mu\text{m}$  TEOS oxide and 0.5  $\mu\text{m}$  of amorphous (a-) silicon, see figures 1 a-c. In order to get the inlayed field plates, overburdening a-Si and TEOS have to be removed by CMP.

This task is similar to the damascene scheme, which has been developed for manufacturing of inlaid copper conductive lines for multi-layer interconnects. Instead of the removal of copper over trenches in the dielectric, here the two materials a-Si and

Figure 1: Field plate trenches. a) after etching, b) after TEOS deposition, c) after a-Si deposition, d) after silicon and oxide CMP



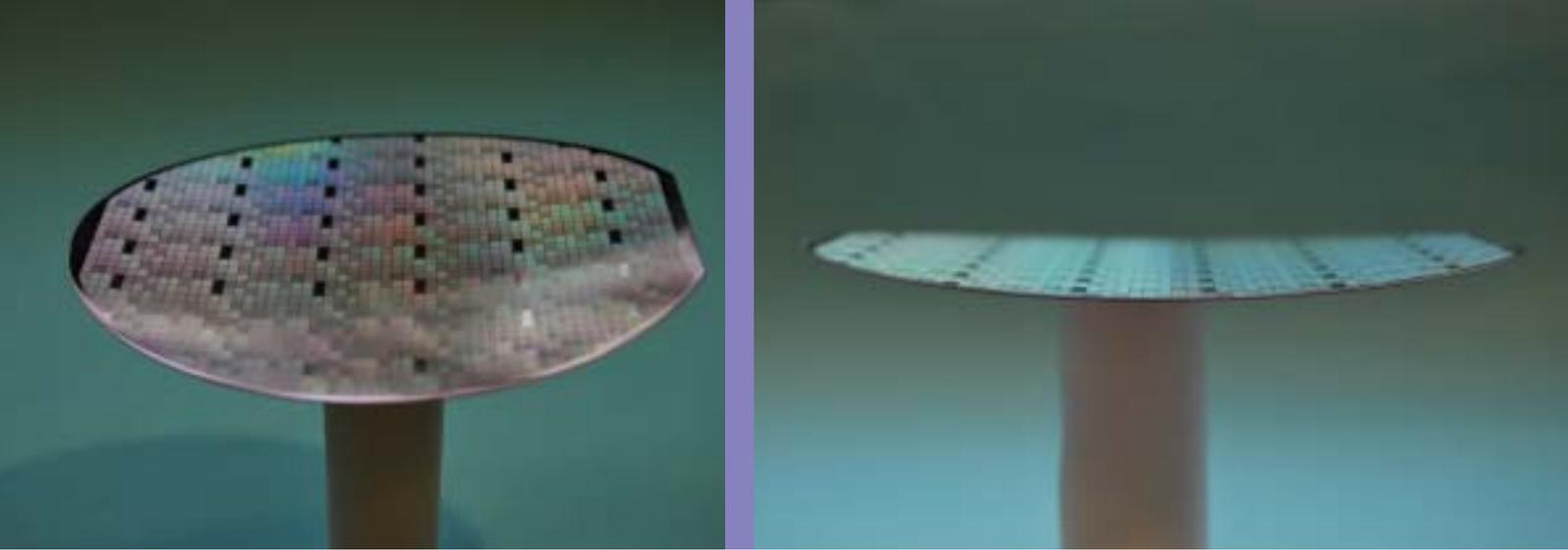


Figure 2 a,b: Warped wafers due to trench geometry and stress of the deposited layers show a bow of several mm.

TEOS have to be polished. A stopping layer as in the case of Cu-CMP does not exist, the polishing process has to be terminated when the substrate is touched. As the exposed silicon substrate is used as active area for the following built-up of vertical trench powerMOS transistors, the exposed silicon has to fulfil highest surface quality requirements like smoothness and cleanliness comparable to silicon prime wafers.

There are two possible approaches to achieve the goal, which have various pros and cons. One approach is the use of two highly selective slurries, the first one for a-Si (selective to TEOS) and the second one for TEOS (selective to silicon). The good silicon surface quality is finally achieved by using a short haze-free polishing step as used for prime wafer fabrication. The advantage of that approach is a stopping of the polishing and a negligible substrate loss. The disadvantage is the formation of a small a-Si topography due to the near-zero silicon removal rate of the second slurry and a slight dishing into the TEOS liner which occurs during overpolish.

The second approach is to use a slurry with nearly identical removal rates for a-Si and TEOS. This process must be performed time-controlled, as no stopping occurs on the mono-Si substrate. The smooth Si surface can again be obtained by the haze-free polishing step. The advantage of that approach is a very high degree of planarity, while, on the other side, there will be some silicon loss during overpolish, which has to be kept under control.

Due to the fact that an oxide slurry with high selectivity to silicon is still under evaluation and not readily available, we have concentrated our development work on the use of the non-selective slurry. In test runs on blanket layers we have determined the a-Si removal rate to 500 nm/min and the TEOS removal rate to 350 nm/min, which can be viewed as equal for this application. The optimized process showed removal non-uniformity values of less than 5.0 % for both a-Si and TEOS, although 2 µm of material has to be polished. The slurry used was the long-year „work horse“ SS25 from Cabot microelectronics, a fumed-silica based slurry originally developed for oxide CMP. As some wafers showed a very pronounced bow and warp due to the trench geometry and the thick deposited layers, a higher than usual downforce had to be applied to press the wafer flat against the polishing pad. A positive side-effect of this procedure were the nearly-equal removal rates, as it has been observed that larger downforce leads to faster increasing oxide rate, while the silicon removal rate increased more slowly. A cross-sectional view of the polished field plates is shown in figure 1d. A very planar surface without any dishing can be observed.

Warped wafers before stress optimization, which showed a bow of several millimeters parallel to the wafer flat direction, are depicted in figures 2a-b. As already mentioned, wafers warped to such an extent represent a particular challenge to achieve a sufficient removal homogeneity. As the 1:1 selectivity approach leads to uncontrolled silicon removal connected with an uncontrolled loss in trench depth, it is planned for the future to employ selective slurries. For a highly selective silicon slurry industrial products are available and already under evaluation, while a highly selective oxide slurry is still under development and needs more tests before introduction in the process flow.

# BIOTECHNICAL MICROSYSTEMS

## THE FRAUNHOFER IN-VITRO-DIAGNOSTIC-PLATFORM

Today many diagnostic tests are done in central medical laboratories. Therefore samples are collected from patients and are sent to these labs for automated measurements. Because of this many patients have to wait for days to get their results even in urgent cases. To shorten this lack of time, the point-of-care-diagnostic directly at the doctor is of high interest. The used measurement devices have to fulfil some characteristic features: They have to be small, inexpensive, fast and reproducible. The Fraunhofer in-vitro-Diagnostic-(ivD)-Platform highlights these features as a result of the combined knowledge of nine Fraunhofer institutes: Fraunhofer IBMT (coordinator), IPA, IFAM, IZM, ENAS, IAP, IPM, IGB and ISIT. The whole project was founded by the Fraunhofer Society as a so called MAVO (Market-driven pre-research).

The ivD-platform consists of a detection device and single use plastic detection cartridges built in a modular way. It should be able to detect DNA as well as proteins. In the detection device the whole electronic parts and in the case of fluorescence detection the optical parts were integrated. The cartridges consists of the complete fluidic parts like reagent reservoirs, gel based electrochemical micropumps, channels and the biochips. The project aims to be problem orientated instead of technology driven. Therefore different detection technologies were inserted - the optical TIRF (Total Internal Reflection Fluorescence) technology from IPM and the electrical biochip technology from ISIT. According to the application it could be chosen between them. To reduce costs in fabrication the introduction of mass production like injection moulding of

Figure 1a: Picture of the array chip with 16 positions.  
Figure 1b: Spot layout for CRP/PSA measurement.

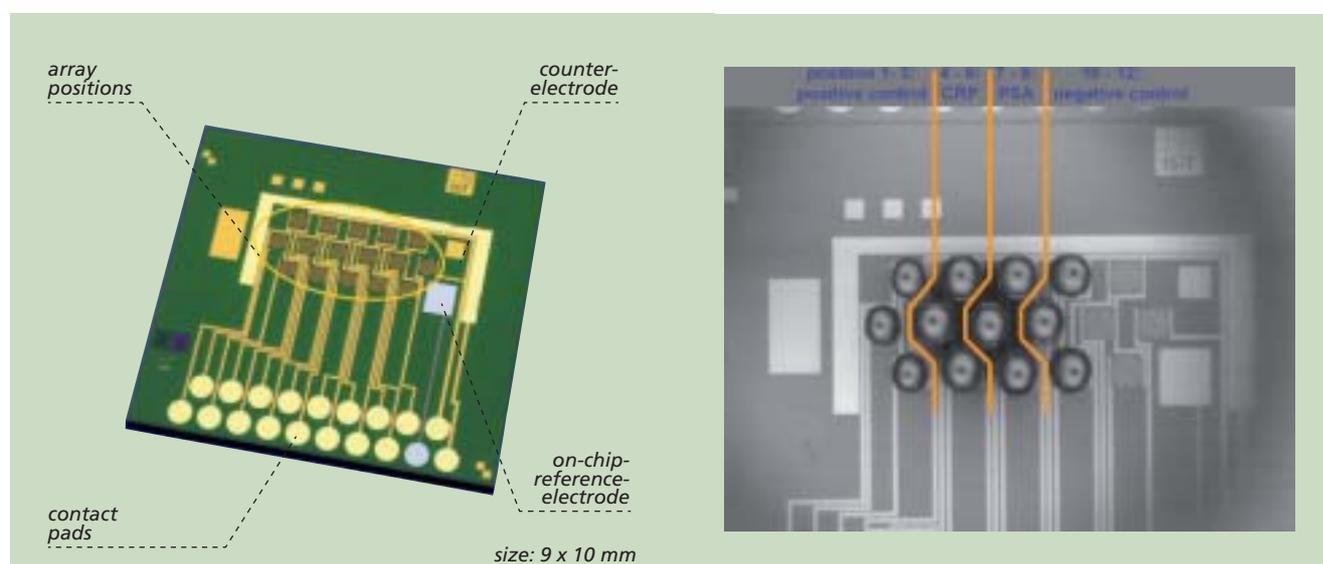




Figure 2a: ivD-cartridge equipped with reservoirs, fluidic parts and chip. Figure 2b: ivD-Measurement device.

plastic parts started from the beginning and in parallel to the research work. Responsible for the construction of the devices was IPM. The cartridges were developed by ENAS, IZM and IPA. The detection of the marker molecules CRP (C-Reactive Protein) and PSA (Prostate Specific Antigen) were used as a model system. These measurements were done in parallel at IBMT, IPM and ISIT with the different detection technologies.

At ISIT these ELISA-like assays (Enzyme-linked immunosorbent assay) were evaluated with a common used electrical biochip array with 16 positions (see figure 1a). The anti-CRP- and PSA-antibodies were spotted by an automated microdispensing device onto 3 chip positions each. They immobilized via thiol links and adsorptive forces to the gold electrodes. Another 3 positions were covered with a mouse IgG antibody for positive control and another 3 positions were covered with a nonbinding protein (BSA) for negative control (see figure 1b). The spotted chips were housed in a so called ChipStick. The assay procedure including the electrochemical detection of an enzyme generated redox active product was done with an "eMicroLISA" device (AJ eBiochip GmbH). The sample was automatically pumped over the chip and during incubation CRP and PSA molecules bound to the immobilized antibodies. Added mouse-Anti-CRP- and mouse-Anti-PSA antibodies acted as detector antibodies. An Anti-mouse-enzyme conjugate acted as a label. It bound to the positive control positions and to detector antibodies at the CRP/PSA positions. The BSA positions left unbound. After this labelling step a substrate was added. This substrate was converted by the label enzyme into its redox active form and could be measured specifically for each position in a stopped flow modus. The resulting current slopes were directly proportional to the CRP and PSA amounts in the sample. This assay procedure including the reagents and the electrical biochip was transferred into the ivD-platform cartridge (see figure 2a) which was controlled by the ivD-measurement device (see figure 2b).

The comparison of an assay with the same CRP and PSA concentrations performed with the "eMicroLISA" on one side and with the ivD-cartridge on the other side showed in general lower signals in the cartridge. This depends on adsorption effects of reagents in the injection moulded and single used fluidic cartridge parts. After standardisation the results are similar to the assay performed with the "eMicroLISA".

The positive and negative control positions were used for an internal calibration. The standard deviation from assay to assay was about 10 % after standardisation. The test sensitivities of 1 ng/ml for CRP and 2 ng/ml for PSA were in the range of the diagnostic demand. The whole assay time is 24 minutes. The results of this project will be improved in a further project called ivD-WISA.

# MODULE INTEGRATION

## EMBEDDING OF ACTIVE DEVICES IN ORGANIC SUBSTRATES

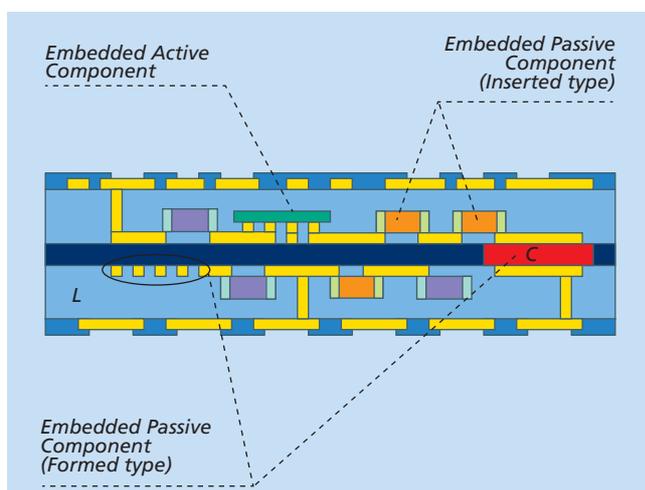
In the past years several techniques have been developed to integrate passive or active components into organic substrates, i.e. printed circuit boards (see figure 1). With this technique the integration density can be increased, thus the weight and geometry of circuit boards can be reduced. Due to reduced circuit paths the signal integrity can be increased for high frequency applications. Therefore it is possible to reduce the signal amplitude to reduce the power consumption or to increase the operation frequency. The incorporation of formed passive components can be used to simplify the assembly process, resulting in distinct cost savings. Whereas embedded active components may give additional functionality, like the identification of circuit boards with RFID chips (radio frequency identification). Even complex functionalities like brand pro-

tection can be realized with invisibly hidden application specific integrated circuits (ASICs). In the latter case it may be necessary to connect a large number of electrical pads with a usually quite dense contact scheme. Due to the embedding of the component pretested bare silicon dies have to be used. Furthermore it is mandatory to use thinned dies with a thickness in the range of 50  $\mu\text{m}$  to 200  $\mu\text{m}$ . Obviously the connection technique should be quite thin, space saving, and robust. Traditional techniques like wire bonding and solder flip chip can not fulfil these requirements. If high electrical conductivity is required, all kind of gluing techniques will not get us very far.

In case of RFID chips isotropic conductive adhesive may be a cheap and simple solution. Whereas anisotropic conductive adhesive gluing or even nonconductive adhesive gluing are feasible if the electrical resistance of the contact is not very important. However, really small electrical resistances can only be achieved with a pure metallic connection, which can be realized by traditional flip chip soldering, anisotropic conductive adhesive (ACA) filled with solder particles (ESC5), intermetal diffusion or ultrasonic bonding. Each of these techniques has its own advantages and disadvantages (see table 1).

Since many ASICs may be available only for wire bond interconnection, a special contact pad modification for flip chip assembly is required. Fraunhofer ISIT selected gold stud bumping as a preferred process which can be applied to wafers as well as single chips. As the stud bump pattern can be changed easily, this contact modification is particularly useful for high variety applications while electroplated bumps are favourable in high volume applications. Additional requests are the avoiding of additional substrate costs by noble metal plating and difficult registration methods that may affect the process yield. Based on these considerations Fraunhofer ISIT sees many benefits in the use of anisotropic

Figure 1: Classification of Embedded Components: Passive components are formed by added materials or placed as SMD component. Active components are always placed.



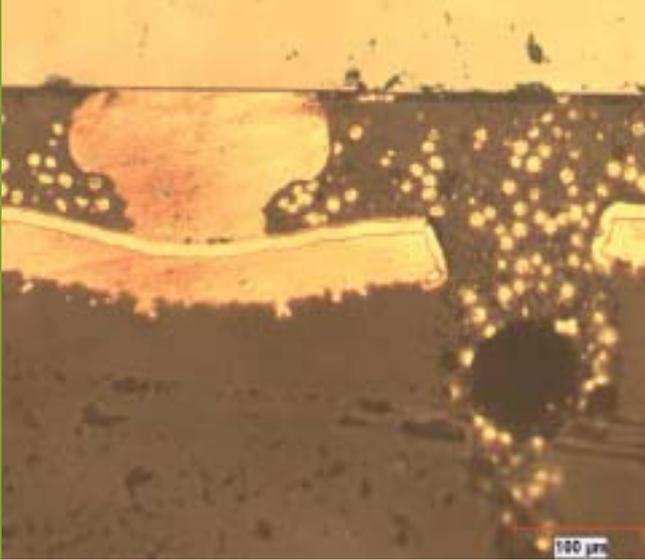


Figure 2: Cross Section of an Embedded Active Component joined with the ESC5 Process.

conductive adhesive (ACA) filled with solder particles. This material has been introduced as ESC5 process by Namics and Panasonic Factory Solutions. This joining technique is quite similar to the usage of conventional anisotropic conductive adhesive, but no metal surface refinement with noble metals is required. Furthermore the electrical conductivity of the joint is comparable to conventional solder joints and the flip chip is

contacted and underfilled at the same time without the need of a solder stop mask. Figure 2 shows a cross section of an active component embedded in an organic substrate based on these techniques. Lamination and accelerated reliability tests have been performed and proved the robustness of this active chip embedding technique with 200 μm thin chips in large substrate panels.

Table 1: Comparison of different flip chip joining techniques

	Solder flip chip	ACA with solder particles (ESC5 process)	Intermetallic diffusion	Ultrasonic bonding	Isotropic gluing	Anisotropic gluing	Nonconductive gluing
Lead free	●	●	●	●	●	●	●
Flux less	●	●	●	●	●	●	●
Low contact resistance	●	●	●	●	●	●	●
Compatible with Au Stud Bumping	●	●	●	●	●	●	●
No surface refinement required	●	●	●	●	●	●	●
No solder resist required	●	●	●	●	●	●	●
Large choice of materials	●	●	●	●	●	●	●
Compatible with preapplied underfill	●	●	●	●	●	●	●
Yield	●	●	●	●	●	●	●
High mechanical rigidity	●	●	●	●	●	●	●
High reliability	●	?	?	●	●	●	●
Long shell live	●	●	●	●	●	●	●
Costs	●	●	●	●	●	●	●

● good   ● fair   ● bad

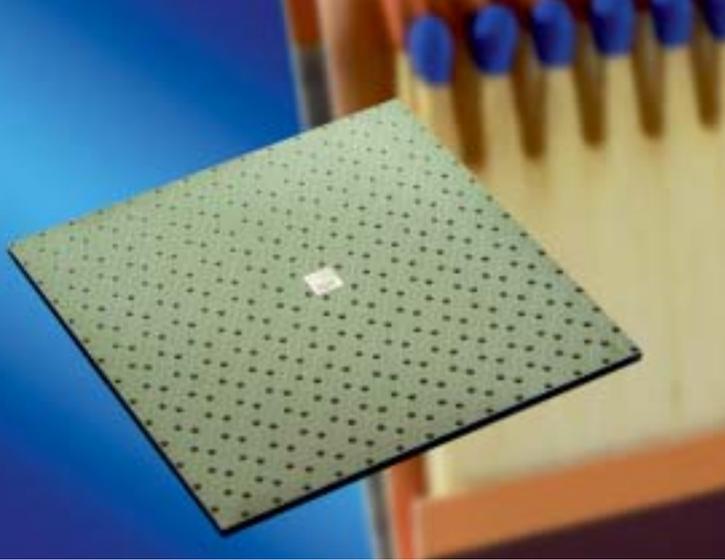


Figure 2: Test chips (see figure 1) in a matrix arrangement to verify different parameters for the Silver epoxy dispensing.



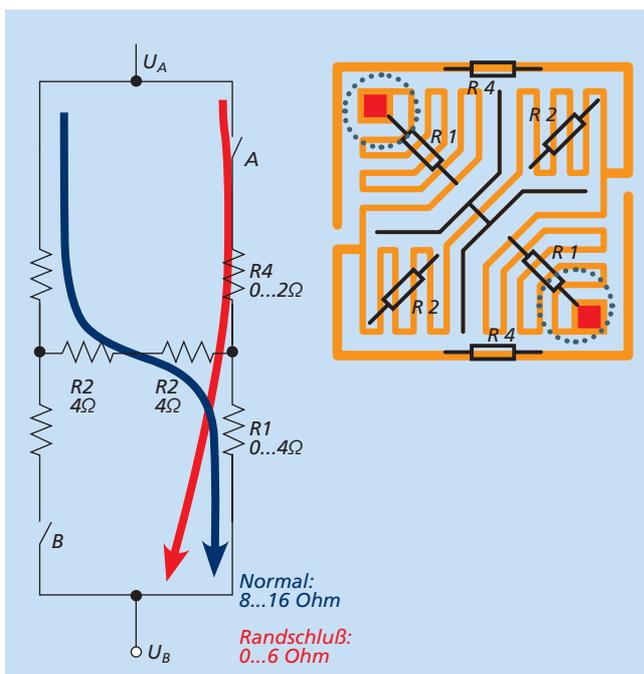
Figure 3: A 13,56 MHz antenna coil, screen printed on paper as a substrate. The pads connect it to a chip module (figure 4).

### WORLDWIDE AND UNIQUE - RFID-LABELS MEET ARTS

Artworks and smart labels have two things in common: They both have something unique, and they travel worldwide. It is not always easy to say what makes an artwork unique, and we will not attempt here to do so. The unique part of a smart label, however, is simply an unchangeable code number in a tiny piece of silicon that allows it to be identified among billions of others, produced each year for applications like access control, inventory management or logistics.

RFID - „Radio-Frequency Identification“ - chips are hardly noticeable: On roughly 1 mm<sup>2</sup> area, they integrate radio transmitter circuits, processor functions and memory space

for user purposes. With a thickness of 150 µm or less, it is possible to embed them in a piece of paper. To form a flexible transponder system, a „smart label“, it is however necessary to connect an antenna to the chip. In the project PESEL, funded by the German Ministry for Education and Research, a consortium of eight companies studied the complete value chain from interconnect technology to a selected logistic application to find optimization potential. In a final field evaluation, more than 2000 smart labels helped to keep track when the 20th century art collection of the „Kunstsammlung Nordrhein-Westfalen“ was moved into three different storage locations. According to the transport company, their customers expect a real added value from using electronic tags to manage their inventory, in particular objects that are frequently moved between exhibitions on an international scale. Finding cost optimization potential in RFID means to look at the whole logistic process: While cost reduction in smart label manufacturing is essentially limited by the semiconductor chip, there is still some potential in the infrastructure used: A new generation of robust RFIDscanners, using globally available wireless communication services, was developed and customized to achieve a time reduction in labeling, scanning and indexing objects. The devices feature fast access to the required elements in each logistic process step.



Figures 1a, 1b: Design of a test chip for assembly process study with isotropically conductive adhesive. Switches „A“ and „B“ represent short circuits of adhesive to the chip edge.

ISIT supported the project as coordinator, provided analytical services and performed studies on assembly technologies in smart labels, for example connecting the tiny chips with antennas printed on paper as a substrate. The common interconnect techniques are the following:

- Soldering: Requires high temperature, in particular if leadfree solders are used, and is therefore limited to relatively expensive electronic substrate material. We supported metallurgical studies on SnBi solder paste with a lower working temperature than SnAgCu alloys.



Figure 4: Paper can even be used to fabricate low cost chip modules. The insets show how material selection (underfill, silver epoxy) affects the result.

- NCA or ACA: Non-conductive or anisotropically conductive adhesives use their pronounced shrinking properties to establish a permanent, force-based electrical contact between surfaces. This approach is common in smart labels, but requires high contact bumps on the chip and a good surface quality of the substrate pads. We prepared cross sections of chip pads on PET substrate contacts formed by electroplating.
- ICA: Isotropically conducting adhesive is not frequently used for RFID chips - the dispensing process becomes dif-

ficult if dimensions are small. A defined volume of ICA has to be placed precisely to avoid short circuits or wetting the chip sidewalls. However, this technique does not principally require high chip bumps and is suitable for rough, porous surfaces like screen-printed conductors.

To allow process adjustment with ICA material on a significant number of samples, a test chip (figure 1) was designed and manufactured: On its surface, meander-like resistors around the pads can tell whether the process stability is constant or runs into critical parameter deviation.

Figure 5: A final look, and chief conservator Werner Müller closes the transport box of a precious sculpture. RFID scanners link objects to boxes.



Figure 6: For the transport of the „K20“ collection, more than 2000 smart labels (inset) have been used on packing systems and artworks.

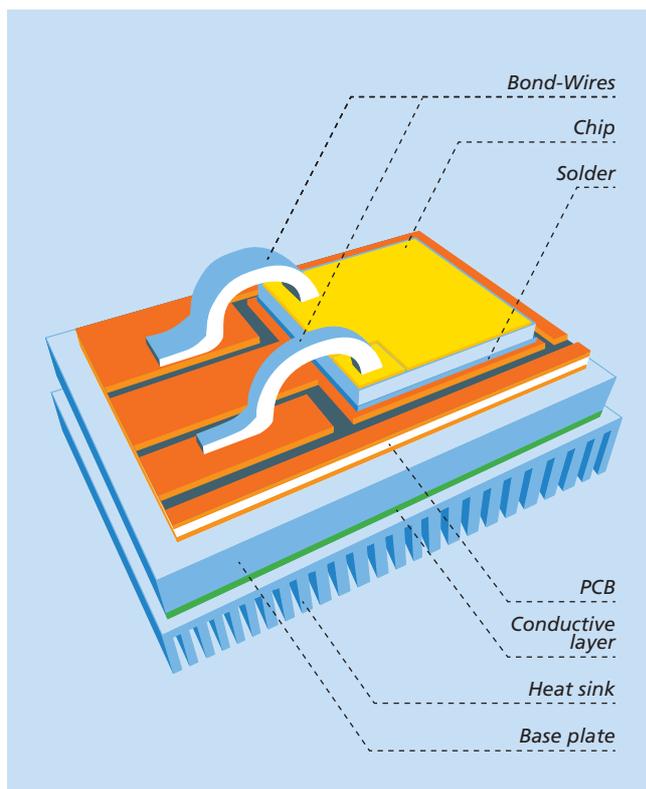


**ANALYSIS OF LARGE AREA SOLDER JOINTS FOR RESIDUAL VOIDS**

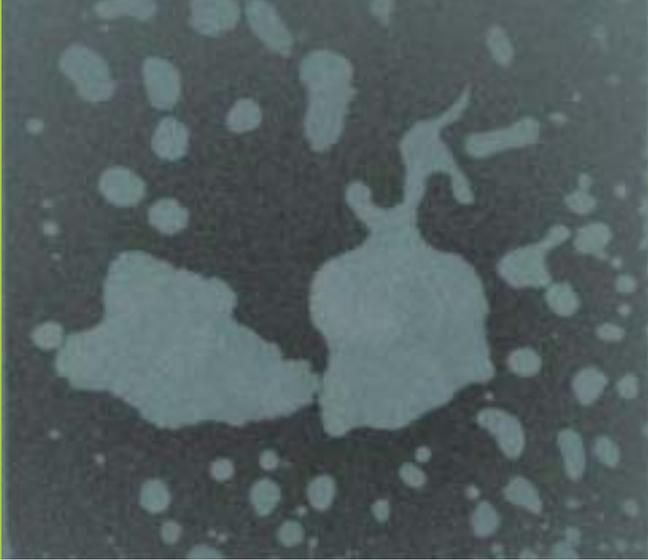
Nowadays, the raising current density in power electronics discloses a basic problem. The power semiconductor generates a lot of heat at high currents. Unfortunately, the heat leads to stress in the conductive layers, because of different coefficients of thermal expansion. This tends to result in defects and finally, it ends in a malfunction. Especially in the automotive industry, this is a serious problem, since the ambient temperature is often higher (engine, drive shaft) than for other applications, and power electronic takes part of many safety-related systems.

The most widely used assembly concept of power modules is shown in figure 1. On a heat sink, a heat-conductive layer warrants the thermal contact with a ground plate. The plate may be any thermally conductive material, normally it is Aluminium. With solder, adhesive or other joining, a substrate is fixed. This can be a Copper coated layer of ceramics (DCB - Direct Copper Bonded, figure 2), a normal printed circuit board (PCB - Printed Circuit Board) or a similar substrate. These allocate also the connections for the supply and control lines. The semiconductor chip (MOSFET, IGBT, etc.) is mounted on this layer by a suitable packaging method, and the top is connected with thin Aluminium or Gold wires (bond-wires) to the source and the gate contact. For the electrical insulation the module is usually filled with a flexible mass, which covers the bond wires and the top of the module. In the case of active cooling and in the typical thermal stack, for the heat exists only one way. Nearly all of the heat has to pass through all layers down to the heat sink. This means a significant disadvantage, because each layer exhibits an own heat conductance value and an own expansion coefficient. From the viewpoint of the thermodynamics such a structure is also known as thermal stack.

Figure 1: Typical thermal stack.



The robustness of a system is, inter alia, dependent on resistance to cycling tests. That means how long a module can resist the forces during temperature cycling around a fixed  $\Delta T$ , excited by a defined current flow. We can determine two main weak spots. On the one hand the wire connection on the top of the chip, on the other hand the solder joint between the semiconductor chip and the substrate. That is the point where the major component of the heat flows through. For this connecting layer is the sintering technique an alternative. In the sintering process, a Silver powder will be sintered under high pressure and at temperatures between 120 °C and 260 °C to a solid layer. This method is not widespread today,



Figures 3a+b: Void generation, at the left without and on the right with a vacuum based soldering process

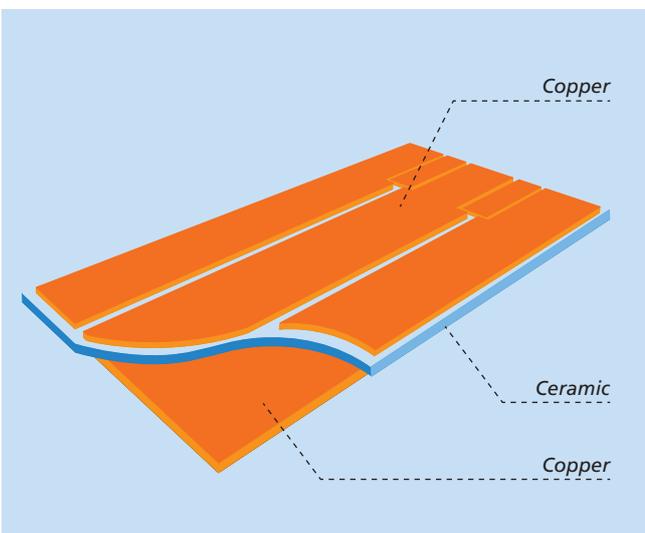


Figure 2:  
Direct copper bonded (DCB)

so most structures use solder joints at this point. The thermal conductivity, and the durability of a solder joint depends on the volume of the solder joint, the used solder and the voids of the connection. Voids in soldered connections occur in the phase of liquidus during the soldering process. Remaining flux or other residual substances from the solder paste expand through the heat of soldering and form bubbles in the liquid solder which either go to the surface of the solder or forms voids during cooling.

The influence of voids in solder joints on the time life was already investigated in the AIF-project „volume effects“ at Fraunhofer ISIT. It was simulated that a void within a solder joint between power semiconductor and substrate leads to an increase of the temperature difference between these components, and thus to an increase in the mechanical stress between chip and substrate leads. In consequence of the increased stress resulting from the temperature difference, the lifetime of the solder joint is significantly reduced.

To take a closer look at the formation of voids, large area solder joints were generated in situ in an X-ray chamber, and the void generation was recorded. The video received during the void formation were evaluated according to time intervals. First results confirm the presumption that the solder pastes behave very differently. Flux or other additives facilitate henceforth void formation significantly. Furthermore, large-area solder joints under vacuum conditions were created and compared with conventional solder joints (see figure 3).

The soldering method in the atmosphere and in vacuum show significant differences. The soldering in vacuum allows solder joints with significantly fewer voids than under atmospheric conditions. The temperature resistance in the connection under vacuum is much lower, the heat load of the material, therefore, smaller. A much longer lifetime of the connection can be expected.

# INTEGRATED POWER SYSTEMS

*Lithium polymer batteries in  
different shapes.*



## NEW ELECTROLYTES FOR IMPROVED SAFETY AND TEMPERATURE PERFORMANCE OF RECHARGEABLE LITHIUM BATTERIES

Lithium ion batteries (LIB) are nowadays used in most electronic devices in the consumer market such as camcorders, laptops and mobile phones. But more and more also bigger batteries for hybrid/electric vehicles or industrial applications are demanded. Here the typical temperature operation range of LIB's of -10°C – 60°C is not sufficient. New approaches to widen this range are needed.

Graphitic carbons are still the first choice material as negative electrode in lithium ion batteries, for the reasons of energy density and cost. But during the last years more and more also its drawbacks are considered. In particular the danger of lithium plating and the flammability of graphite leads to a reduced intrinsic safety that can cause higher risks if such accumulators are used in automobiles or medical devices. Moreover this battery type usually shows lower cycle stability and durability as well as a significant self discharge.

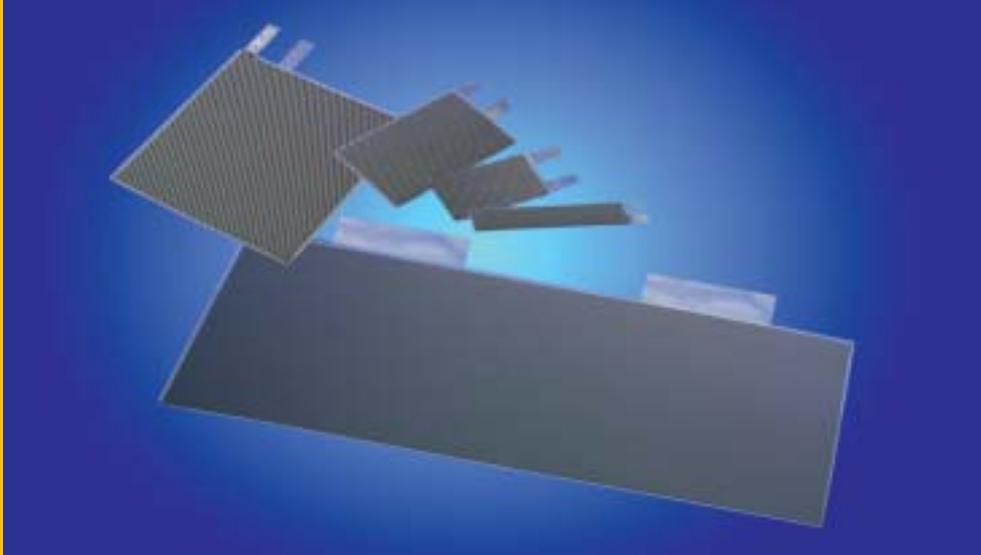
Additionally this anode material is stable only in a limited number of electrolyte compositions due to the formation of a stable solid electrolyte interface (SEI) on the graphite particles.

Such electrolytes are primarily responsible for the limited temperature range of LIB's. Ethylene carbonate (EC), that is essential for the formation of the SEI on the graphite particles, is solid at room temperature. A viscosity reducing solvent like DMC with a low boiling point is therefore indispensable. Both, boiling and melting point are basically determining the temperature operation range of LIB's as indicated in table 1. Therefore alternative anode materials were investigated for new applications that may be used in combination with alternative electrolytes to improve safety as well as increasing the temperature operation range of LIB's.

One promising candidate is  $\text{Li}_4\text{Ti}_5\text{O}_{12}$  that holds several advantages. The material is inflammable and the high positive lithium intercalation potential prevents the deposition of

*Table 1: Comparison of a standard LIB electrolyte (LP30) and new electrolyte compositions investigated here for lithium titanate based systems.*

Type	Conducting Salt	Solvent Composition	Boiling Temp. (°C)	Melting Temp. (°C)
Standard LP30	Li PF <sub>6</sub>	Ethylene Carbonate (EC)	247 ... 249	<b>35 ... 39</b>
		Dimethyl Carbonate (DMC)	<b>90</b>	0,5 ... 4,7
	Li PF <sub>6</sub>	Gamma-Butyro-lactone (GBL)	204 ... 206	- 44
	Li BF <sub>4</sub>	Gamma-Butyro-lactone (GBL)	204 ... 206	- 44
	Li BF <sub>4</sub>	Gamma-Butyro-lactone (GBL)	204 ... 206	- 44
		Vinylene Carbonate (VC)	204 ... 206	- 44



Variety of battery cell designs for different applications.

metallic lithium on the electrode surface. From the same reason reductive electrolyte decomposition is drastically reduced, improving the cycle stability and durability of the battery. The application of new electrolytes can be considered, that are usually not stable in combination with graphite based lithium-ion accumulators.

Several electrolyte compositions were investigated at the Fraunhofer ISIT with the objective of widening the operation temperature window of lithium batteries with  $\text{Li}_4\text{Ti}_5\text{O}_{12}$  anodes. One solvent for a new electrolyte is  $\gamma$ -Butyro-lactone

(GBL). It possesses a high boiling temperature of  $204^\circ\text{C}$ , a low melting point of  $-44^\circ\text{C}$  and good solubility of lithium salts. GBL has been known as solvent in lithium batteries for many years but unfortunately it was not possible so far to produce stable graphite based lithium accumulators due to the reductive electrolyte degradation that in this case does not form a stable solid electrolyte interface (SEI).

In our work we demonstrated that in combination with lithium titanate as anode material good cycle stability can be reached with that solvent in combination with  $\text{LiBF}_4$  as

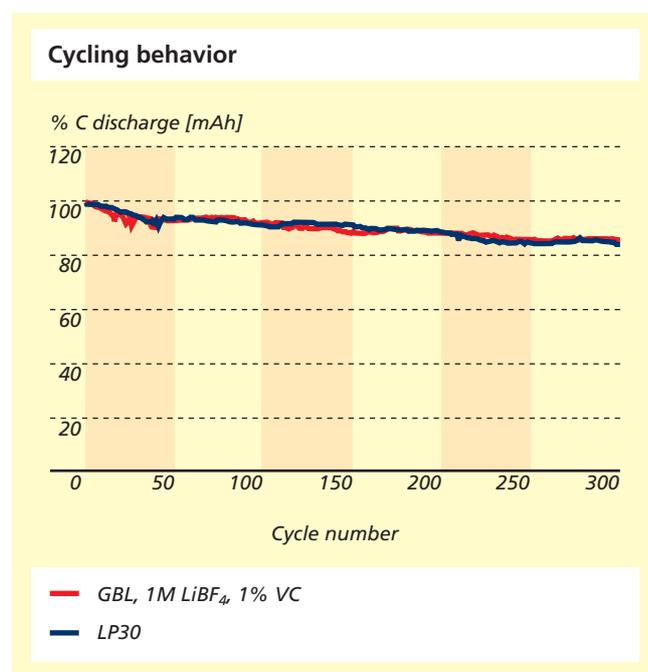


Figure 1: Typical result of an experiment showing the cycle stability of a lithium – polymer – accumulator with  $\text{Li}_4\text{Ti}_5\text{O}_{12}$  as active anode material. Two electrolyte systems GBL, 1M  $\text{LiBF}_4$  + 1% VC and ECI DMC 1:1, 1M  $\text{LiPF}_6$  (LP30) were compared.

lithium salt and Vinylene Carbonate (VC) as additive (see figure 1). It is also possible to charge and discharge batteries at temperatures of at least 80° C (see figure 2) without any gas evolution and below -30° C with still remarkable capacity (see figure 3). Therefore we see this material combination as a good candidate in e-mobility applications as a high operation temperature range is aspired there.

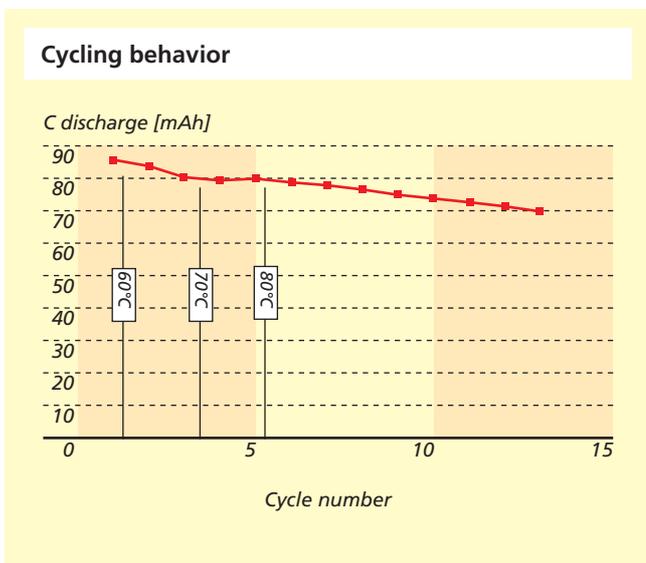


Figure 2: High temperature behavior of a test battery with GBL+ 1% VC, 1M LiBF<sub>4</sub> as electrolyte system. A higher fading can be observed at 80° C, but the battery is still working without any gas evolution.

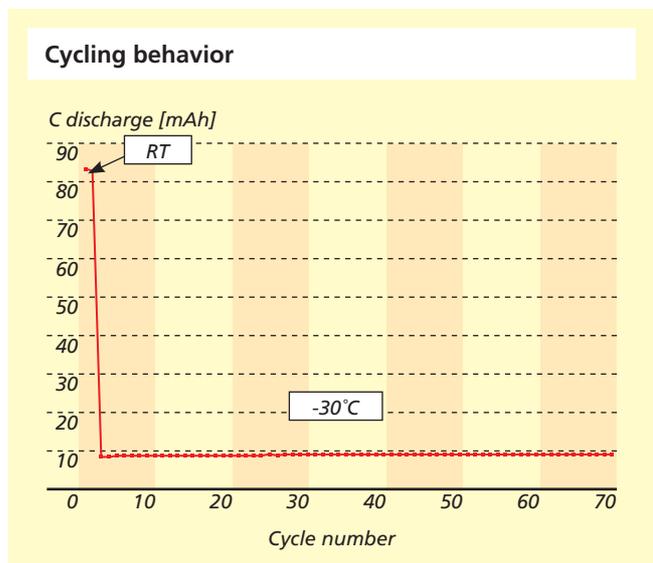


Figure 3: Low temperature behavior of a test battery with GBL + 1% VC, 1M LiBF<sub>4</sub> as electrolyte system. At -30° C 10 % of the initial charge at RT can be retained.



## **IMPORTANT NAMES, DATA, EVENTS**





ISIT Deputy Director Dr. Wolfgang Windbracke at pressconference „Neues Kompetenzzentrum Leistungselektronik in Schleswig-Holstein“. April 08.

**LECTURING ASSIGNMENTS AT UNIVERSITIES**

**R. Dudde**

Honorary Professor, Mikrotechnologie, Fachbereich Technik, FH Westküste, Heide

**O. Schwarzelbach**

Mikroelektromechanische Systeme (MEMS), Institut für elektrische Messtechnik und Mess-Signalverarbeitung, Technische Universität Graz, Austria

**B. Wagner**

Micro- and Nanosystem Technology I and II, Technische Fakultät der Christian-Albrechts-Universität, Kiel

**MEMBERSHIPS IN COORDINATION BOARDS AND COMMITTEES**

**T. Ahrens**

Member of AOI-Anwenderkreis (Automated Optical Inspection)

**T. Ahrens**

Member of DVS Fachausschuss Löten

**T. Ahrens**

Member of Hamburger Lötzirkel

**T. Ahrens**

Chairman of DVS AG V63 "Ausbildung Weichlöten in der Elektronikfertigung"

**J. Eichholz**

Member of MEMS and Sensor Systems, DATE '08 Conference

**J. Janes**

Member at MEMUNITY, The MEMS Test Community

**G. Neumann**

Member of Netzwerk „Elektrochemie“ der FhG

**G. Neumann**

Member of Netzwerk „Batterien“ of the Fraunhofer-Gesellschaft

**G. Neumann**

Member of Verbund Energie of the Fraunhofer-Gesellschaft

**K. Pape**

Member of BVS, Bonn

**K. Pape**

Member of FED

**M. H. Poech**

Member of „Arbeitskreis Bleifreie Verbindungstechnik in der Elektronik“

**M. H. Poech**

Mitarbeit im Arbeitskreis „Zuverlässigkeit, bleifreie Systeme“ des FhG IZM

**M. H. Poech**

Member of Arbeitskreis „Voids“ of Fraunhofer IZM

**M. H. Poech**

Member of „Voids“

**W. Reinert**

Member of Arbeitskreis A2.6, "Waferbonden", DVS

**W. Reinert**

Member of technical committee of Electronics Packaging Technology Conference, (EPTC)-Singapore

**W. Reinert**

Member of technical committee of conference Design, Test, Integration and Packaging of MEMSIMOEMS (DTIP)

**M. Reiter**

Member of Gf Korr "Arbeitskreis Korrosionsschutz in der Elektronik"

**M. Reiter**

Member of "Arbeitskreis Bleifreie Verbindungstechnik in der Elektronik"

**H. Schimanski**

Member of VDI Fachausschuss Assembly Test, VDI, Frankfurt

**H. Schimanski**

Member of ZVEI Ad-hoc Arbeitskreis Repair and Rework (R/R)

**B. Wagner**

Member of GMM-Fachausschusses 4.1 „Grundsatzfragen der Mikrosystemtechnik und Nanotechnologie“, VDE/VDI-Gesellschaft für Mikroelektronik, Mikro- und Feinwerktechnik

**A. Würsig**

Member of AGEF (Arbeitsgemeinschaft Elektrochemischer Forschungsinstitutionen e. V.)

**G. Zwicker**

Head of Fachgruppe Planarisierung / Fachausschuss Verfahren / Fachbereich Halbleitertechnologie und -fertigung der GMM des VDE/VDI

**G. Zwicker**

Member of International Executive Committee of International Conference on Planarization/ CMP Technology (ICPT)



Dietrich Austermann, former Economy Minister in Schleswig-Holstein presenting ISIT expansion plans. Pressconference June 08.



Fraunhofer board member Prof. Marion Schick congratulates Marie Theresa Alt and her training officer Arne-Veit Schulz-Walsemann for her distinguished apprenticeship.

## COOPERATION WITH INSTITUTES AND UNIVERSITIES

**Centro National Micro-electronics**, Barcelona, Spain

**Slovak Academy of Sciences**, Bratislava, Slovakia

**Intl. Centre of Biodynamics**, Bukarest, Rumania

**Cambridge University**, UK

**University of Cardiff**, Great Britain

**University of Coimbra**, Coimbra, Portugal

**Technische Universität Dresden**, Institut für Aufbau- und Verbindungstechnik

**Technische Universität Eindhoven**, Netherlands

**VTT**, Espoo, Finland

**University of Exeter**, Great Britain

**Fachhochschule Flensburg**

**University of Gdansk**

**Ernst-Moritz-Arndt-Universität (EMAU)**, Greifswald

**LETI, CEA (Commissariat à l'Energie Atomique)**, Grenoble, France

**Hochschule für Angewandte Wissenschaften**, Hamburg

**Technion**, Haifa, Israel

**Fachhochschule Westküste**, Heide

**Technische Universität Ilmenau**

**Christian-Albrechts-Universität**, Technische Fakultät, Kiel

**Fachhochschule Kiel**

**École Polytechnique Fédérale de Lausanne**, Switzerland

**IMEC**, Leuven, Belgium

**Lund University of Technology**, Lund, Sweden

**Monash University**, Melbourne, Australia

**Wehrwissenschaftliches Institut**, Munster

**DLR**, München

**CSEM**, Neuchâtel, Switzerland

**Sintef ICT**, Oslo, Norway

**Universität Oulu**, Finland

**École Polytechnique**, Paris, France

**University of Perugia**, Italy

**Drexel-University**, Philadelphia, USA

**University of Pisa**, Italy

**Royal Institute of Technology (KTH)**, Stockholm, Sweden

**IMS Chips**, Stuttgart

**VTT**, Technical Research Center of Finland, Tampere, Finland

**LAAS-CNRS**, Toulouse, France

**Universität Ulm**

**Uppsala University**, Uppsala, Sweden

**Plant Research International**, Wageningen, Netherlands

**Fachhochschule Vorarlberg**, Austria

**University Wroclaw**, Poland

**Fachhochschule Wedel**

**FBK**, Trento, Italy

**IEMN**, Lille, France

**Tyndall National Institute**, Cork, Ireland

## DISTINCTIONS

**Marie Theresa Alt**

Distinction of being best apprentice as a Mikro-technologie I focus Microsystems Technology at IHK Kiel for which she was awarded by Fraunhofer board member Prof. Marion Schick, München, November 2008.

**Bruno Elsholz**

Nominated from "The Human Genome Organization and Ocimum Biosolution and Gene Logic" as one of the Genomic Pioneers for his outstanding contribution to the field of Genomics and was given this recognition during the HGM 2008.



ISIT presentation at Hannover Messe, April 08.



Projectpartners of „Flottenversuch Elektromobilität“ in Berlin, June 08.

## TRADE FAIRS AND EXHIBITIONS

### Electronics/EP

*International Trade Fair for Components, Instruments and Measurement, January 28 – January 30, Stockholm, Sweden*

### EBL 2008

*Elektronische Baugruppen und Leiterplatten, February 13 – February 14, Fellbach*

### Hannover Messe 2008

*April 21 – April 25, 2008, Hannover*

### Sensor 2008

*The Measurement Fair, May 6 – May 8, 2008 Nürnberg*

### PCIM Europe 2008

*International Exhibition and Conference for Power Electronics / Intelligent Motion / Power Quality, May 27 – May 29, Nürnberg*

### SMT Hybrid Packaging 2008

*System Integration in Micro Electronics, Exhibition and Conference, June 3 – June 5, 2008, Nürnberg*

### Automatica 2008

*3. International Trade Fair for Automation and Mechatronics, June 10 – June 13, München*

### Biotechnica 2008

*16. International Trade Fair, Partnering and Award for Biotechnology October 7 – October 9, 2008, Hannover*

### Semicon Europa 2008

*International Trade Fair for Equipment, Material and Services for the Semiconductor, MST/MEMS, and Photovoltaic Industries, October 7 – October 9, Stuttgart*

### Electronica 2008

*23. International Trade Fair for Components, Systems and Applications in Electronics, November 11 – November 14, 2008, München*

### Medica 2008

*November 19 – November 22, 2008, Düsseldorf*



ISIT seminar activities.

## MISCELLANEOUS EVENTS

### Aspekte moderner Siliziumtechnologie

Public lectures.

Monthly presentations, ISIT, Itzehoe

### Produktgestaltung: Design for Excellence aktuell

Seminar: February 12 and  
December 2, 2008, ISIT,  
Itzehoe

### RoHS-konforme Baugruppenfertigung

Seminar: February 13 and  
December 3, 2008, ISIT,  
Itzehoe

### Der bleifreie Lötprozess in der Elektronikfertigung

Seminar: February 26 –  
February 29 and October  
7 – October 10, 2008, ISIT,  
Itzehoe

### Manuell bleifrei Löten – praxisorientierte Schulung

Seminar: March 11 – March  
13 and November 4 – No-  
vember 6, 2008, ISIT, Itzehoe

### SMT-Rework-Praktikum – praxisorientierte Schulung – bleifrei

Seminar: March 11 – 13 and  
November 4 – 6, 2008, ISIT,  
Itzehoe

### Lötprozess II – praxisorien- tierte Schulung zum „LEAD- FREE Specialist“ an der ISIT-LEADFREE Trainingslinie

Seminar: April 7 – April 11  
and November 24 – Novem-  
ber 28, 2008, ISIT, Itzehoe

### 20. CMP Users Meeting

April 11, 2008, ISIT, Itzehoe

### Pressconference “Fraunhofer ISIT initiiert neues Kompe- tenzzentrum Leistungselek- tronik in Schleswig-Holstein”

Speakers: Dietrich Auster-  
mann (former Minister for  
Economic Affairs in Schles-  
wig-Holstein) Dr. Wolfgang  
Windbracke, ISIT, April  
14, 2008, Fraunhofer ISIT,  
Itzehoe

### ISIT presentation in the framework of Seminar

„Boost Biosystems Broke-  
rage Event“, organized by  
Norgenta GmbH, Hamburg,  
April 23, 2008, Fraunhofer  
ISIT, Itzehoe

### Tutorial and Training “Re- liable Soldering for Power Electronics Manufacturing”

Seminar: June 18 – June 19,  
2008, ISIT, Itzehoe

### Pressconference “45-Millionen-Investition in ISIT-Erweiterung”

Speakers:  
Dietrich Austermann (former  
Minister for Economic Af-  
fairs in Schleswig-Holstein)  
Dr. Wolfgang Windbracke,  
ISIT, Prof. Dr. Ulrich Bul-  
ler, Member of Board of  
Fraunhofer-Gesellschaft,  
June 23, 2008, Fraunhofer  
ISIT, Itzehoe

### Pressconference Start of BMU-Verbundpro- jekt “Flottenversuch Elektro- mobilität”

June 26, 2008, Automobil-  
forum unter den Linden ,  
Berlin

### LEADFREE STEW Solder Trai- ning and Exhibition Weeks

Business and Conference  
Center, Timisoara CCIAT  
– CRAFT, Romania, July 7 –  
July 18, 2008

### 21. CMP Users Meeting

October 10, 2008, Congress  
Centrum, Boeblingen

### Intensivtraining Handlöten – praxisorientierte Schulung

Seminar: November 3 –  
November 7, 2008, ISIT,  
Itzehoe

### Pan-Mobile Erfassung mit optimierten Smart-Labels zur Effizienzsteigerung von Logistikprozessen

RFID Clustermeeting.  
November 5, 2008, Berlin

### Lötfachkraft 1 – Elektronik- fertigung an der Prototy- pen-Linie

Seminar: November 10 –  
November 14, 2008, ISIT,  
Itzehoe

### Lötfachkraft 2 – praxisori- entierete Schulung an der LEADFREE Trainingslinie

Seminar: November 24 –  
November 28, 2008, ISIT,  
Itzehoe

### Lötfachkraft 3 – Baugrup- penfertigung: Qualitätssi- cherung und Fehlerbehe- bung

Seminar: December 8 –  
December 12, 2008, ISIT,  
Itzehoe



## JOURNAL PAPERS, PUBLICATIONS AND CONTRIBUTIONS TO CONFERENCES

**B. Elsholz, A. Nitsche, J. Achenbach, H. Ellerbrook, L. Blohm, J. Albers, G. Pauli, R. Hintsche, and R. Wörl:**  
*Electrical Low Density Microarrays for Highly Sensitive Detection of Multiplex PCR Products from Biological Agents. Biosens. Bioelectron., 2008*

**T. Falat, K. Friedel, N. Marengo, S. Warnat:**  
*TSV constraints related to temperature excursion, pressure during moulding, materials used and handling loads. Microsystem Technologies, Vol. 15, No. 1, pp. 181-190*

**U. Hofmann, M. Oldsen, H.-J. Quenzer, J. Janes, M. Heller, M. Weiss, G. Fakas, L. Ratzmann, E. Marchetti, F. D'Ascoli, M. Melani, L. Bacciarelli, E. Volpi, F. Battini, L. Mostardini, F. Sechi, M. De Marinis, B. Wagner:**  
*Wafer-Level Vacuum Packaged Resonant Micro-Scanning Mirrors for Compact Laser Projection Displays. Proceedings of SPIE (International Society for Optical Engineering) Vol. 6882, Photonics West, Conference on MOEMS and Miniaturized System VII, San José, USA, 2008*

**C. Klein, E. Platzgummer, H. Loeschner, G. Gross, P. Dolezel, M. Tmej, V. Kolarik, W. Klingler, F. Letzkus, J. Butschke, M. Irmischer, M. Witt, W. Pilz:**  
*Projection Maskless Lithography (PML2): Proof-of-Concept Setup and First Experimental Results. SPIE Advanced Lithography – Emerging Lithographic Technologies XII International Conference, Session “Parallel E-Beam Lithography”, San Jose, California, USA, February 27, 2008*

**P. Lange, M. Melani, L. Bertini, M. De Marinis:**  
*Thermal Mass Flow Sensor for Measurement of Liquids (Water). Proceedings Smart System Integration. Barcelona, Spain, April 9 – April 10, 2008*

**P. Lange, N. Marengo, S. Gruenzig, S. Warnat, T. Semperowitsch:**  
*Dicing of Fragile MEMS Structures. Materials Research Society Fall Meeting 2008, Boston, December 1, 2008*

**P. Lange:**  
*Neuer Sensor zur Leckortung in Wasserverteilungsnetzen. Energie/Wasser – DVGW Jahressrevue, December, 2008*

**Y. Liu, B. Elsholz, S.-O. Enfors, and M. Gabig-Ciminska:**  
*Critical Factors for the Performance of Chip Array-Based Electrical Detection of DNA for Analysis of Pathogenic Bacteria. Anal. Biochem., 382 p. 77-86, 2008*

**K. Malecki, L. Pikur, K. Friedel, N. Marengo, G. Bock, G. Hillmann, A. Sigl:**  
*A Numerical Study on Heat Flow and Load Distribution during Chip to Wafer or Wafer to Wafer Bonding in Vacuum. Proceedings of EPTC Conference 2008, pp. 18-23*

**N. Marengo, W. Reinert:**  
*Kleines Raumwunder mit großer Zukunft. Mechatronik F&M, Issue 5-6/08, pp. 54-56*

**N. Marengo, W. Reinert, H. Kostner, G. Hillmann:**  
*Hybrid Chip-Scale Integration of Inertial MEMS by Chip-to-Wafer Vacuum Bonding. Proceedings of Smart Systems Integration 2008, pp. 351-358*

**N. Marengo, W. Reinert, S. Warnat, P. Lange, S. Gruenzig, G. Hillmann, H. Kostner, G. Bock, S. Guadagnuolo, A. Conte:**  
*Vacuum Encapsulation of Resonant MEMS Sensors by Direct Chip-to-Wafer Stacking on ASIC. 10th Electronics Packaging Technology Conference, Singapore, 2008*

**M. Melani, L. Bertini, M. De Marinis, P. Lange, F. D'Ascoli, L. Fanucci:**  
*Hot Wire Anemometric MEMS Sensor for Water Flow Monitoring. Proceedings Date 08, Munich, March 10 – March 14, 2008*

**P. Merz, M. Kandler:**  
*Kombisensor SD755: Mikro-mechanischer Inertialsensor für die Messung von Beschleunigung und Drehrate. Automobil Konstruktion, Konradin Verlag Robert Kohlhammer, 2008*

**G. Neumann:**  
*Lithium-Akkumulatoren: Vielseitige und leistungsfähige Speicher elektrischer Energie. Technik in Bayern 6, 2008*

**M. Oldsen, U. Hofmann, H.-J. Quenzer, J. Janes, C. Stolte, K. Gruber, M. Ites, F. Sörensen, B. Wagner:**  
*A Novel Fabrication Technology for Anti-Reflex Wafer-Level Vacuum Packaged Microscanning Mirrors. Proceedings of SPIE (International Society for Optical Engineering) Vol. 6887, Photonics West, Conference on Micromachining and Microfabrication Process Technology XIII, San José, USA, 2008*



**M. Oldsen, U. Hofmann,  
W. Reinert, H.-J. Quenzer,  
B. Wagner:**  
*Waferlevel Vacuum  
Packaging: Essential for  
Microscanners in Mobile  
Applications. ECS Transac-  
tions Vol. 14 No. 1, Chip  
in the Pampa (SBMicro),  
Gramado, Brasil, September,  
2008*

**H.-J. Quenzer, R. Dudde,  
H. Jacobsen, B. Wagner,  
H. Föll:**  
*Deposition of Functional PZT  
Films as Actuators in MEMS  
Devices by High Rate Sputte-  
ring. Proceedings of  
Nanotech 2008,  
June 1 – June 4, Boston, MA,  
USA 2008*

**S. Warnat, S. Gruenzig,  
N. Marengo, W. Reinert,  
P. Lange, R. Ecke:**  
*Through Silicon Vias in  
Micro-Electro Mechanical  
Systems. Proceedings of MRS  
Fall 2008 Meeting, Boston  
(MA), to be published*

**G. Zwicker:**  
*CMP for the Fabrication of  
Advanced MEMS Devices.  
Proceedings of Semicon-  
ductor Conference Dresden  
(SCD) 2008, Dresden, April  
23-24, 2008*



## TALKS AND POSTER PRESENTATIONS

### T. Ahrens:

*Impact of Voiding on Load-Free CSP Solder Joint Reliability, Electronics I EP, Stockholm, January 28 – January 30, 2008*

### T. Ahrens:

*Fertigungsgerechtes Baugruppen-Design: Standards für Padlayout, Lotpastendruck, Bestückung, Lötwärmebedarf, bleifrei. Seminar: Design for Excellence aktuell, Fraunhofer ISIT, Itzehoe, February 12 and December 2, 2008*

### T. Ahrens:

*Verantwortung im Design, Einbau der Zuverlässigkeit: Betriebsbelastung, Materialkombination, Anforderungen an Bauteile und Leiterplatten, Entwärmung. Seminar: Design for Excellence aktuell, Fraunhofer ISIT, Itzehoe, February 12 and December 2, 2008*

### T. Ahrens:

*DfX: Designprinzipien, Null-Fehler-Strategie, Bauteil-Verfügbarkeit, Chancen durch Redesign & bleifrei. Seminar: Produktgestaltung: Design for Excellence aktuell, Fraunhofer ISIT, Itzehoe, February 12 and December 2, 2008*

### T. Ahrens:

*Lötqualität, Lötmetallurgie, Lötberflächen, Flussmittel. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, Feb. 26 and October 7, 2008*

### T. Ahrens:

*Qualitätsprüfung an Leiterplatten, Prüfmethode, -standards, Ausfallbeispiele. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, February 27 and October 8, 2008*

### T. Ahrens:

*Baugruppen- und Fehlerbewertung, Inspektion Röntgenverfahren, Querschleife. Seminar: SMT-Rework-Praktikum, ISIT, Itzehoe, February 27, March 11, October 8 and November 4, 2008*

### T. Ahrens:

*Knackpunkte bleifreies Löten, Konstruktion, Prozess und Materialauswahl. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, February 28 and October 8, 2008*

### T. Ahrens:

*Bleifrei Reparaturlöten, Lote und Flussmittel, Löttemperatur und Wärmebeständigkeit der Materialien. Seminar: SMT-Rework-Praktikum, ISIT, Itzehoe, March 11 and November 4, 2008*

### T. Ahrens:

*Baugruppenreparatur, Fertigungsstrategien für zuverlässige Baugruppen. 11. Europäische Elektronik-technologie-Kolleg, Colonia St. Jordi, Mallorca, April 16 – April 20, 2008*

### T. Ahrens:

*Design for Excellence – Brückenschlag zwischen Design und Fertigung, Zuverlässigkeit / Modellierung der Lötstellen-degradation. Ifm Ecomatic Technologietag, Kressbronn, April 23, 2008*

### T. Ahrens:

*Qualitätsbewertung: Was wusste Aschenputtel von ISO 9000? Prozesskontrolle in der Elektronikfertigung, Hilpert Electronics, CH-Baden-Dättwil, May 8, 2008*

### T. Ahrens:

*Wer soll denn das Löten... On Board with Juki & ZEVAC, Kiel-Oslo-Kiel, September 5 – Sept. 7, 2008*

### T. Ahrens:

*Effect of Microvia and Voiding on the Reliability of Pb-free CSP Solder Joints. Joint International Conference and Exhibition, Electronics Goes Green 2008+, Merging Technology and Sustainable Development, Berlin, September 8 – September 10, 2008*

### T. Ahrens:

*Neue Fachkräfte braucht das Land – neues Ausbildungsprogramm für die Baugruppenfertigung Weichlöten in der Elektronikfertigung. Vorsprung durch Wissen und Kommunikation – Im Dialog die Zukunft meistern, 16. FED Kongress, Bamberg, September 25 – September 27, 2008*

### T. Ahrens:

*Poren in CSP-Lötverbindungen, Zuverlässigkeit, Via-In-Pad, bleihaltig/bleifrei. Seminar: Der Lötprozess in der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, October 9, 2008*

### T. Ahrens:

*Bleifreies Handlöten, OTTI Fachforum Weichlöten. Würzburg, October 20 – October 21, 2008*

### T. Ahrens:

*The Effect of Voiding on Lead-Free CSP Solder Joints – Reliability with and without Microvia-In-Pad. Workshop: Soldering Dynamics. European Electronics Assembly Reliability Summit, Tallinn, Estonia, October 22 – October 24, 2008*

### T. Ahrens:

*Baugruppen aufbauen und definiert zerstören: Zuverlässigkeitsprüfung. JUKI meets Friends 3. Fraunhofer ISIT, Itzehoe, October 29, 2008*

### T. Ahrens:

*Heat Dissipation – Package, Module and PCB Structures for Heat Dissipation, Transfer and Conduction. Technology-World 2008, Coventry, UK, Nov. 17, 2008*

### R. Dudde:

*Deposition of functional PZT Films as Actuators in MEMS Devices by High Rate Sputtering. Nanotech 2008, Boston, MA, USA, June 1 – June 4, 2008*



**J. Eichholz:**

*Mikromechanische Kraft/ Drehmoment-Sensoren für die Robotik. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, October 1, 2008*

**J. Eichholz:**

*Development of  $\mu$ -mirror for Laser Projection. Satellite Workshop of ICT, 3D Integration for Ambient Intelligence Application, Lyon, France, November 26, 2008*

**U. Hofmann:**

*Mikrospiegel für kompakte Laserprojektionssysteme im Mobiltelefon- und Automotive-Anwendungsbereich. IHK Seminar „Forschung erforschen, Itzehoe, January 29, 2008*

**T. Kraft:**

*Präparation von Durchkontaktierungen an Siliziumwafern (Cross-selection preparations for material analysis in through-silicon vias). Materialographie Konferenz, Jena, Germany, September 17 – September 19, 2008*

**P. Lange, M. Melani, L. Bertini, M. De Marinis:**  
*Thermal Mass Flow Sensor for Measurement of Liquids (Water). Proceedings Smart System Integration. Barcelona, Spain, April 9 – April 10, 2008*

**P. Lange:**  
*International Workshop on Drinking Water Loss*

*Reduction. Exhibition of Water Flow Meter for Water Loss Reduction, UN Campus, Bonn, Germany, September 3 – September 5, 2008*

**P. Lange, N. Marengo, S. Gruenzig, S. Warnat, T. Semperowitsch:**  
*Dicing of Fragile MEMS Structures. Materials Research Society Fall Meeting 2008, Boston, December 1 – December 5, 2008*

**P. Lange:**  
*The Challenge of Dicing MEMS Structures. Micro-Electromechanical System MEMS/MST, Semicon Conference, Stuttgart, Germany, October 7 – October 9, 2008*

**N. Marengo, W. Reinert, S. Warnat, P. Lange, S. Gruenzig, G. Hillmann, H. Kostner, G. Bock, S. Guadagnuolo, A. Conte:**  
*Vacuum Encapsulation of Resonant MEMS Sensors by Direct Chip-to-Wafer Stacking on ASIC. 10th Electronics Packaging Technology Conference, Singapore, 2008*

**N. Marengo:**  
*A Numerical Study on Heat Flow and Load Distribution during Chip-to-Wafer or Wafer-to-Wafer Bonding in Vacuum EPTC Conference, Singapore, December 9 – December 12, 2008*

**N. Marengo:**  
*Das sehende Auto – Mikrokameras unterstützen den Fahrer. Seminar: Aspekte*

*moderner Siliziumtechnologie, ISIT, Itzehoe, September 3, 2008*

**N. Marengo:**  
*Hybrid Chip-Scale Integration of Inertial MEMS by Chip-to-Wafer Vacuum Bonding. Smart Systems Integration, Barcelona, Spain, April 9 – April 10, 2008*

**N. Marengo:**  
*Reliability and Text Challenges around C2W and W2W SiP assemblies. Invited talk, Reliability and DfX Engineering Workshop, Pallanza, Italy, May 29, 2008*

**N. Marengo:**  
*The DAVID Integration Approach for Hybrid MEMS-Resonator Vacuum Packaging on CMOS-Wafer. Lyon, November 26, 2008*

**N. Marengo:**  
*Vacuum Encapsulation of Resonant MEMS Sensors by Direct Chip-to-Wafer Stacking on ASIC EPTC Conference, Singapore, December 9 – December 12, 2008*

**N. Marengo:**  
*Zuverlässigkeit durch Unterfüllen direct gelöteter Chips Fachforum „Kleben in der Elektronik“, Regensburg, February 20 – February 21, 2008*

**M. Melani, L. Bertini, M. De Marinis, P. Lange, F. D’Ascoli, L. Fanucci:**  
*Hot Wire Anemometric MEMS Sensor for Water*

*Flow Monitoring. Proceedings Date 08, Munich, March 10 – March 14, 2008*

**G. Melmer, S. Kraus, A. Merckelbach, S. Barth, E. Nebling, J. Nähring:**  
*Development of a Novel Diagnostic Chip for the Genotype Specific Detection of HCV. Science to Market - EAPB Conference, BIOTECH-NICA, Hannover, October 7 - October 9, 2008*

**P. Merz:**  
*Herstellung robuster MEMS Bauelemente: Einfluss von Material-, Design- und Prozesseigenschaften auf die Zuverlässigkeit von mikromechanischen Sensorsystemen. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, March 5, 2008*

**P. Merz:**  
*Herstellung robuster MEMS Bauelemente: Einfluss von Material-, Design- und Prozesseigenschaften auf die Zuverlässigkeit von mikromechanischen Sensorsystemen. Fraunhofer ISIT, Itzehoe, 2008*

**E. Nebling:**  
*Electrical Biochip Technology - A Universal Platform for Bioanalysis. ScanBalt - Boost Biosystems Industry Study Tour, Fraunhofer ISIT, Itzehoe, April 23, 2008*

**E. Nebling:**  
*Electrical Detection and Readout of the ivD-platform. Workshop: Die Fraunhofer*

*ivD-Plattform - eine modulare Entwicklungs- und Technologieplattform für die Point of Care Diagnostik, MEDICA, Düsseldorf, November 19 - November 22, 2008*

**G. Neumann:**  
*Lithiumakkumulatoren: Sicherheit und Materialien. VCC Elektrochemische Energiequellen, Lithium-Ionen-Batterien für Unterwasser-Marinesysteme, Erding, June 10 - June 11, 2008*

**T. Otto, J. Nestler, A. Morschhauser, M. Schueller, J. Krissler, F. Ebling, F. Bier, E. Ehrenreich-Foerster, N. Gajovic-Eichelmann, A. Grzesiak, M. Burgard, A. Brandenburg, G. Sulz, E. Nebling, T. Gessner:**  
*Highly Integrated Polymer-Based Technology Platform for In-Vitro Diagnostics. Smart Systems Integration Conference, Barcelona, April 9 - April 10, 2008*

**M.-H. Poech:**  
*Thermisches Management elektronischer Systeme - Teil 2: Bauelemente-Level Auswahl und Beschreibung von Aufbauvarianten, Bauelementen. Haus der Technik, Essen, February 26 - February 27, 2008*

**M.-H. Poech:**  
*Das Reflow-Lötprofil unter dem Zeichen bleifreier Fertigung, Temperaturverteilung in der Baugruppe. Seminar: Der Lötprozess in*

*der Fertigung elektronischer Baugruppen, ISIT, Itzehoe, February 26 and October 7, 2008*

**M.-H. Poech:**  
*Bleifreie Lötverbindungen - Ergebnisse zur Zuverlässigkeit. ZVE Technologieforum, Oberpaffendorf, October 23, 2008*

**M.-H. Poech:**  
*Sind bleifrei gelötete Baugruppen zuverlässig? 34. Treffen des Arbeitskreises „Zuverlässige, bleifreie Systeme“ des Fraunhofer IZM, Berlin, November 4, 2008*

**M.-H. Poech:**  
*High Current PCBs and Suitable Connection Techniques. ECPE Workshops "Advanced Cooling" and "Power PCBs and Busbars", Delfi, November 20 - November 21, 2008*

**J. Quenzer:**  
*Anwendungen von piezokeramischen Schichten in der Mikrosystemtechnik. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, November 5, 2008*

**H. Schimanski, T. Ahrens:**  
*Reworkstrategien in der Baugruppenfertigung - Lötprozessoptimierung bei eingeschränktem Prozessfenster und richtige Handhabung von Bauteilen und Baugruppen. 16. FED-Konferenz, Bamberg, September 25 - September 27, 2008*

**H. Schimanski, T. Ahrens:**  
*Reworksysteme im Einsatz - Baugruppenschonende Reworkprozesse Demonstration verschiedener Geräte und Verfahren. 16. FED-Konferenz, Bamberg, September 25 - September 27, 2008*

**H. Schimanski:**  
*Temperatur Measurement Exerc.. Timisoara, Romania, July 16, 2008*

**H. Schimanski:**  
*DfX - Design Prinzipien, Brückenschlag zwischen Design und Fertigung. Mönchengladbach, September 18, 2008*

**H. Schimanski:**  
*Komplexe SMT-Baugruppen. Seminar: SMT-Rework-Praktikum, ISIT, Itzehoe, November 4, 2008*

**B. Steible:**  
*Kupfer-CMP für die RF-MEMS-Fertigung. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, June 8, 2008*

**B. Wagner:**  
*2. Workshop „Norddeutsche Initiative Nanomaterialien“. Schleswig, November 27, 2008*

**S. Warnat, Ecke, N. Marenco, S. Gruenzig, W. Reinert, P.Lange:**  
*Through Silicon Vias in Micro-Electro Mechanical Systems. Fall MRS 2008, Boston*

**S. Warnat:**  
*Hybrid Chipscale Integration for Inertial Sensor Clusters Semicon 2008 Conference, Stuttgart, Germany, October 7 - October 9, 2008*

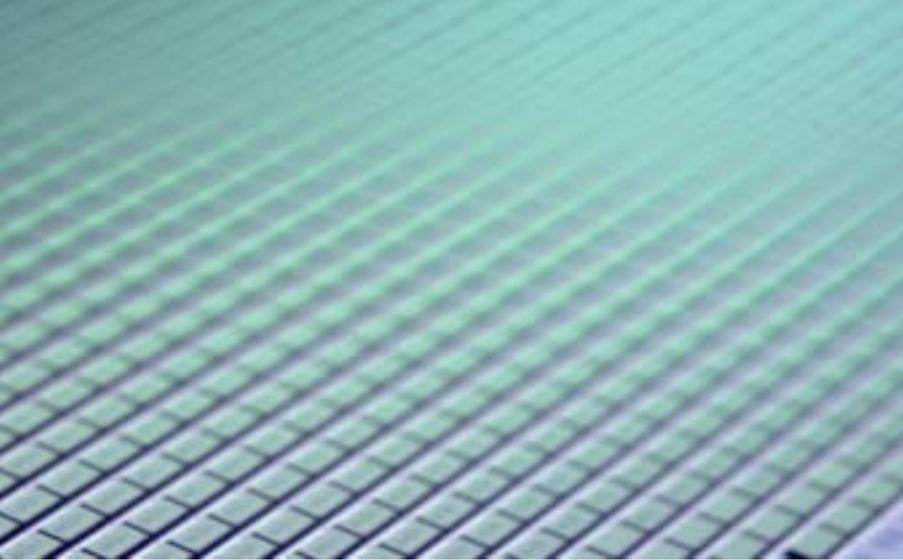
**S. Warnat:**  
*Integration of post-CMOS compatible Through Silicon Vias in MEMS (Metallization Aspects). Technical Faculty of the Cristian-Albrechts University to Kiel, Jan. 9, 2008*

**S. Warnat:**  
*Through Silicon Vias in Micro-Electro Mechanical Systems MRS Fall Meeting, Boston (MA), USA, December 1 - December 5, 2008*

**S. Warnat:**  
*Hybrid Chipscale Integration for Inertial Sensor Clusters Semicon 2008 Conference, Stuttgart, Germany, October 7 - October 9, 2008*

**A. Würsig:**  
*Neue Elektrodenmaterialien in Lithium-Polymer-Akkus für Anwendungen von der Medizintechnik bis zum Hybridfahrzeug. Seminar: Aspekte moderner Siliziumtechnologie, ISIT, Itzehoe, May 7, 2008*

**A. Würsig:**  
*Novel Electrolytes for Lithium-Titanate (Li4Ti5O12) based Lithium-Ion Batteries: Widening the Temperature Range. GDCH-Tagung Electrochemistry - Crossing Boundaries, Giessen, October 6 - October 8, 2008*



## DIPLOMA THESES

### **G. Zwicker:**

*Examples of CMP Processes for the Manufacturing of MEMS Devices. 2nd Annual CPMUG Meeting, Semicon West, San Francisco, July 16 – July 17, 2008*

### **G. Zwicker:**

*CMP for the Fabrication of Advanced MEMS Devices. Semiconductor Conference Dresden (SCD) 2008, Dresden, April 23 – April 24, 2008*

### **G. Zwicker:**

*CMP for the Manufacturing of MEMS Devices. 19th MicroMechanics Workshop Europe 2008 (MME), Aachen, September 28 – September 30, 2008*

### **G. Zwicker:**

*CMP – An Enabling Technology for MEMS Fabrication. SEMI International MEMS/ MST Industry Forum, Stuttgart, October 6, 2008*

### **Kai Gruber:**

*Strukturierbare Getter in MEMS Gehäusen, eine Machbarkeitsstudie für die Mikrosystemtechnik. Universität Hamburg, January, 2008*

### **Arthur Schott:**

*Entwicklung eines ASIC zur Steuerung und Signalerfassung eines resonanten MEMS Magnetfeldsensors. Technischen Universität Hamburg-Harburg (TUHH), September, 2008*

### **Jerome Tonn:**

*Optimierung einer Waferendvermessung auf der Basis mathematischer Auswerte- und Vergleichsstrategien. Fachhochschule Flensburg, February, 2008*

### **Thorge Wegers:**

*Aufbau einer relationalen Datenbank zur Überwachung und Organisation der Materialflussdaten einer Sensorproduktion und Entwicklung der benötigten Anwendersoftware. Fachhochschule Wedel, January, 2008*

### **F. Windbracke:**

*Charakterisierung der Herstellungstechnologie von feldplattenbasierenden Kompensationsdioden in MOS-Leistungstransistoren. Fachhochschule Westküste, Heide, December, 2008*

### **Stephan Wolff:**

*Mathematische Modellierung eines neuartigen mikromechanischen Drehratensensors unter Verwendung der finiten Elemente Methode. Fachhochschule Flensburg, February, 2008*



## OVERVIEW OF PROJECTS

- Development and fabrication of RF High Precision Capacitors
- Support for Build Up a 0,8  $\mu\text{m}$  CMOS Technology
- Support for Build Up a 0,35  $\mu\text{m}$  CMOS Technology
- Feedthrough and Wrap Around for Power Devices
- Optimierung von AMR Winkelsensoren
- Entwicklung von Cu-Pillars auf Basis dicker Lacke
- Durchkontaktierung von Power Devices mittels W-CVD
- Super Junction PowerMOS
- Ultrathin Trench IGBTs on sub-100  $\mu\text{m}$  Si-Substrates
- Simulationskonzept für 32 nm CMOS Technologien (SIMKON)
- Carbon Nanotube Devices for Integrated Circuit Engineering
- Untersuchung von Ceroxid-Dispersionen für CMP
- Untersuchung der Poliereigenschaften verschiedener Slurries für Cu-CMP
- Entwicklung von poly-Si CMP Prozessen für die MEMS Herstellung
- Untersuchung an mikro-mechanischen Drehraten-Sensoren
- Ev. Magnetometer für IMU
- Entwicklung von kapazitiven HF-Schaltern
- Entwicklung von piezoelektrischen Schichten für Si-Mikroaktuatoren
- Ultraschallanalyse flüssiger Mehrphasengemische
- Herstellung mikrooptischer Linsenarrays aus Glas
- RF-MEMS Packaging
- Zero- and First – Level Packaging of RF MEMS
- MEMS Pack
- Drehratensensoren für Raumfahrtanwendungen
- Piezoelektrischer Messkopf für die Ultraschallanalytik
- Mikroschnitt-Systeme für Display Anwendungen
- Mikrotechnische Fabrikation von Laserresonator-Spiegeln
- Herstellung mikrotechnischer analoger Ablenkeinheiten
- Charged Particle Nanotech, CHARPAN
- Maskless lithography for IC manufacturing, MAGIC
- Radical Innovation Maskless Nanolithography, RIMANA
- Mikrosystemtechnische Laserprojektion zur informatorischen Fahrerassistenz, MIKLAS
- Study on Silicon MEMS Force Sensors, SMERobot
- Development of an ASIC for the control of BLDC-motors
- Micro-Nano Integrated Platform for Transverse Ambient Intelligence Applications, MINAMI
- Probebased terabit memory. PROTEM
- Generic Manufacturing and Design Technology Platforms Based on Novel RF Technologies, RF-PLATFORM
- Customer Support and Design Centre for Physical Measurement Systems, EURO PRACTICE CCMesys
- Microactuator Competence Centre, EURO PRACTICE CCMicro
- Vollautomatische Detektion biologischer Gefahrstoffe mit integrierter Probenaufbereitung, BioPROB
- Genotype-Specific Hepatitis C Diagnostic Chip, HCV
- Entwicklung biochemischer Erkennungssysteme für portable elektrische Detektionssysteme von Biowaffen-Toxinen
- Elektrischer DBD-ISIT-eBS-Array-Immundefektor: Beratung, Bereitstellung und Spotten von Mikrochips für den Toxinnachweis, Service
- Analysesystem für die markergestützte intraoperative Tumordiagnostik
- USDEP, Ultrasensitive Detection of Emerging Pathogens
- ivD-MAVO, in vitro Diagnostik Plattform
- Chipkartenbestückung mit Grautonblenden
- Stressoptimierte Montage und Gehäusestechnik für mikromechanisch hergestellte Silizium-Drehratensensoren
- Glassfritt Vacuum Wafer Bonding
- Glaslotbonden mit strukturierten Capwafern und Musterwafern
- Automotives Mikrokamerasystem für Fahrzeugumfelderfassung,  $\mu$ -CAM
- Downscaled Assembly of Vertically Interconnected Devices, DAVID

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- *Wafer Level Packaging*
- *Process Development for hermetic AuSn vacuum sealing of  $\mu$  Bolometer Sensors on Wafer level*
- *Wafer Level Balling for 100  $\mu$ m up to 500  $\mu$ m Spheraes*
- *Customer Specified Test Wafers*
- *Neon Ultra Fine Leak Test for Resonant Micro Sensors*
- *Solder flip chip on flex*
- *Flip chip Embedding Study and Demonstration*
- *Qualitätsbewertung an bleifreien Baugruppen*
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- *Tin-Whisker Evaluation of Components and Assemblies with Tin Finishes*
- *Assistance for Electronics Manufacturers in the Transformation to RoHS Compliant Products and Processes*
- *Untersuchung zu den thermischen und prozesstechnischen Eigenschaften von Flussmitteln für bleifreie Lötlegierungen auf hochzuverlässigen Baugruppen*
- *Flottenversuch Elektromobilität*
- *Ionische Liquide für elektrochemische Applikationen (IL-Echem)*
- *Akkus für medizinische Anwendungen im Rahmen des EU-Projektes MINAMI (Micro-Nano integrated platform for transverse Ambient Intelligence applications)*
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- *Alterungsuntersuchungen an langzeitbetriebenen Lithiumakkumulatoren zur Solarstromspeicherung*
- *Amagnetische Lithiumzellen*
- **P. Birke, F. Salam**  
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- **P. Birke, G. Neumann**  
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- **H. J. Quenzer, P. Merz, A. V. Schulz**  
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- **H. J. Quenzer, P. Merz, M. Oldsen, W. Reinert**  
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We would be glad to answer your questions.

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