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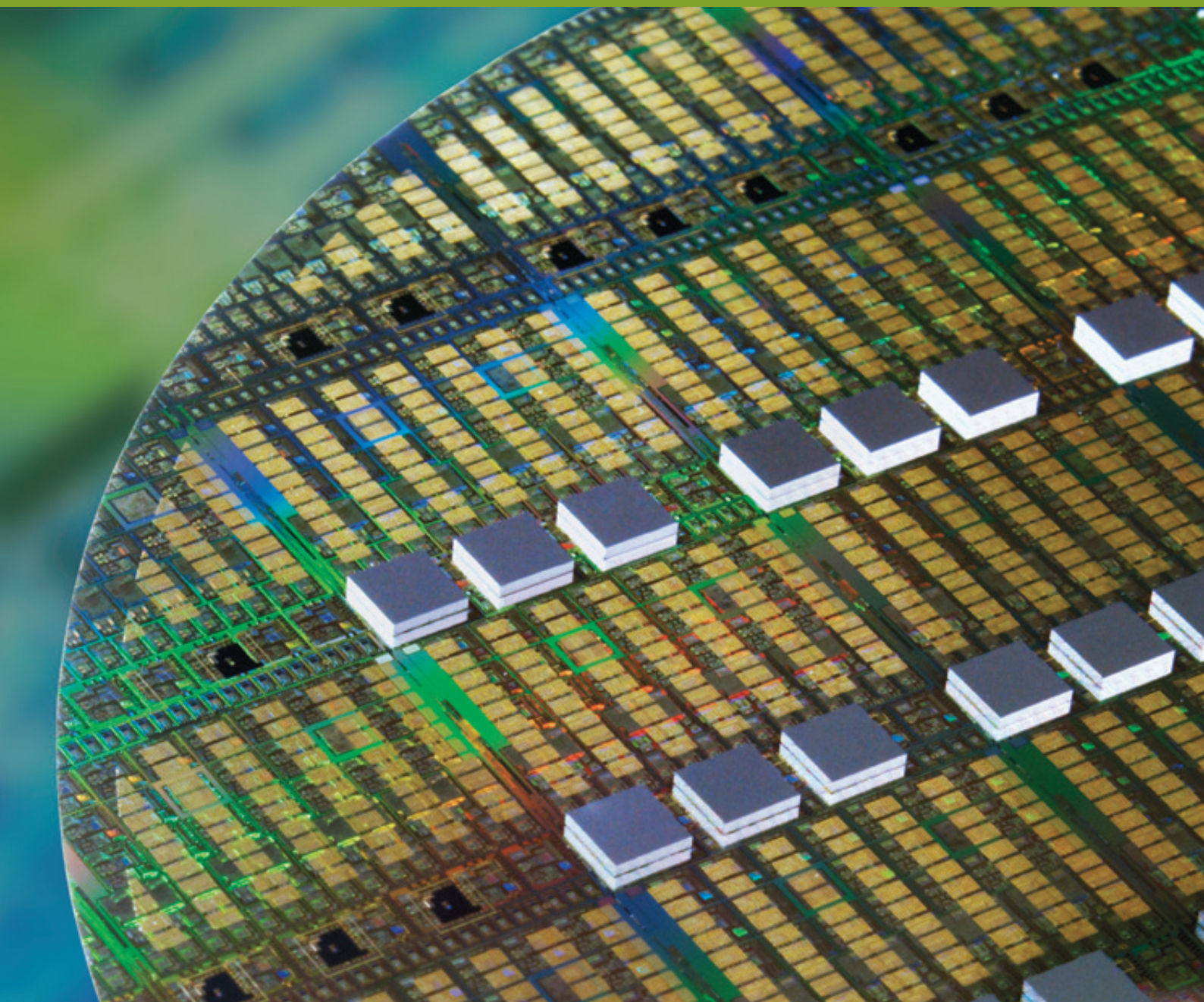
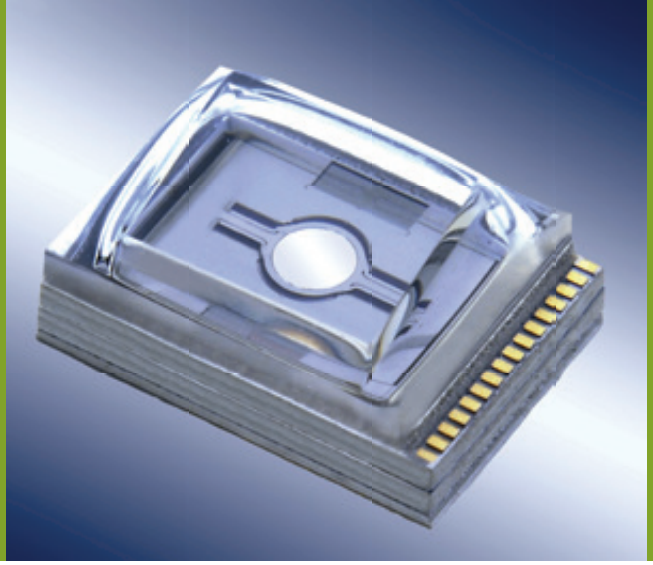
ISIT

FRAUNHOFER-INSTITUT FÜR SILIZIUMTECHNOLOGIE ISIT

ADVANCED PACKAGING FOR MICROSYSTEMS, SENSORS AND MULTICHIP MODULES



Part of a wafer with vacuum encapsulated gyroscope sensors



Vacuum packaged micro mirror for laser projection

SPECIAL REQUIREMENTS IN MOUNTING OF MICROSYSTEMS

The development of microsystems is a central working field of Fraunhofer ISIT. Hereby, special requirements are necessary for mounting and packaging technique referring the accuracy of component placement, the choice of bonding materials, and the minimization of stress. In recent years, ISIT has crucially enhanced its competences by developing security-relevant angular rate sensors for automotive industry. With the new MEMS pilot line for 200 mm, ISIT and in flexible facilities and quality management for development and pilot production of novel micro-system assemblies. On customer's request, the packaging development also can be accompanied with an FMEA. After successful qualifying the process can be transferred to a high-volume manufacturing environment.

WAFER LEVEL PACKAGING

Hermetic encapsulation

ISIT offers a wide portfolio of different hermetic sealing technologies on wafer level ranging from glass frit bonding over anodic bonding to a range of eutectic alloys (AuSn, AuSi, AlGe) and transient liquid phase bonding in the system CuSn and AuSn. Along with the encapsulation vertical electrical contacts can be manufactured. ISIT enables the vacuum encapsulation of optical micro devices based on it's glass-forming technology offering unique cap geometries with good optical properties.
Fraunhofer ISIT offers process customization and development of encapsulated wafers in 8" size, additionally the environment for pilot series of encapsulated components for evaluation of technology and reliability is also available.

Neon Ultra-Fine Leak Test

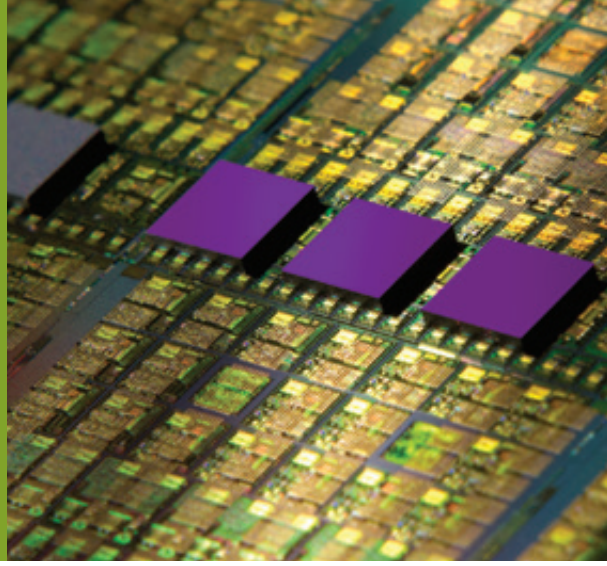
An extremely long lifetime up to 20 years is required by many applications today. In case of very small cavities, as they are formed by wafer-level packaging, air leak rates smaller than 10^{-14} mbar l/s have to be measured, which is nearly impossible by conventional techniques.

The Neon ultra-fine leak test, developed at ISIT, has been proven to detect leak rates as small as 10^{-17} mbar l/s. The only requirement is a micromechanical resonator with a high Q-factor. The test exposes a batch of wafers to defined Neon atmosphere. During a dwell time, Neon is diffused into the leaky devices, resulting in a mechanical damping of the resonator. A following measurement of the Q-factor change allows quantitative statements on the gas leakage.

MEMS-Chip Size Packaging

The increase of microstructured components in mobile electronic devices necessitates extremely miniaturized components with thicknesses below 1 mm. Fraunhofer ISIT is specialized on the advanced hybrid integration of micro components like e.g. inertial sensors with electronic driver circuits. Depending on chip geometry, this assembly method can also be applied on wafer level, which allows particularly thin assemblies. The institute has developed a modular toolbox of key technologies that allow a rapid customized component development. These key technologies comprise symmetrical wafer thinning of MEMS components, special dicing techniques to expose wirebond pads, electrical feedthroughs in wafers (TSV), chip-stacking techniques with adhesive transfer foils, spacer technologies, 3D wire bonding and solder bumping and balling. Transfer molding of assemblies can be performed in collaboration with external partners to realise an industrial pilot production of qualified sample parts.

MEMS-CSP vision of a 3D-integration of MEMS and ASIC



Realization of MEMS chip assembly on ASIC wafer

WAFER MODIFICATION

Bumping and Balling

For the application of solder balls on wafer- and substrate level, ISIT can offer two different technologies. CSP components are typically processed on wafer level using solder balls. The available facilities can process wafers up to 300 mm diameter with solderable contact metallisation. Solder balls down to 250 µm diameter are processed with high yield (> 99.9 %). Depending on customer's requirements, the process can be adapted to specific boundary conditions, e.g. special solder alloys, very thin wafers or wafers with TAIKO© geometry. Alternatively, a precision stencil printing technique is available to form flip-chip solder bumps with down to 250 µm pitch in industrial quality. For demonstration, pitch dimensions down to 170 µm can also be realized.

UBM

If no redistribution is needed, ISIT can offer an in-house developed chemical coating technology with Ni/Au.
The process can be realized up to 200 mm wafer diameter. Due to a long-time experience with a large variety of customer wafers the coating process is very stable. Generally, before wafer thinning the wafers are equipped with chemical Ni-Au UBM, subsequently the wafers can be thinned, bumped, and diced to target thickness. The processing of thinned wafers down to a thickness to 70 µm or wafers with TAIKO© geometry has been successfully performed.

Electrical Feedthrough Technology

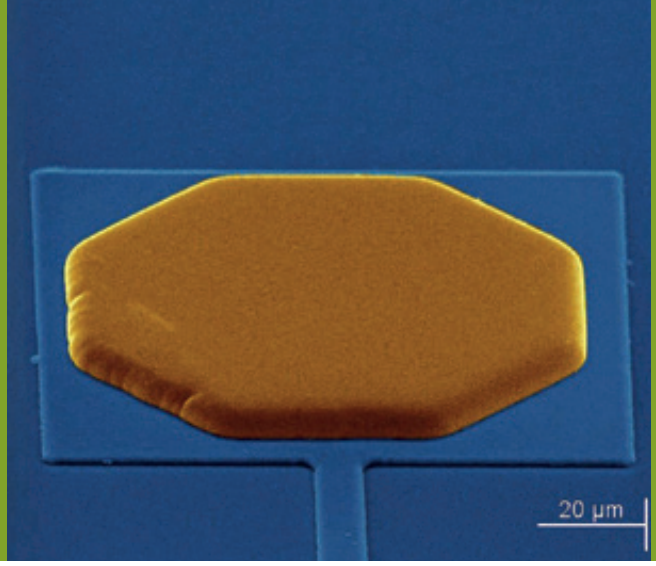
Fraunhofer ISIT has developed two different electrical feedthrough technologies (via) for microsystem and microelectronic applications. Vias in glass wafers are particularly suitable for optical MEMS packages and high frequency components. Comparably, dry-etched vias in silicon wafers enable a larger via density. Both technologies seal hermetically and are applicable on 200 mm wafers. They can be combined with contact redistribution and balling. The wafer thicknesses are in the range from 300 µm to 600 µm. Based on these predevelopments, customer specific solutions can be designed.

Sealing Frames

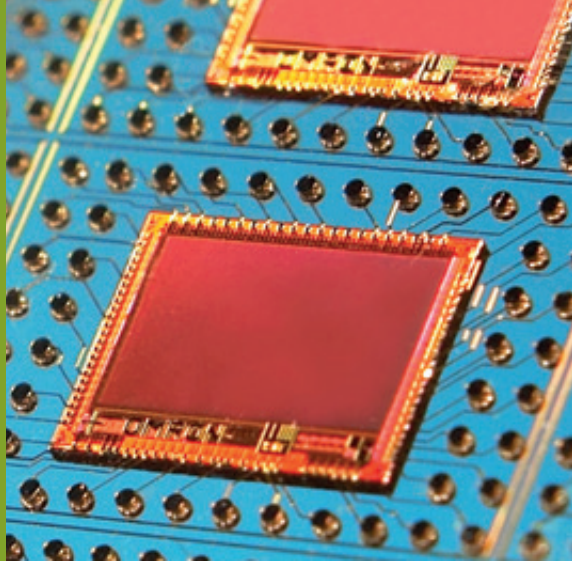
The deposition of metallic sealing frames on the active side of ASICs enables a direct connection to the micro sensor structures. The deposition of the frame structures and, when indicated, vertical contacts takes place on the entire wafer. ISIT has specific knowledge regarding the metallisation across elevated wafer topographies, the choice of adhesion promoting and barrier layers and the sealing process technology. For metal joints, e.g. in eutectic AuSn bonding, the wetting control of the formed liquid is of crucial importance for the bonding result.

Testwafers and Substrates

Test chips are extremely helpful for the development of process technologies, for material screening, and also for training purposes. Depending on the planned application, test chips with standard design or customer specific layout may be requested. The wafer thickness as well as the dicing pitch and the dicing foil can be varied. Test chips also can be equipped with solder bumps or chemical NiAu UBM. Due to the daisy-chain structure available on all test chips, the evaluation of process yields and reliability of most assembly technologies is possible. The test chips are usually provided as entire diced 200 mm wafers on foil. Customer specific samples with specific geometries, even on glass wafers, can be developed on demand. Glass dies are particularly suited for an accurate post-bond measurement of the die bonders alignment , precision and for optimizing underfill processes.



Contact pad with electroless Ni/Au UBM



Assembly of a picture sensor on a glass wafer with redistribution and balls

MODULE INTEGRATION

Stress-controlled packaging

The use of bonding and packaging materials with different coefficients of thermal expansion in combination with small component sizes result in high material stresses. In many sensors this can cause undesireable signal drift by temperature changes. High performance sensors, e.g. for process control, need an ageing-resistant condition with very low thermomechanical mismatch of the used materials. Fraunhofer ISIT can solve these problems by combining materials science and knowledge of processing technologies. The realisation of reproducible bonding methods enables the compensation of ageing effects by calibration of components.

Chip stacking method

The vertical integration of ASICs into a microsystem aims on improvement of component functionality, e.g. memory modules with high capacity. The ICs are processes as ultra-thin chips to realize very low assembly thickness. Fraunhofer ISIT has special knowledge to process ultra-thin chips up to 20 µm residual thickness. The chips are mounted in a layered structure which brings the flexible chips to a flexural resistant assembly. Contacting is carried out by sophisticated wire bonding or feed through technology in silicon. Fraunhofer ISIT persues this special mounting technology regarding optical sensors and actuators, e.g. by minimized cameras with integrated optics and projection systems with single mirror technique.

Fraunhofer ISIT
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